Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
Title	**Comments on IEEE 802.16.1pc-00/23**
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Re:	IEEE 802.16.1pc-00/23 "FEC Alternatives for BWA Burst Communications"
Abstract	The referenced submission contains errors, omissions, and potentially misleading statements. This submission corrects the errors etc. that relate to Block Turbo Codes.
Purpose	This submission is offered to the IEEE 802.16 group as a means of more accurately understanding FEC alternatives for BWA Burst Communications.
Notice	
Release	
Patent Policy and Procedures	

Comments on IEEE 802.16.1pc-00/23

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1.0 Introduction

Submission IEEE 802.16.1pc-00/23 [1] proposes several Forward Error Correction (FEC) schemes based on concatenated codes where the outer code is a Reed-Solomon code. As part of its argument for consideration of the proposed codes, the document compares them to codes contained in a conference paper [2]. The document also cites access to this information via the web (www.aha.com).

This submittal corrects the errors found in sections 5 and 6 of IEEE 802.16.1pc-00/23 and provides additional insights into the advantages of block turbo codes (BTC), which AHA refers to as Turbo Product Codes (TPCs).

The information needed to acquire the correct facts and conclusions are contained in the conference paper cited with additional supporting information available on the web site cited.

2.0 Corrections to IEEE 802.16.1pc-00/23 section 5.0

In the first paragraph of section 5.0, the document states, *"…..decoder engine for TPC is complex and sub-optimal the practical implementation is highly complex and speed limited (<40 Mbps)."*

Published articles, press releases [3] [4] and information publicly available show that the decoder technology used is easily within the range of requirements for 802.16 with announcements of low complexity decoders which can provide 10's of megabits/sec operation to high performance decoders operating in the 1 Gbit/sec range.

Also in the first paragraph, the document states, *"Although the code operates on a block and does not require interleaving, it does require iterative decoding…..which introduces latency. Therefore BTC if at all is more suitable for continuous transmissions (TDM) and not for bursts."*

The decoding latency of the cited TPC's is less than two block lengths [6] at the specified data rate. The first block length is used to acquire the block, and in the time required to receive the next block, the first block is corrected and output of the corrected data will begin. All iterations are done during this time.

In regards to suitability for burst communications, it is a well-known fact that TPCs are ideally suited for burst communications with many users of this technology designing TPC technology into their burst mode communications systems.

In the second paragraph the document states, *"In the plot a concatenated RS …+Conv. Code… was compared with a BTC based on a extended Hamming code (64,57) (coding rate about 0.7). The paper did an unfair comparison by assuming no interleaving for the first scheme while allowing 16 iterations for their own code."*

There are several inaccurate claims made in this paragraph. The cited paper [2] in fact did a fair comparison by making the block sizes identical (192 data bytes) and the code rates as close as practical. The comment regarding "no interleaving" is an incorrect assertion since adding even a depth 2 interleaver for the RS+C code would double its effective block size thereby not meeting the stated goal of a 192 byte packet. If the block size of the TPC block is also doubled the performance of the TPC solution would also improve.

As stated earlier, the latency of the cited TPC technology is similar to that of an equivalent block size RS solution no matter how many iterations are programmed into the decoder. Finally, there is no real relationship between iterations and interleaving.

On the next page of the submission is a plot, which makes a comparison of the proposed code solution to the previously mentioned 192 byte packet Bit Error Rate plot. The document makes at least one error on this plot as well as potentially misleading the reader into believing that the proposed solution can effectively compete with the TPC code.

First, the document includes a notation on the graph that the TPC simulation will degrade "at least 0.5 dB". This is patently false. The simulations are based on "bit and resolution" accurate results and have been verified with actual working hardware that was introduced in November 1998 [4]. Companies who have built and fielded

complete communication systems using the cited TPC technology further support this claim. One such company is Comtech Communications (www.comtechcom.com). Comtech has issued a public statement to this affect.

In addition, the document plots a "RS/Viterbi curve with perfect interleaving". As noted earlier, adding interleaving increases the effective block size of a code making such a comparison invalid since increasing the block size of a TPC code also increases its performance.

Note that the recent 802.16 contribution "Metrics and Techniques for Evaluation of FEC Systems" [8] suggests a set of metrics to evaluate different FEC coding schemes, which includes comparisons of block sizes. This will lead to better decisions regarding code selection. In addition to the metric's cited, packet error rates are also an important metric as not all FEC schemes will behave in the same manner.

One final note, we would like to point out that enhanced TPC (eTPC) technology introduced in 1999 and briefly mentioned in a press release [3], virtually eliminates the error flare seen in the mentioned plot thereby adding approximately another 1 dB of coding gain advantage over the RS+BC(40,32) solution at low bit error rates.

In the last paragraph of section 5.0, the document makes several errors. As mentioned earlier, the document makes a false assumption regarding the state of the art of TPC technology. The eTPC technology that was introduced last year pushes the asymptotic bound well below that shown on the plot.

Second the document claims "at least a 0.5 dB degradation should be expected." As mentioned earlier, this is not true. Third, the document claims its code is only 1-1.5 dB worse than the TPC *"…yet has no burden on hardware complexity as the TPC does."* In fact, there has been no public statement as to the complexity of the TPC decoder cited, nor has the document described the complexity of its proposed codes.

There is one TPC IC on the market today, and there will be at least two others that will be introduced this year. Additionally, cores for TPC decoder's [3] are available

In the concluding section (6.0), the document states that if coding rate flexibility is needed then the suggested parity check code could be replaced by *" a block code which can be soft decoded"* gaining up to 2 dB more coding gain. The document offers no concrete solution, does not comment on the implementation cost of alternative solution, and does not provide any simulation results.

In response, note that a unified TPC design can readily support code rates from rate 1/5 to rate 0.98 with no change in coding strategies or additional hardware. In addition to the cited TPC technology, others [5] have published papers extolling the virtues of block turbo codes (aka BTC and TPC) and have published alternative decoding strategies for the decoding of these codes.

Also in this last section, the document states that *"Block Turbo codes are not suitable for BWA burst communications as they fail to deliver their theoretical performance for a reasonable "price" and impose processing speed limitations. Even when compared to the traditional concatenated coding for continuous transmissions a performance advantage of 1 dB is not attractive enough."*

As noted previously these comments are either false or subjective and are not supported by fact.

In closing, generic block turbo codes were described in published papers and textbooks almost twenty years ago. The required encoder for a block code was described in the literature in 1954. As such, it is believed that anyone can build either an encoder or decoder for this technology without IP infringement, subject to specific decoder SISO implementations. AHA has patented SISO technology, which it makes available for fair and reasonable license terms via its Galaxy Core Generator. Companies who wish to pursue decoder designs based on alternative decoder strategies may do so without a license from AHA.

In addition, there are indications that several other companies will soon have TPC (block turbo code) technology that provides significant coding gain advantages at an implementation cost that can be used to either improve performance or be applied to other link budget cost factors such power amplifiers, antenna sizes, or lower cost receivers.

3.0 References

[1] IEEE 802.16.1pc-00/23 submission , Jay Klein, Ensemble Communications, Inc, 4/24/00

[2] Hewitt, E, "Turbo Product Codes for LMDS," IEEE Radio and Wireless Conference, August 1998

[3] Press Release, "AHA announces Turbo Product Code Core Generator", September 20 1999

[4] Press Release, "AHA announces Turbo Product Code Forward Error Correction Technology", Nov. 2, 1998

[5] R. Pyndiah, "Near-Optimum Decoding of Product Codes: Block Turbo Codes" IEEE Trans. Comm., vol. 46, pp. 1003-1010

[6] Specification, "AHA4501 36 Mbits/sec Turbo Code Encoder/Decoder," November 1998

[7] P. Elias, "Error-Free Coding, " IRE Trans. Inf. Theory, PGIT-4, pp.29-37, September 1954

[8] IEEE 802.16.1pc-00/25 submission, Eric Jacobsen, Intel Corp., 4/26/00