Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
Title	**FEC Performance of Concatenated Reed-Solomon and Convolutional Coding with Interleaving**
Date Submitted	**2000-06-08**
Source(s)	Jeff Foerster Alcatel 1221 Crossman Avenue Sunnyvale, CA 94089 Voice: 408-745-3983 Fax: 408-745-0390 mailto: jeff.r.foerster@alcatel.com John Liebetreu Sicom, Incorporated 8515 East Anderson Drive Scottsdale, AZ 85255 Voice: 480-607-4830 Fax: 480-607-4806 mailto: john@sicom.com
Re:	This document is a response to the call for contributions, document IEEE 802.16.1p-00/06, asking for the performance of FEC schemes applicable to broadband wireless access systems.
Abstract	This contribution provides the performance metrics for the concatenation of an outer Reed-Solomon code followed by a byte interleaver and an inner convolutional code, which is currently defined in the Mode A of the draft physical layer standard.
Purpose	To assist the 802.16.1 working group in evaluating the best code selection for the standard.
Notice	This document has been prepared to assist IEEE 802.16. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein.
Release	The contributor grants a free, irrevocable license to the IEEE to incorporate text contained in this contribution, and any modifications thereof, in the creation of an IEEE Standards publication; to copyright in the IEEE's name any IEEE Standards publication even though it may include portions of this contribution; and at the IEEE's sole discretion to permit others to reproduce in whole or in part the resulting IEEE Standards publication. The contributor also acknowledges and accepts that this contribution may be made public by IEEE 802.16.
Patent Policy and Procedures	The contributor is familiar with the IEEE 802.16 Patent Policy and Procedures (Version 1.0) <http://ieee802.org/16/ipr/patents/policy.html>, including the statement "IEEE standards may include the known use of patent(s), including patent applications, if there is technical justification in the opinion of the standards-developing committee and provided the IEEE receives assurance from the patent holder that it will license applicants under reasonable terms and conditions for the purpose of implementing the standard." Early disclosure to the Working Group of patent information that might be relevant to the standard is essential to reduce the possibility for delays in the development process and increase the likelihood that the draft publication will be approved for publication. Please notify the Chair <mailto:r.b.marks@ieee.org> as early as possible, in written or electronic form, of any patents (granted or under application) that may cover technology that is under consideration by or has been approved by IEEE 802.16. The Chair will disclose this notification via the IEEE 802.16 web site <http://ieee802.org/16/ipr/patents/letters>.

FEC Performance of Concatenated Reed-Solomon and Convolutional Coding with Interleaving

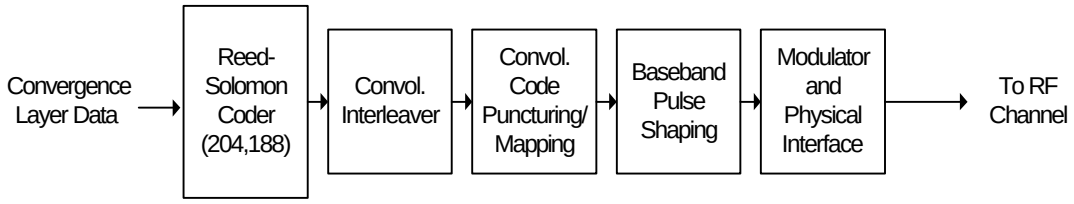
Jeff Foerster and John Liebetreu

Introduction

The purpose of this contribution is to provide the performance of the concatenated Reed-Solomon and convolutional code that is described in Mode A of the current draft physical layer standard. This code is only applicable for the downstream channel that uses a continuous transmission stream in a frequency division duplexed (FDD) system. As a result, it may not be appropriate for a frequency switched division duplexed (FSDD) system or a time division duplexed (TDD) system, unless the interleaver is shortened and the convolutional code is terminated through tail biting. These latter options are not considered here. In addition, it may not be appropriate for systems that employ adaptive modulation in the downstream channel, due to the overall length of the concatenated code and interleaver. However, this code does provide a strong coding gain with flexibility in the selection of the code rate and modulation level, as will be shown. In addition, this code has been used for years in the digital video broadcasting (DVB) environment [1], and has mature implementations in silicon that closely approximate the theoretical performance predicted for the code.

Code Description

The code analyzed in this contribution for the downstream channel is shown in the following block diagram.



Conceptual Block diagram of the Concatenated Reed-Solomon/Convolutional Coding Scheme

Following the convergence layer, systematic shortened (204,188) Reed-Solomon encoding is performed on each received 188 byte packet, with T = 8. This means that 8 erroneous bytes per transport packet can be corrected. This process adds 16 parity bytes to the transport packet to give a 204 byte codeword.

The Reed-Solomon code has the following generator polynomials:

Code Generator Polynomial: $g(x) = (x+\mu^0)(x+\mu^1)(x+\mu^2) \ldots (x+\mu^{15})$, where μ= 02hex

Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$

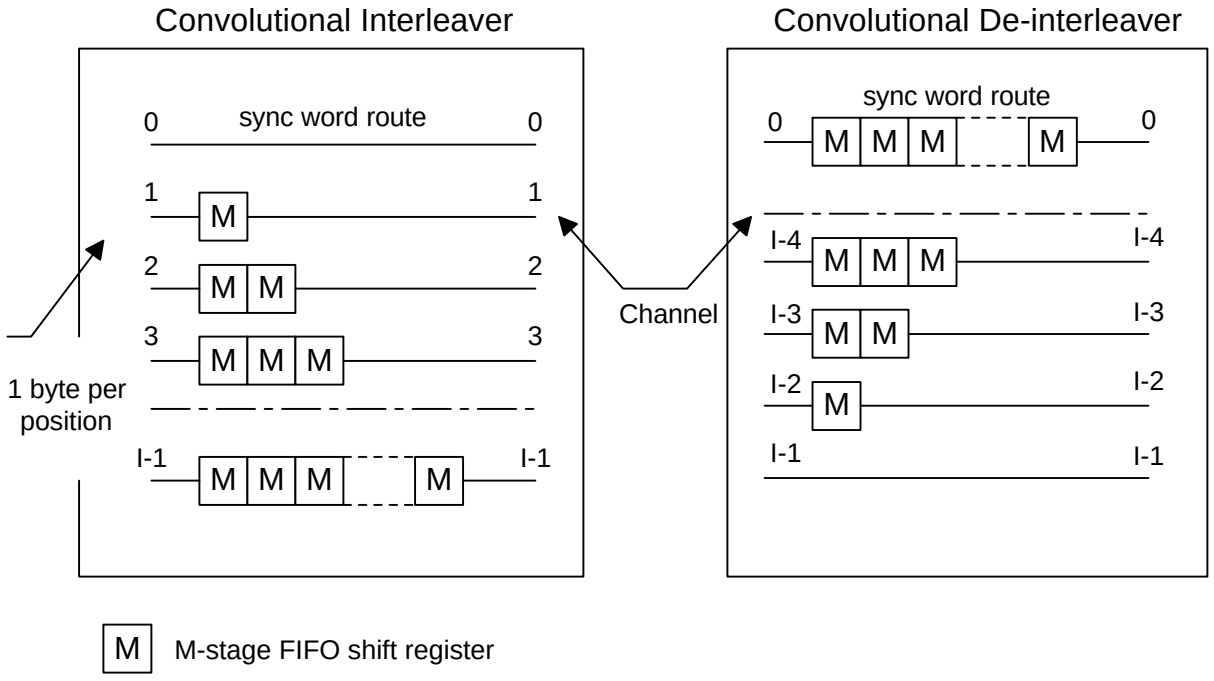
The shortened Reed-Solomon code is implemented by appending 51 bytes, all set to zero, before the information bytes at the input of a (255,239) encoder; after the coding procedure these bytes are discarded.

The convolutional interleaving process is based on the Forney approach, with a depth of I=12. The interleaved frame is composed of overlapping error protected packets and shall be delimited by synch. bytes (preserving the periodicity of 204 bytes).

The interleaver is composed of I branches, cyclically connected to the input byte-stream by the input switch. Each branch shall be a First In First Out (FIFO) shift register, with depth (M) cells (where M = N/I, N = 204 = error protected frame length, I =12 = maximum interleaving depth, j = branch index). The cells of the FIFO shall contain 1 byte, and the input and output switches shall be synchronized, as shown in the diagram below.

For synchronization purposes, the sync bytes and the inverted sync bytes shall be always routed into the branch "0" of the interleaver (corresponding to a null delay).

The deinterleaver is similar, in principle, to the interleaver, but the branch indexes are reversed (i.e. j = 0 corresponds to the largest delay). The de-interleaver synchronization is achieved by routing the first recognized sync byte into the "0" branch.



Conceptual diagram of the convolutional interleaver and de-interleaver

The convolutional code is chosen from the following table of code rates, which are obtained by puncturing a rate 1/2 constraint length K = 7 code having the following generator vectors G, and puncturing patterns P (0 denotes punctured (deleted) bit).

Convolutional Code Puncture Patterns

Original code			**Code rates**									
			1/2		2/3		3/4		5/6		7/8	
K	G_1	G_2	P	d_{free}	P	d_{free}	P	d_{free}	P	d_{free}	P	d_{free}
7	171_{oct}	133_{oct}	X=1 Y=1 I=X_1 Q=Y_1	10	X=10 Y=11 I=$X_1Y_2Y_3$ Q=$Y_1X_3Y_4$	6	X=101 Y=110 I=X_1Y_2 Q=Y_1X_3	5	X=10101 Y=11010 I=$X_1Y_2Y_4$ Q=$Y_1X_3X_5$	4	X=1000101 Y=1111010 I=$X_1Y_2Y_4Y_6$ Q=$Y_1Y_3X_5X_7$	3
NOTE: 1=transmitted bit 0 = non transmitted bit												

Finally, the bit pairs out of the convolutional encoder are mapped to gray-coded QPSK symbols.

Analytical Performance

The results presented here are primarily based on a theoretical evaluation of the concatenated Reed-Solomon and convolutional code. The following analysis has been widely used in the literature (see [2]-[7]) and has been shown to yield results that very closely approximate simulation results. The performance of the convolutional code is approximated truncating the union bound after a significant number of terms, and can be expressed by the following:

$$P_{cb} \approx \frac{1}{k} \sum_{d=d_{free}}^{d_{free}+N} c_d P_d \ ,$$

where k is the number of bits input into the encoder, d_{free} is the free distance of the convolutional code, c_d is the total number of bit errors that occur in all the incorrect paths in the trellis that differs from the correct path in exactly d positions, P_d is the probability of choosing an incorrect path that differs from the correct path in exactly d positions, and N is the number of significant terms used in the calculation. The values for d_{free} and c_d are well tabulated in [2] and [3] for all the punctured codes given above, and are given in the table below for easy reference. For coherent QPSK, P_d is given by the following equation:

$$P_d = \frac{1}{2}\mathrm{erfc}(\sqrt{dg_c}),$$

where $g_c = qg_b$, g_b is the SNR per informatin bit, and q is the overall code rate of the concatenated R-S and convolutional code. Assuming interleaving between the Viterbi decoder and the Reed-Solomon decoder is sufficiently long to break up long bursts of errors out of the Viterbi decoder, which is the case here, the Reed-Solomon symbol error probability, for symbols in GF(2^b) can be upper bounded by the simple union bound [6][7] as follows:

$$P_s \le bP_{cb}$$

where, in this case, b=8. This symbol error probability can then be used in the following equation to yield an overall bound on the bit error probability out of the Reed-Solomon decoder [5], as follows:

$$P_b < \frac{1}{n}\sum_{i=T+1}^{n} i\binom{n}{i}P_s^i(1-P_s)^{n-i}$$

where n=204 is the length of the Reed-Solomon code and T=8 is the error correction capability of the code.

The following graphs illustrate the performance of these codes. Figure 1 shows simulation results for some of the convolutional codes analyzed here and verifies that the union bound approximation for the bit error rate out of the convolutional code is accurate for a bit error rate < 10^{-3}. Figure 2 provides the analytical performance of all the convolutional codes considered here, and Figure 3 provides the analytical results for the concatenated Reed-Solomon and convolutional code. Finally, tables are provided which summarize the performance results at bit error rates of 10^{-6} and 10^{-9}.

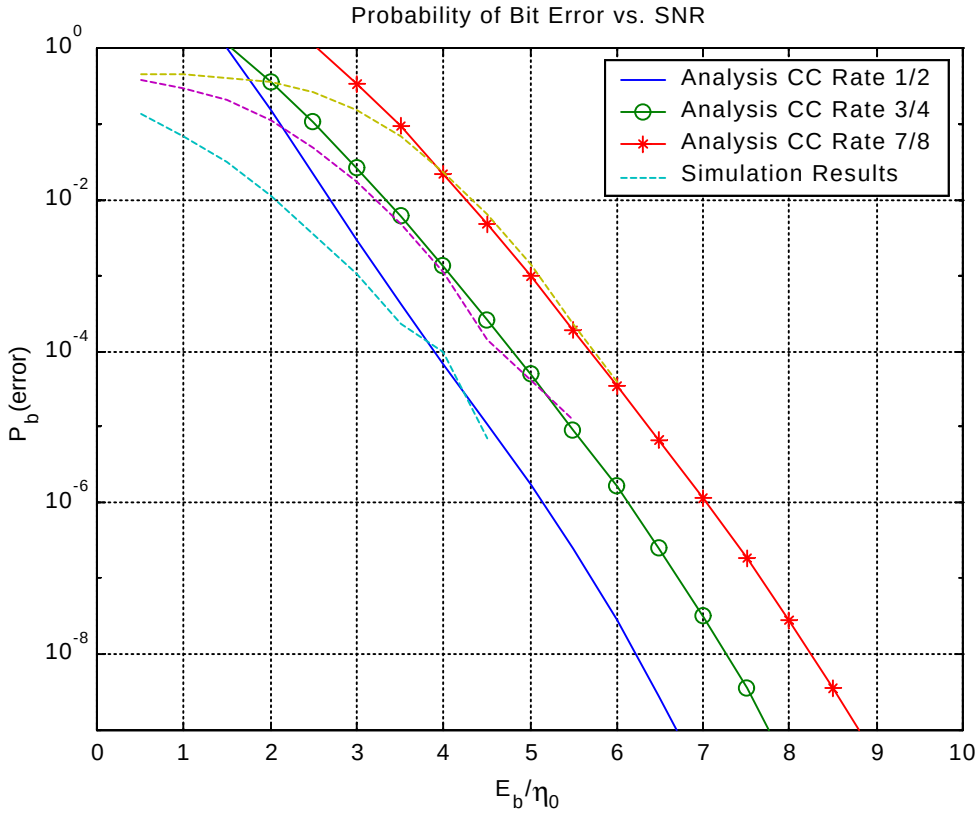


Figure 1: Comparison between Analysis and Simulation of Convolutional Code Performance

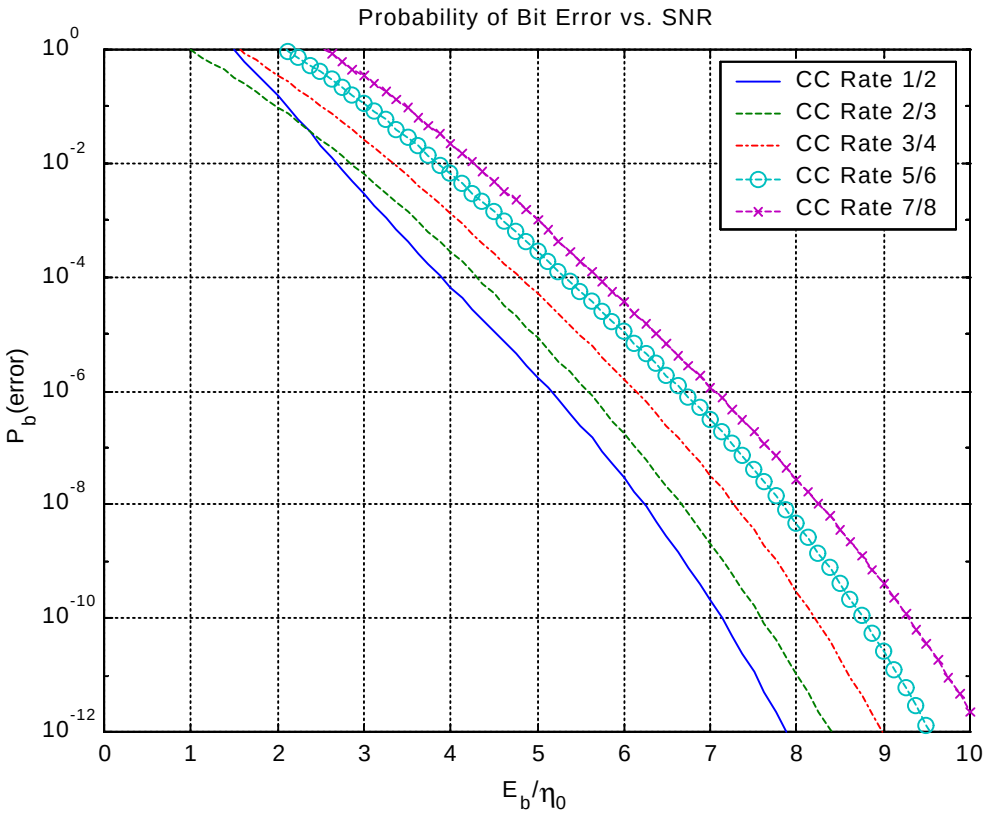


Figure 2: Performance of Convolutional Codes

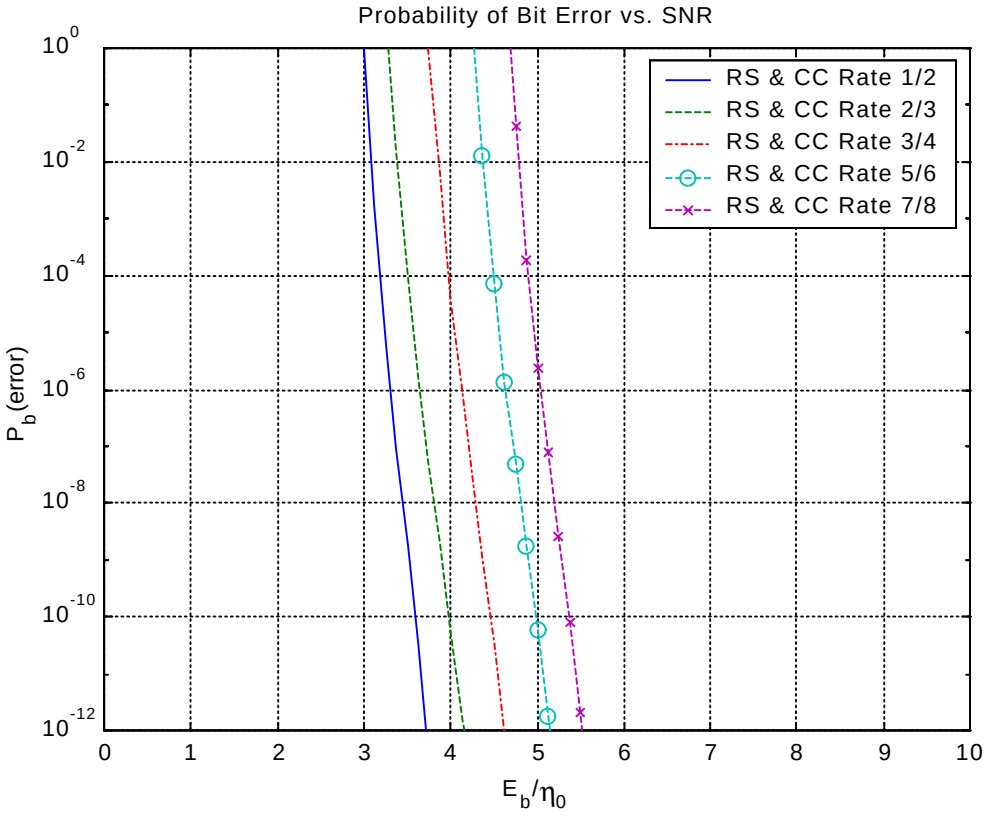


Figure 3: Performance of Concatenated Reed-Solomon with Convolutional Code

Code	½	2/3	¾	5/6	7/8
d_{free}	10	6	5	4	3
c_d	[36,0,211,0,1404,0,11633,0,77433,0,502690,0,3322763,0,21292910,0,134365911,0]	[3,70,285,1276,6160,27128,117019]	[42,201,1492,10469,62935,379644]	[92,528,8694,79453,792114]	[9,500,7437,105707,1402743]
E_b / h_0 for BER=10^{-9} at RS decoder output	3.6250	4	4.5000	5	5.3750
BER out of convolutional decoder	2.6120e-004	2.7735e-004	2.6187e-004	2.7833e-004	2.8799e-004
E_b / h_0 for BER=10^{-6} at RS decoder output	3.3750	3.7500	4.1250	4.7500	5.1250
BER out of convolutional decoder	6.6746e-004	6.3073e-004	8.7689e-004	6.2099e-004	6.5700e-004

Comparison Table

Code	½	2/3	¾	5/6	7/8
Aggregate Code Rate	0.4608	0.6144	0.6912	0.768	0.8064
Uplink/Downlink/Both	Downlink	Downlink	Downlink	Downlink	Downlink
E_b / h_0 for BER=10^{-6}	3.3750	3.7500	4.1250	4.7500	5.1250
E_b / h_0 for BER=10^{-9}	3.6250	4	4.5000	5	5.3750
Encoder Complexity (QPSK)	11,000 gates 16kb RAM)	One encoder accommodates all rates. Value in column 2 includes RS encoder, convolutional encoder, and Forney interleaver specified in [1]			
Encoder Complexity (64QAM; gates)	No additional *encoder* complexity; the *encoder* is the same as the basic rate 1/2 concatenated encoder.				
Decoder Complexity (QPSK; gates)	94,000 gates 27kb RAM	One decoder accommodates all rates. Value in column 2 includes RS decoder, convolutional decoder, and Forney deinterleaver specified in [1]			
Decoder Complexity (64QAM; gates)	No additional *decoder* complexity; the *decoder* is the same as the basic rate 1/2 concatenated decoder.				
Block size, in payload data bits.[1]	16,544 payload bits	16,544 payload bits	16,544 payload bits	16,544 payload bits	16,544 payload bits

Latency (end to end), in payload data bits.[1]	16,544 payload bits + decoder delay	16,544 payload bits + decoder delay	16,544 payload bits + decoder delay	16,544 payload bits + decoder delay	16,544 payload bits + decoder delay

[1] Although this code is not a block code, it can be viewed as having an approximate block size = I*(I-1)*M.

Support for higher order modulations

The same coding structure can be used to support 8-PSK and 16-QAM modulation using a pragmatic trellis coding approach, as described in [8].

References

[1] ETSI EN 300 421 V1.1.2 (1997-08), "Digital Video Broadcasting (DVB); Framing structure, channel coding and modulation for 11/12 GHz satellite services."

[2] J. Conan, “The Weight Spectra of Some Short Low-Rate Convolutional Codes,” *IEEE Trans. on Commun.*, p. 1050-1053, Vol. COM-32, No. 9, Sept. 1984.

[3] L.H.C. Lee , *Convolutional Coding: Fundamentals and Applications,* Artech House, Inc., 1997.

[4] J. Klein, “FEC Alternative for BWA Burst Communications,” IEEE 802.16.1pc-00/23.

[5] J. Proakis, *Digital Communications,* Second Edition, McGraw-Hill, 1989.

[6] A. Lapidoth, “On the Probability of Symbol Error in Viterbi Decoders”, *IEEE Trans. on Commun.*, p. 152-155, Vol. 45, No. 2, Feb. 1997.

[7] R. Cideciyan, E. Eleftheriou, and M. Rupf, “Concatenated Reed-Solomon/Convolutional Coding for Data Transmission in CDMA-Based Cellular Systems,” *IEEE Trans. on Commun*., p. 1291-1303, Vol. 45, No. 10, Oct. 1997.

[8] ETSI EN 301 210 V1.1.1 (1999-03), "Digital Video Broadcasting (DVB); Framing structure, channel coding and modulation for Digital Satellite News Gathering (DSNG) and other contribution applications by satellite."