

BTC Capabilities Overview

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Purpose:

This presentation summarizes the Block Turbo Code submittal to the the FEC Ad Hoc committee.

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Block Turbo Code

(Turbo Product Code)

Capability and Benefit Summary

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Based on 802161pc-00_35

Overview

- Block Turbo Codes (BTCs) are very flexible
- Can support any data block size, resolution 1 bit
- BTCs can support a very wide range of code rates with a single, unified encoder/decoder strategy
- From below rate $1/3$ to as high as rate 0.98
- Multiple vendor support exists
- Simulation results show that performance results are similar for different vendor implementations

802.16 Small Block Performance

| Code | 39,32 x 39,32 sb 0 | 46,39 x 46,39 sb 17 | 63,56 x 63,56 sb 0 |
|---|--|---|--|
| Aggregate Code Rate | 0.673 | 0.717 | 0.790 |
| Uplink/Downlink/Both | Downlink | Downlink | Downlink |
| Eb/No Required @ 10 ⁻⁶ QPSK/16QAM/64QAM | 3.5/6.5/10.7 dB | 3.6/6.6/10.5 dB | 3.5/6.9/11.0 dB |
| Eb/No Required @ 10 ⁻⁹ QPSK/16QAM/64QAM | 4.3/7.5/11.7 dB | 4.3/7.8/11.5 dB | 4.3/7.5/12.0 dB |
| Encoder Complexity QPSK/16QAM/64QAM | 10 Kgates | 10 Kgates | 10 Kgates |
| Decoder Complexity QPSK/16QAM/64QAM | < 150 Kgates @ 5 iter and 240 Mbits/sec | < 150 Kgates @ 5 iter and 240 Mbits/sec | < 150 Kgates @ 5 iter and 240 Mbits/sec |
| Block size (payload bits) | 1024 (128 bytes) | 1504 (188 bytes) | 3136 (392 bytes) |
| Latency | < 2 coded blocks | < 2 coded blocks | < 2 coded blocks |

Note: Gate counts are for a single encoder or decoder that supports all of the small block codes shown. Estimates take into account all memory requirements.

- 5, 14 and 57 byte codes also included in submittal

Large Block Code Performance

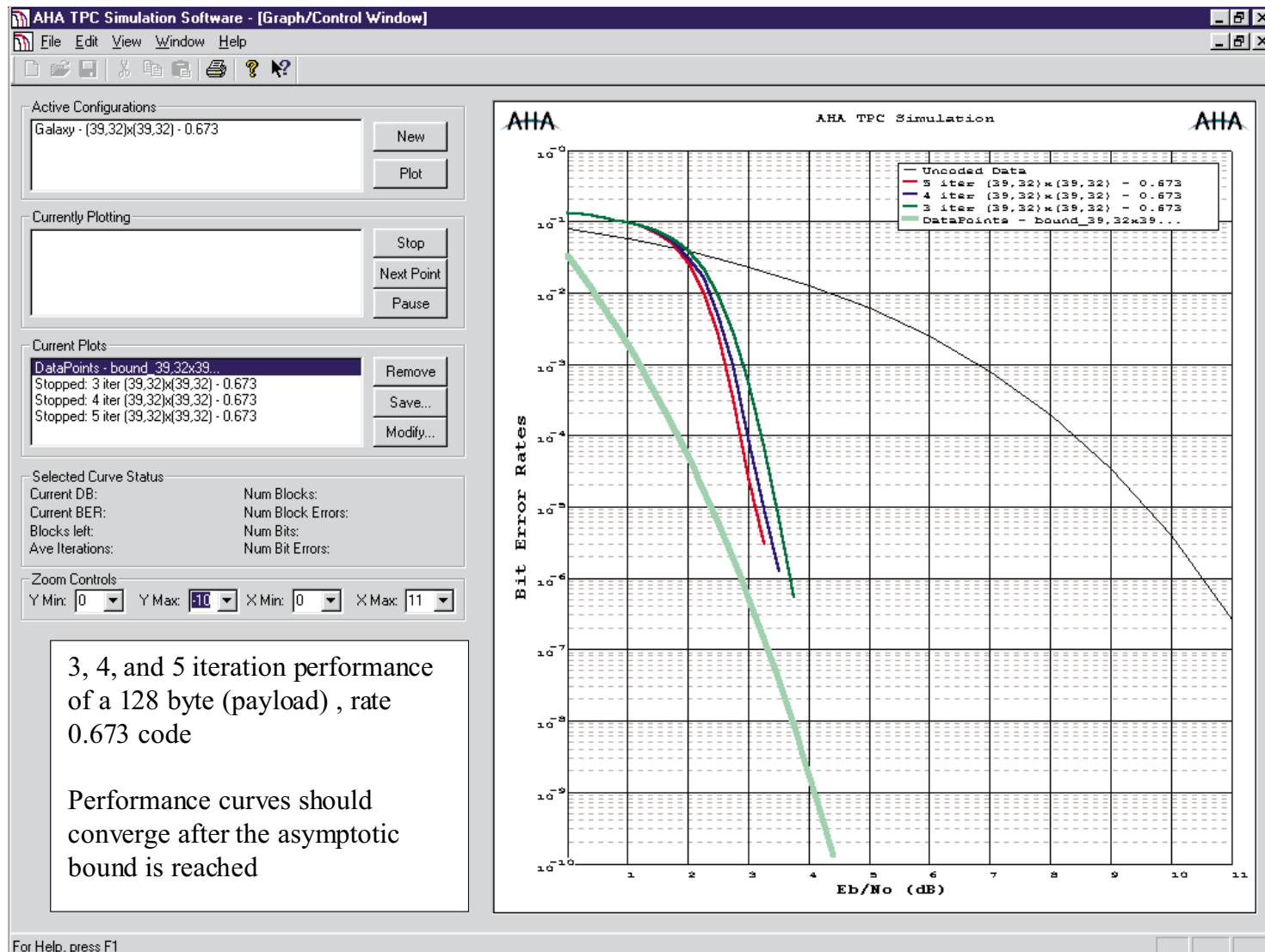
- Large Block can provide significant code rate and coding gain advantages
- Code rates as high as $R = 0.98$ for higher bandwidth efficiency
- Optimal efficiency for continuous downstream transmission
- A single unified decoder design will also support the small block codes but with higher coding gain when the larger blocks are used
- Enhanced burst error performance without interleaving

Large Block Performance

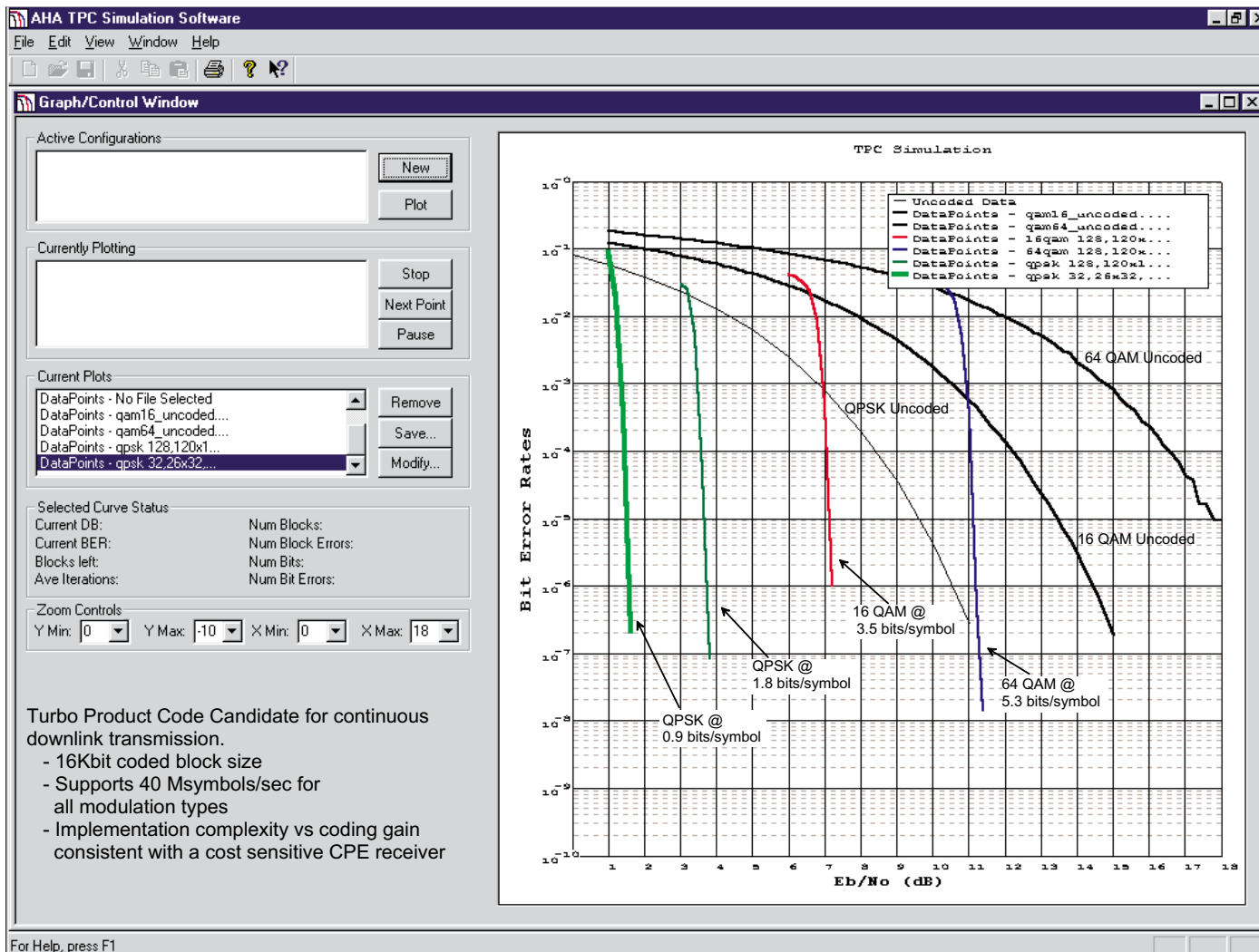
| Code | 32,26 x 32,26 x 16,11 (sb 4) | 128,120 x 128,120 (sb 0) | 128,127 x 128,127 (sb 1) |
|--|---------------------------------|--------------------------------|-----------------------------|
| Aggregate Code Rate | 0.454 | 0.880 | 0.980 |
| Uplink/Downlink/Both | Downlink | Downlink | Downlink |
| Eb/No Required @ 10^{-6} | 1.5 dB | 3.8 dB | 7.5 dB |
| Eb/No Required @ 10^{-9} | 1.8 dB | 4.0 dB | 8.5 dB |
| Encoder Complexity QPSK/16QAM/64QAM | 15 Kgates | 15Kgates | 15 Kgates |
| Decoder Complexity QPSK/16QAM/64QAM | < 250 Kgates | < 250 Kgates | < 250 Kgates |
| Block size (payload bits) | 7,432 | 14,400 | 16,128 |
| Latency | 2 blocks max | 2 blocks max | 2 blocks max |

Notes: The complexity estimates are provided for data rate of 240 Mbit/s. For data rates of up to 150 Mbit/s the complexity will be reduced significantly. Gate counts are estimates which include required RAM (2 bits = 1 gate equiv), 5 iterations and 4 soft input bits to decoder. Dropping iterations to 4 iterations will reduce performance by about 0.1 dB but will also reduce complexity significantly.

Effect of Decoder Iterations on Performance



Representative Large Block Performance



Availability and Time to Market

- BTC hardware is available and fielded for almost 2 years
- Two different BTC evaluation systems are available
- A single chip encoder/decoder that supports channel rates up to 300 Mbits/sec will be available in Q3CY00
 - Supports both small and large block codes
 - Full duplex encoder and decoder
 - Supports QPSK, 16 QAM and 64 QAM needed for 802.16
- BTC cores available for ASIC integration
- VHDL or Verilog targeted to any foundry
- Simulation tools available
 - Includes high order modulation support
 - Includes C/C++ and/or Matlab support
 - Facilitates system level simulations for channel models, phase jitter, burst noise and other impairments

Conclusions

- All coding schemes proposed including traditional RSV and RS+BC provide good performance
- BTCs provide best performance and can offer a very wide range of block sizes and code rates with no change in coding strategy
- BTC codes have multiple vendor availability
- Both off the shelf ICs and ASIC Cores are available