IEEE 802.16.3 PHY Utilizing Turbo Product Codes

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IEEE 802.16.3 PHY Utilizing Turbo Product Codes

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Structure of Presentation

- ¥ Turbo Product Codes
- ¥ Encoding TPC s
- ¥ TPC s Under Single Carrier System
- ¥ TPC s Under Multicarrier System
- ¥ Conclusion

Properties of TPCs

- Turbo Product Codes (TPCs) are very flexible
- Can support any data block size, resolution 1 bit
- TPCs can support a very wide range of code rates with a single, unified encoder/decoder strategy
- From below rate 1/3 to as high as rate 0.98
- Multiple vendor support exists
- Product Codes were described in 1948 by Elias

cont

Properties of TPCs (cont)

- Codes described here are the same type that are included in the 802.16.1 specification
- Data rates are lower, hence decoder is potentially less complex/lower cost than 802.16.1 codes
- Depending on codes chosen, the decoder can be implemented with < 150 Kgates (includes memory)

TPC — Encoding Operation

$$(n,k) = (n_x\text{-}s_x, k_x\text{-}s_x) \times (n_y\text{-}s_y, k_y\text{-}s_y)$$

- ¥ Choose Code Parameter (n,k)
- ¥ Choose Component Codes (n_x, k_x)
- ¥ Shorten Component Codes as Required $(s_x,$

Note on Component Codes

- Component Codes based on extended Hamming Codes (Hamming Code+1 bit parity)

Extended Hamming Code	Hamming Code	Gen Poly
(8,4)	(7,4)	$x^3 + x + 1$
(16,11)	(15,11)	$x^4 + x + 1$
(32,26)	(31,26)	$x^5 + x^2 + 1$
(64,57)	(63,57)	$x^6 + x + 1$
(128,120)	(127,120)	$x^7 + x^3 + 1$
(256,247)	(255,247)	$x^8 + x + 1$

2D TPC Coding Example

TPC Code Required: **(2304,1681)**

¥ Choose Component Codes (use ÷*n*)

¥ Extended Hamming Code **(64,57)**

¥ Shorten Code by 16, to make **(48,41)** code

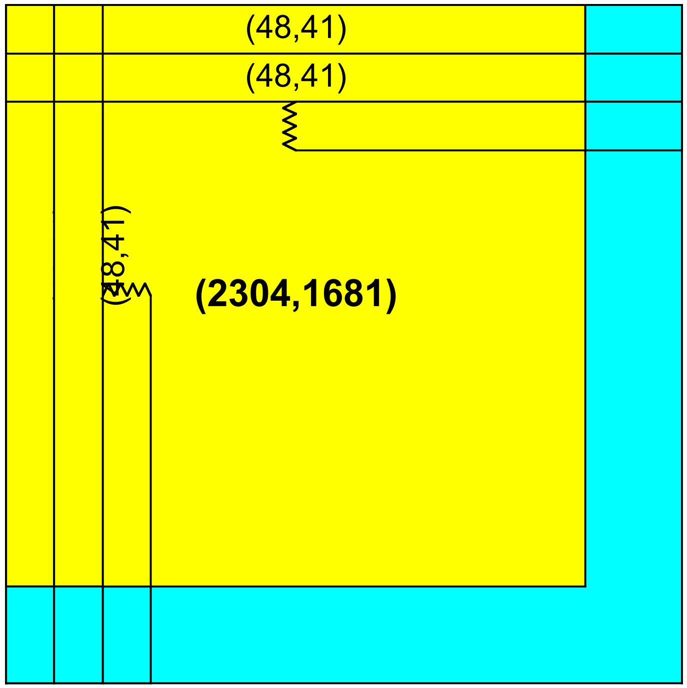
(48,41) x **(48,41)** = **(2304,1681)**

2D Visualization

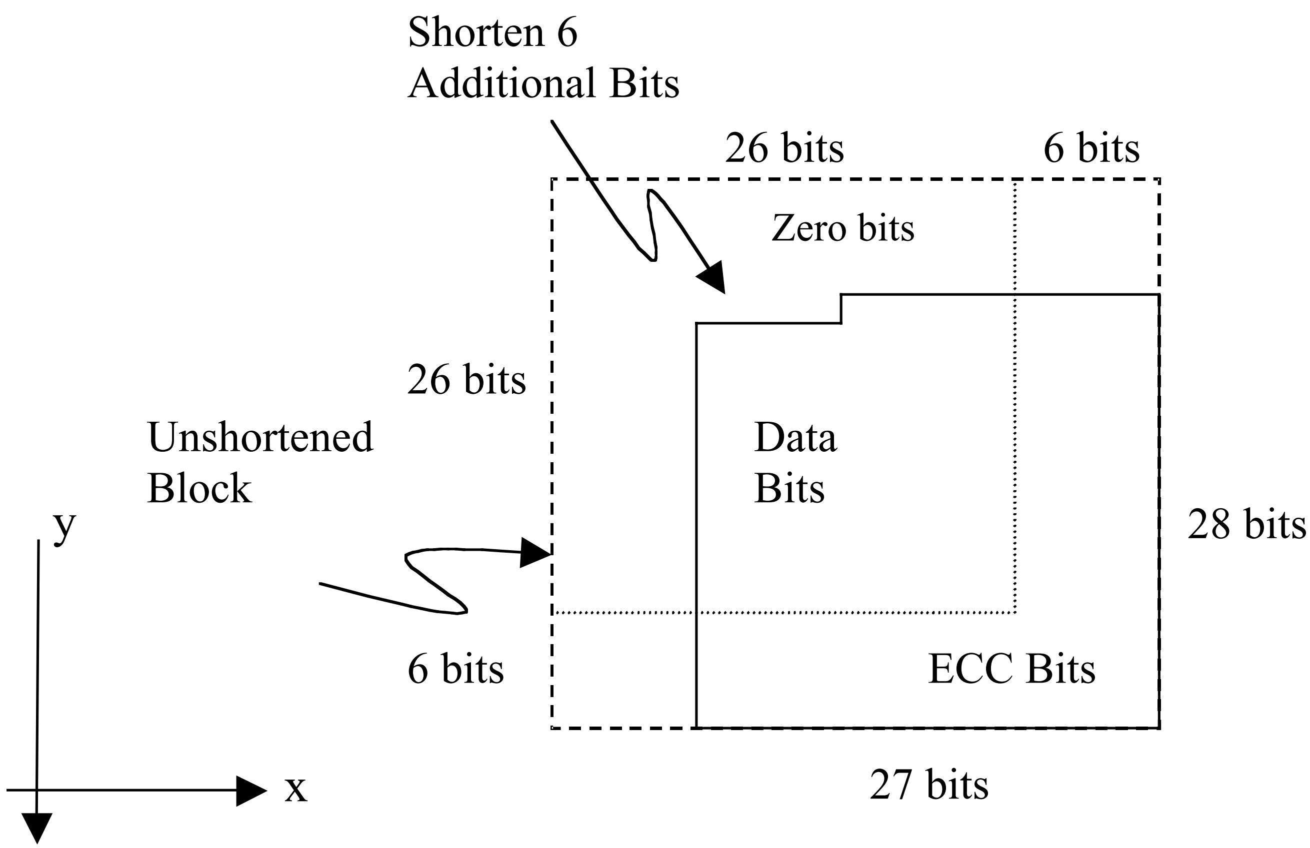
Resultant code is:

(48, 41)x(48, 41) =

(2304, 1681)



Encoding a 2-D TPC

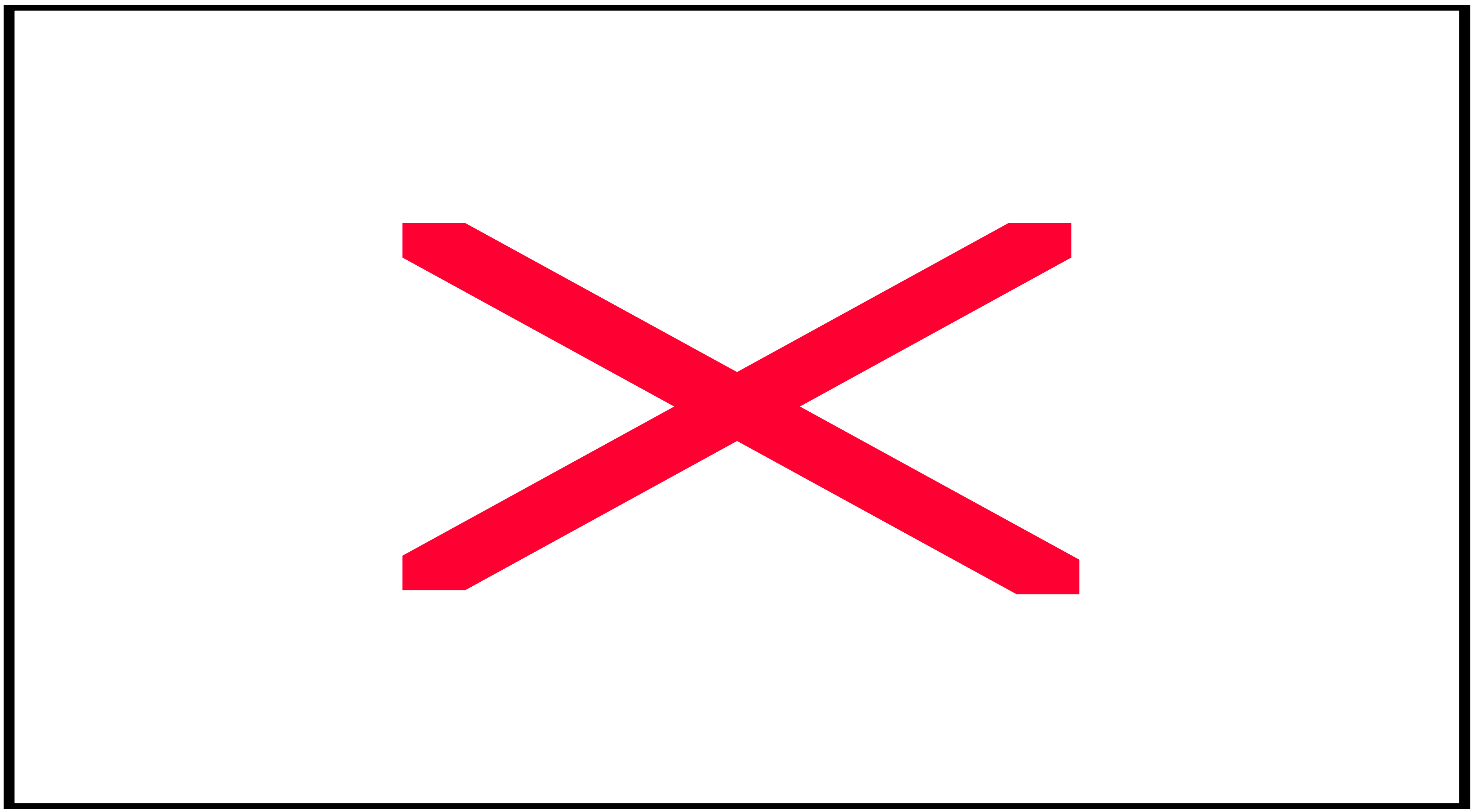


TPC s Under Single Carrier System

- ¥ Typical Single Carrier Framework
- ¥ Integrating TPC s into Single Carrier Systems
- ¥ Performance Enhancements with TPC s

Single Carrier PHY

¥ Comprises of:



Representative TPC s for Single Carrier

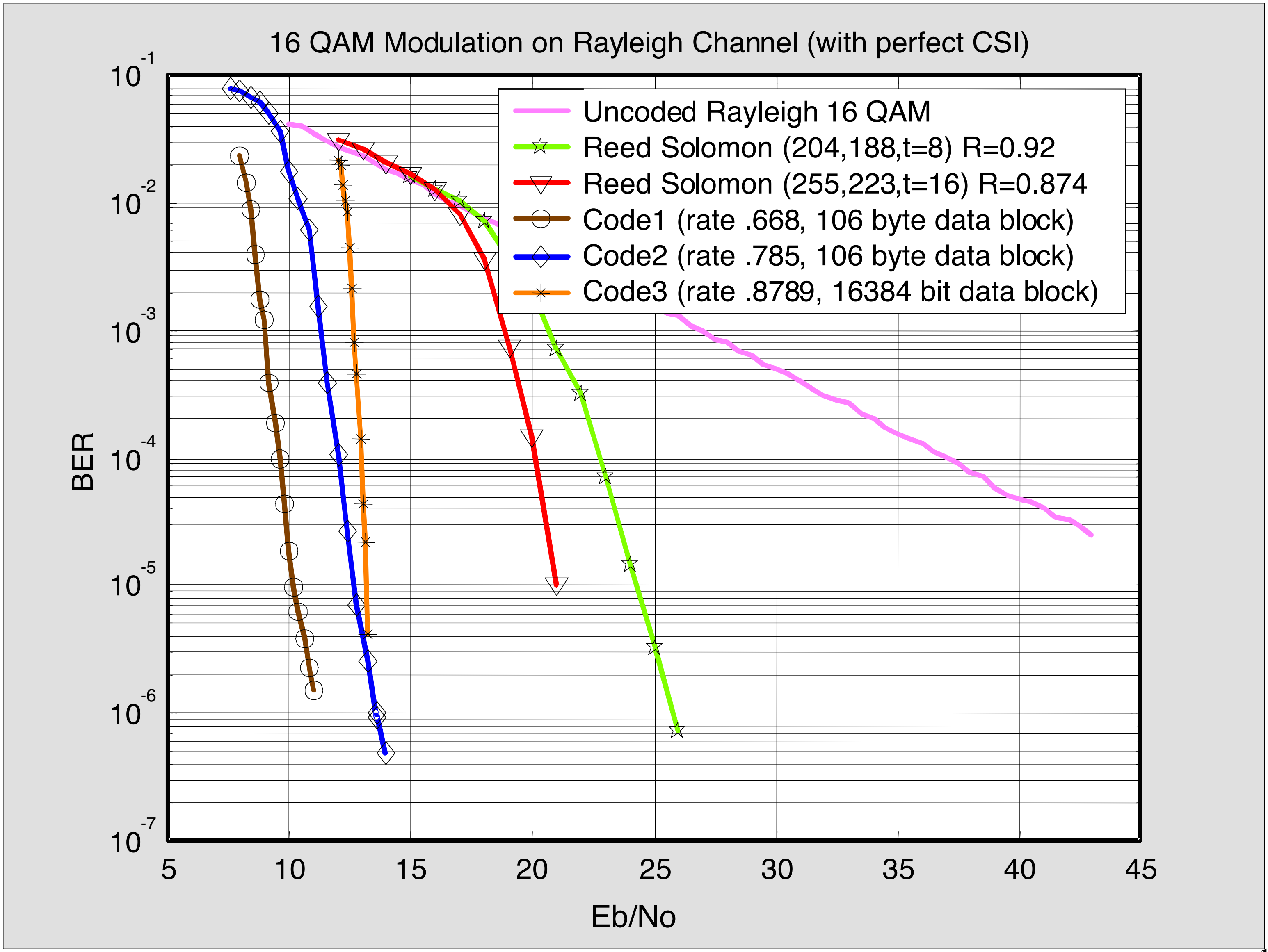
Larger TPCs

Code	$(32,26)^2$x(16,11), QPSK	$(32,26)^2$x(16,11), 16 QAM
Code Rate	0.454	0.454
Eb/No @BER=10^{-6}	1.5	4.7
Eb/No @BER=10^{-9}	1.8	5.1

Shorter TPCs, from TG1 (burst or continuous)

Code	(39,32)x(39,32) s1=s2=25	(46,39)x(46,39) s1=s2=18 s=17
Code Rate	0.673	0.717
Eb/No @BER=10^{-6} (4/16/64 QAM)	3.5/6.5/10.7	3.6/6.6/10.5
Eb/No @BER=10^{-9} (4/16/64 QAM)	4.3/7.5/11.7	4.3/7.8/11.5

16 QAM Performance in a Rayleigh Channel



TPC s Under Multicarrier System

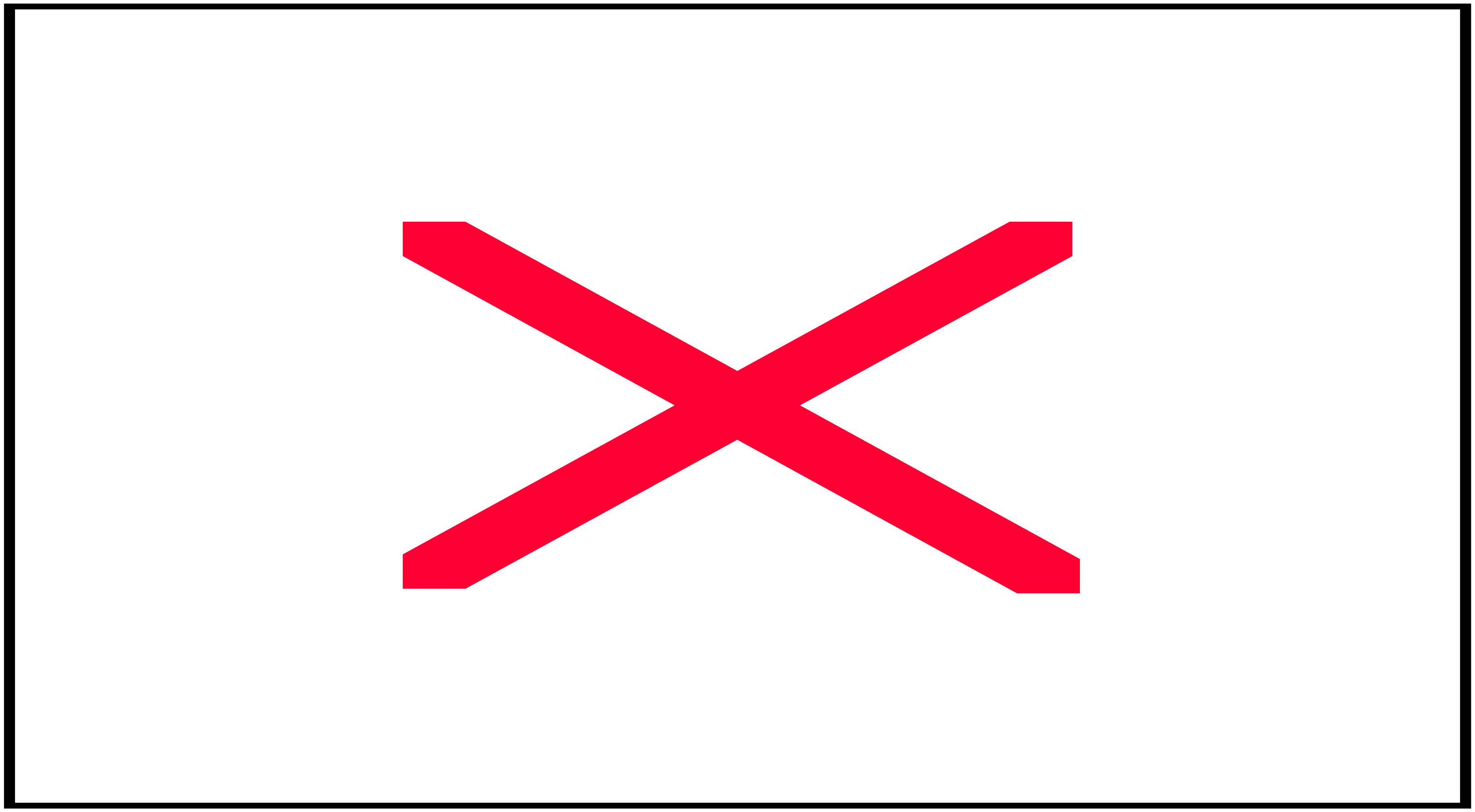
¥ Typical Multicarrier Framework

¥ Integrating TPC s into Multicarrier Systems

¥ Performance Enhancements with TPC s

Multicarrier 64 Point FFT PHY

¥ Comprises of:



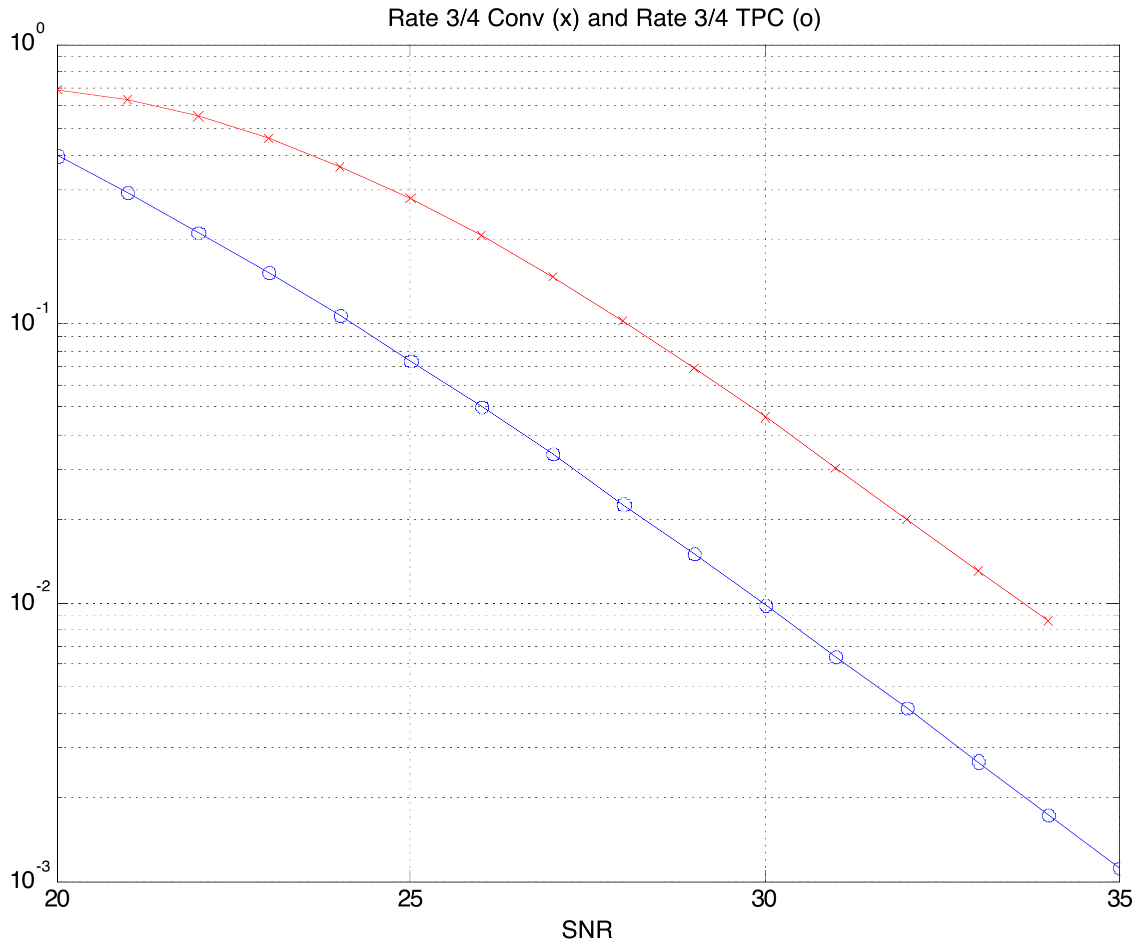
64 Point FFT Structure

¥ Code lengths multiple of 48 bits

¥ Minimum number of TPCs Required

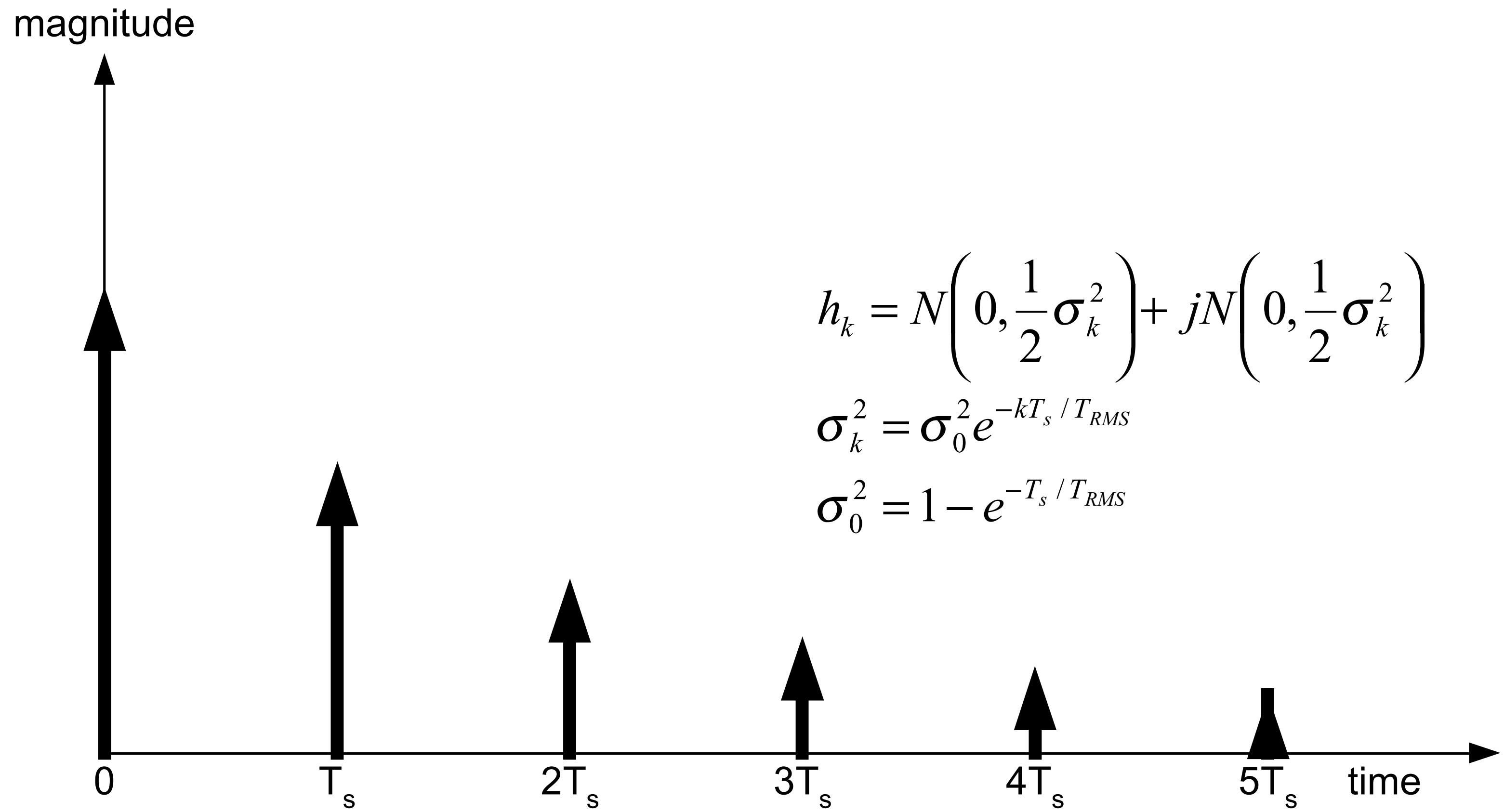
Subcarrier Modulation	**Coding Rate**	**Data Rate /Mbit/s**	**Coded Bits per OFDM symbol**	**Data bits per OFDM symbol**
BPSK	1/2	1.33	48	24
BPSK	3/4	2	48	36
QPSK	1/2	2.66	96	48
QPSK	3/4	4	96	72
16 QAM	1/2	5.33	192	96
16 QAM	3/4	8	192	144
64 QAM	2/3	10.67	288	192
64 QAM	3/4	12	288	216

Multicarrier Performance Under Fading Conditions



Fading Model

Independent fade across packets



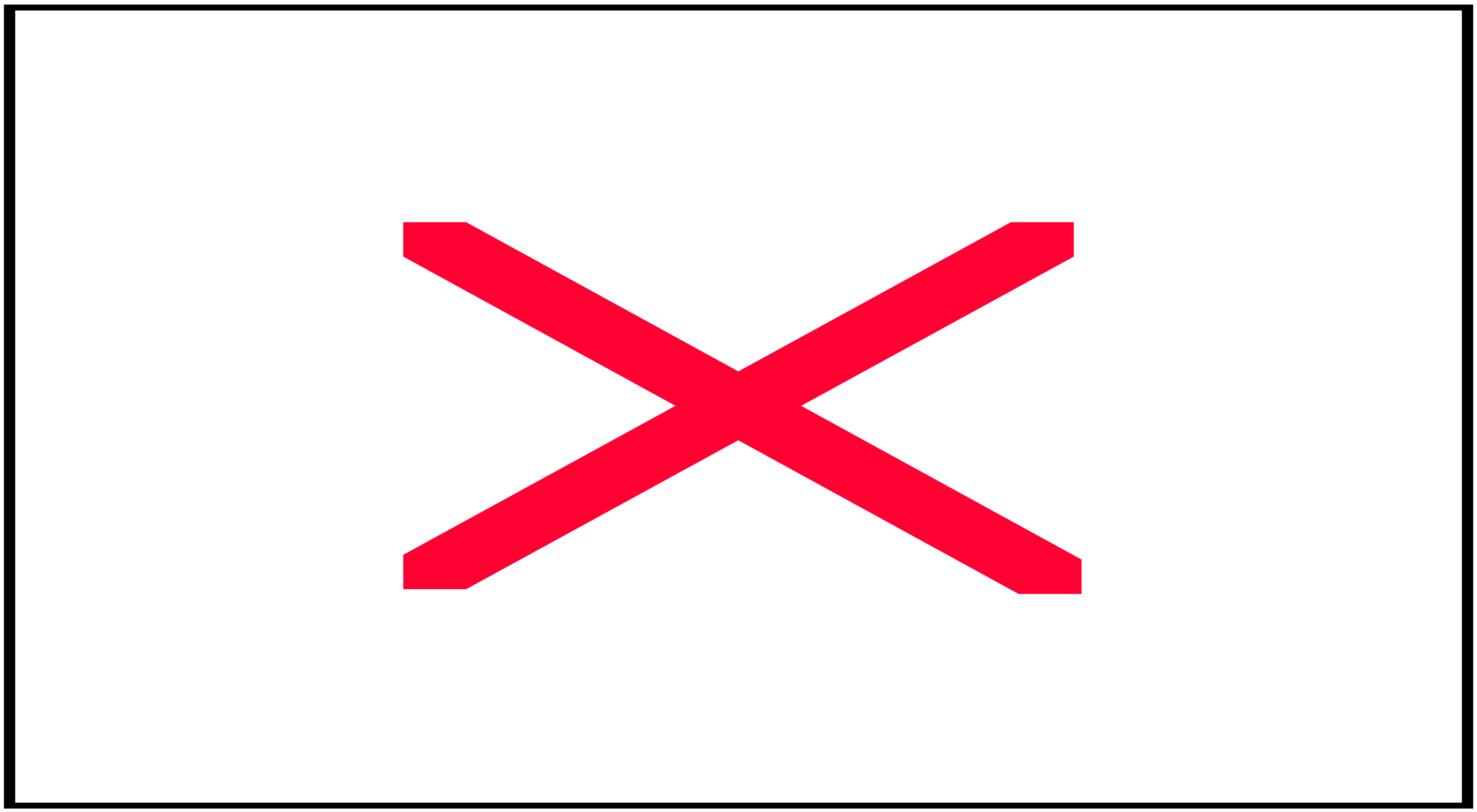
$$h_k = N\left(0, \frac{1}{2}\sigma_k^2\right) + jN\left(0, \frac{1}{2}\sigma_k^2\right)$$

$$\sigma_k^2 = \sigma_0^2 e^{-kT_s/T_{RMS}}$$

$$\sigma_0^2 = 1 - e^{-T_s/T_{RMS}}$$

Enhanced Multicarrier Format

¥ Comprises of:



256 Point FFT Structure

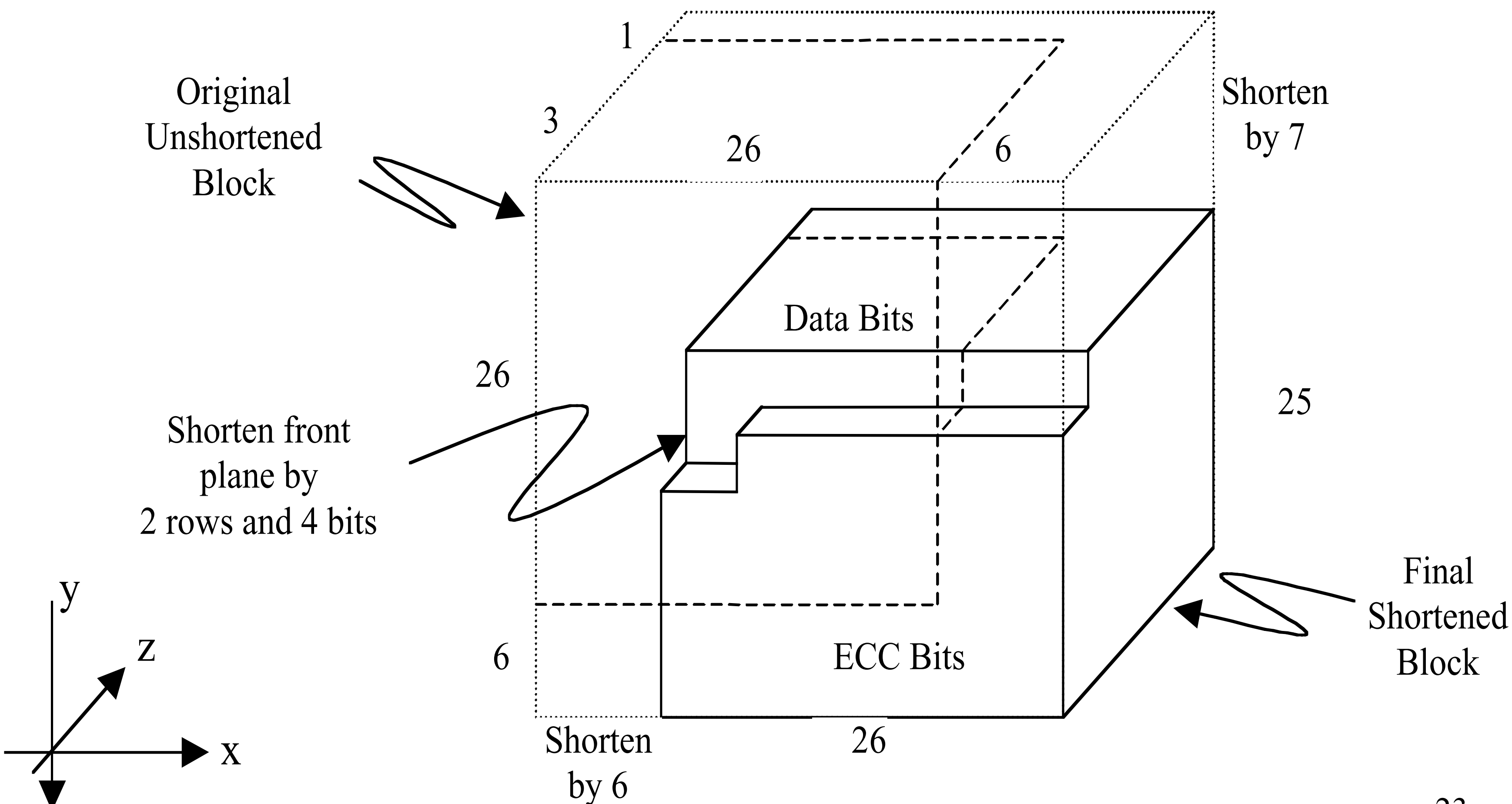
- Code lengths multiple of 96 bits
- Minimum number of TPCs Required

Subcarrier Modulation	Coding Rate	Data Rate /Mbit/s	Code Bits per OFDM symbol	Data bits per OFDM symbol
BPSK	1/2	1.33	192	96
BPSK	3/4	2	192	144
QPSK	1/2	2.66	384	192
QPSK	3/4	4	384	288
16 QAM	1/2	5.33	768	376
16 QAM	3/4	8	768	576
64 QAM	2/3	10.67	1152	768
64 QAM	3/4	12	1152	864

Conclusion

- ¥ TPCs are readily integrated into single carrier of multicarrier frameworks
- ¥ TPCs Provide high performance combined with high spectral efficiency
- ¥ TPCs may be implemented IP free
- ¥ TPCs have been selected TG1
- ¥ Off the shelf chips and cores available
- ¥ TPC technology is consistent with both SS and BS target costs

Example of 3-D TPC



Error Floor vs. Flare

- For TPCs, there is minimal error flare because of high Dmin (typ 16 or greater)
- Depending on the TPC code used:
  - Minor flaring starting @ about 10^{-6} to 10^{-12}
  - Flare is predictable
    - Block size
    - d_{min}