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Title	**SSTTG and SSRTG Requirements for SS HD-FDD Radio Architecture**
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Re:	
Abstract	The contribution identifies a problem and proposes a solution in the OFDM H-FDD SSTTG and SSRTG values contained in P802.16d/D2-2003
Purpose	Error correction
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Radio Architecture Methods for IEEE 802.16a OFDM Radio Transceiver

By Roger Eline, Intel Corporation

Forward

Cost is arguably the key component in the successful deployment of high volume commercial products. This document looks at low cost radio architectures applicable to IEEE 802.16a ñ OFDM. In specific, this document examines the transmit and receive transmission gap, TTG and RTG respectively, required to support a very low cost HD-FDD radio transceiver solution, and proposes a minimum TTG and RTG time.

Background

The IEEE 802.16a standard permits three subscriber station duplex mode profiles for the OFDM PHY.

- FDD
- HD-FDD
- TDD

The implementation cost associated with the different duplex modes range from highest for FDD, to lowest for TDD.

A TDD architecture has the lowest overall complexity which ultimately leads to lowest cost. In a TDD architecture, components can be shared between the transmit and receive channel. This type of architecture has found use in low cost system designs like UMTS-TDD, Bluetooth, and IEEE 802.11a, b, g. The average price of an IEEE 802.11b chipset, this year, is $6, down from $16 of the previous year. It is estimated IEEE 802.11g chipsets will hit an average {price projections deleted by Working Group Chair} , providing an extremely affordable solution to today's hottest selling wireless technology. Technology continually advances to allow such low cost solutions, while meeting the requirements of a higher order modulation, 64 QAM-OFDM. Products built around new Standards, whose key elements benefit from high volume off the shelf components are likely to find instant consumer endorsement because of their low cost entry into the market place.

The similarities between the RF requirements of an 802.11a&g product and those of an 802.16a product for the unlicensed band are noticeable.

- Modulation type: QPSK OFDM, 16-QAM OFDM, 64-QAM OFDM
- Bandwidth: Up to 20MHz
- RX/TX Frequency: Unlicensed band: 2.4-2.485GHz and 5.15 ñ 5.85GHz

It therefore makes sense for developing Standards to allow exploitation of current technology, when available, to better position advanced products for the marketplace.

Figure 1 shows a typical radio architecture for a good performance FDD transmit and receive chain. A baseband Zero-IF IQ data interface is implemented between the baseband modem and the radio.

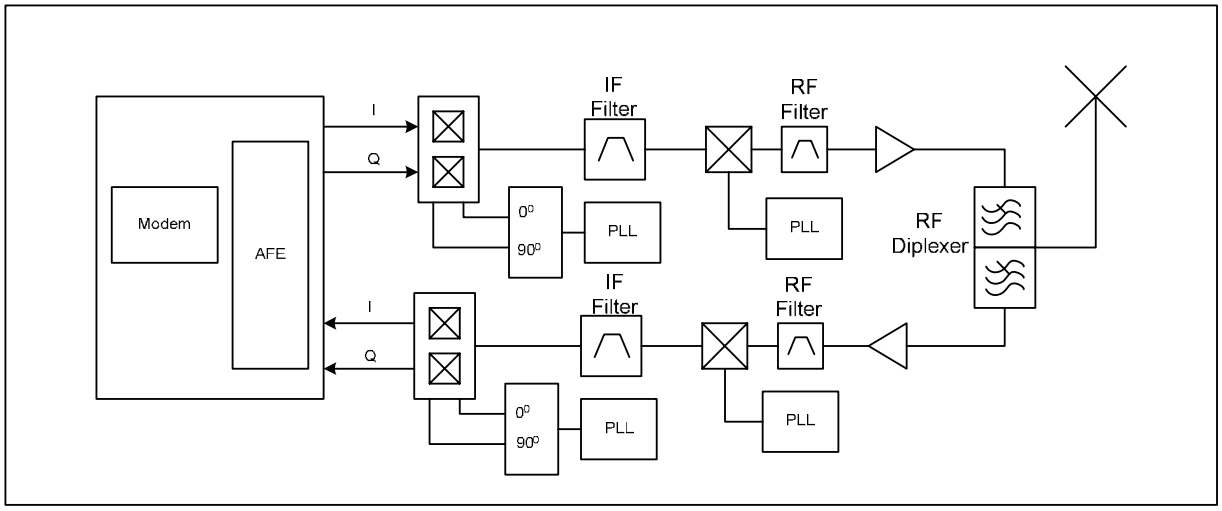

Figure 1. FDD System

The FDD architecture has two independent chains, one for transmit and one for receive. To meet the requirements for transmit and receive isolation a high performance RF Diplexer is required on the front end. Each chain will also require their own IF filter and RF filter, which are major cost items on the radio bill of materials.

Figure 2 shows a typical radio architecture for a good performance HD-FDD transmit and receive chain.

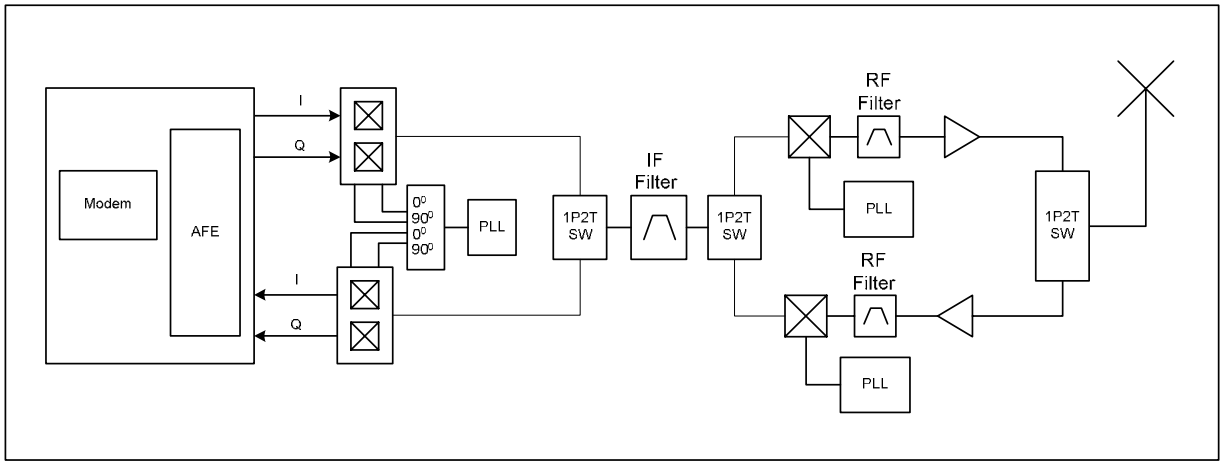

Figure 2. HD-FDD System

The HD-FDD radio in figure 2 is a hybrid design. The backend IF section architecture is similar to the TDD radio shown in figure 3. The frontend RF architecture is similar to the FDD radio shown in figure 1. This radio architecture provides a lower cost implementation when compared to the FDD radio. The HD-FDD radio design allows sharing the IF filter across the transmit and receive chain. Also a single IF RFIC can be used with no regard for transmit to receive isolation.

However, the HD-FDD architecture is not as low cost as the TDD implementation. An HD-FDD system requires unique transmit and receive carrier frequencies and therefore unique local oscillator frequencies. To maintain the isolation between transmit and receive chains, separate frontend RFICs are typically used.

The drawing of Figure 3 is a typical radio architecture for a good performance TDD transmit and receive chain. A baseband Zero-IF IQ data interface is implemented between the baseband modem and the radio.

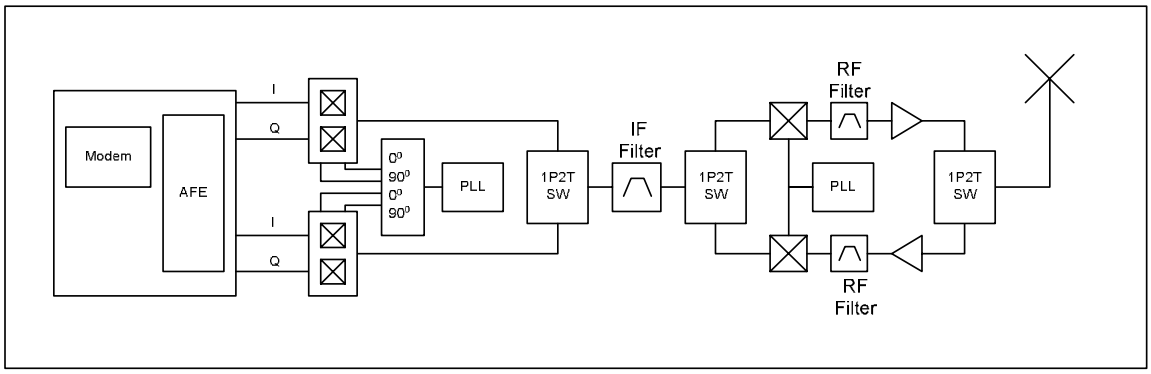

Figure 3. TDD System

The TDD radio architecture represents the lowest cost radio topology of those described in this document. The transmit architecture and receive architecture are decoupled from each other except at the areas where substantial cost savings is realized; they share local oscillators and a common IF filter. Aside from cost savings due to shared components, the time duplex nature of this architecture has minimal isolation requirements between transmit and receive paths. This allows constructing a radio transceiver based on a single chip RFIC.

Comparison of TDD and HD-FDD Topologies

Examining the architectural similarities of the TDD and HD-FDD topologies, one sees the TDD system has a shared RF local oscillator for transmit and receive channels, while the HD-FDD system contains two independent RF local oscillators. It becomes obvious that if the TDD systems RF local oscillator could step and settle fast enough to the required frequencies of the HD-FDD transmit and receive channels, then an RFIC implementing the TDD architecture could operate in an HD-FDD system. To determine the feasibility of using a typically TDD transceiver architecture in an HD-FDD application, it is necessary to analyze the RF local oscillator PLL requirements.

PLL Requirements

To enable the TDD radio architecture, as shown in figure 3, to support the requirements of IEEE 802.16a HD-FDD there are several key requirements placed on the RF PLL local oscillator.

- Fast settling time.
  - Typically settled to better than 100^{th} of the symbol frequency in the defined TTG and RTG period.

        - Typically allowable demodulator frequency error vs. channel bandwidth
            - 55Hz @ BW=1.25MHz
            - 75 Hz @ BW=1.75MHz
            - 150 Hz @ BW=3.5MHz
            - 450 Hz @ BW=10MHz
- Low phase noise, better than 1.2^0 rms or -34dBc
- Relatively small step size:
    - 0.5MHz to 1 MHz

Based on the above criteria a typical PLL design was simulated with the following parameters.

- Minimum Step Size: 500 kHz
- Loop BW: 50 kHz, simulation 1 (Loop BW @ $1/10^{th}$ ref. freq.)
  40 kHz, simulation 2 (Loop BW @ $1/12.5^{th}$ ref. freq.)
- Phase noise: optimized loop BW for min. value
- Frequency Duplex Offset: 100MHZ
- F_{LO} receive: 2.92 GHz
- F_{LO} transmit: 3.02 GHz
- Damping Factor: 0.707
- Loop Type: Type 2, third-order

A transient analysis of the PLL, run with frequency change from 2.92GHz to 3.02GHz, yielded the open loop gain curve of figure 4.

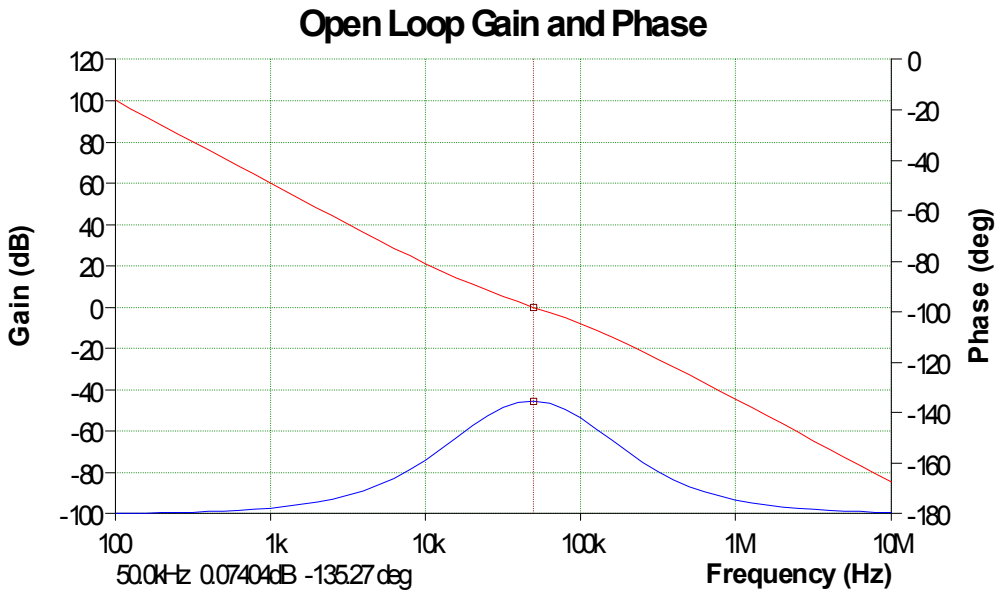

Figure 4

The closed loop settling time response is shown in figures 5 and 6 for a 100MHz step and 50 kHz loop BW. Figures 7 and 8 are the closed loop settling time response for a 100 MHz step and 40 kHz BW. Figures 5, 6, 7, and 8 were used to complete table 1.

Figure 5. Frequency settling time for loop BW of 50 kHz

Figure 6. Phase settling time for loop BW of 50 kHz

Figure 7. Frequency settling time for loop BW of 40 kHz

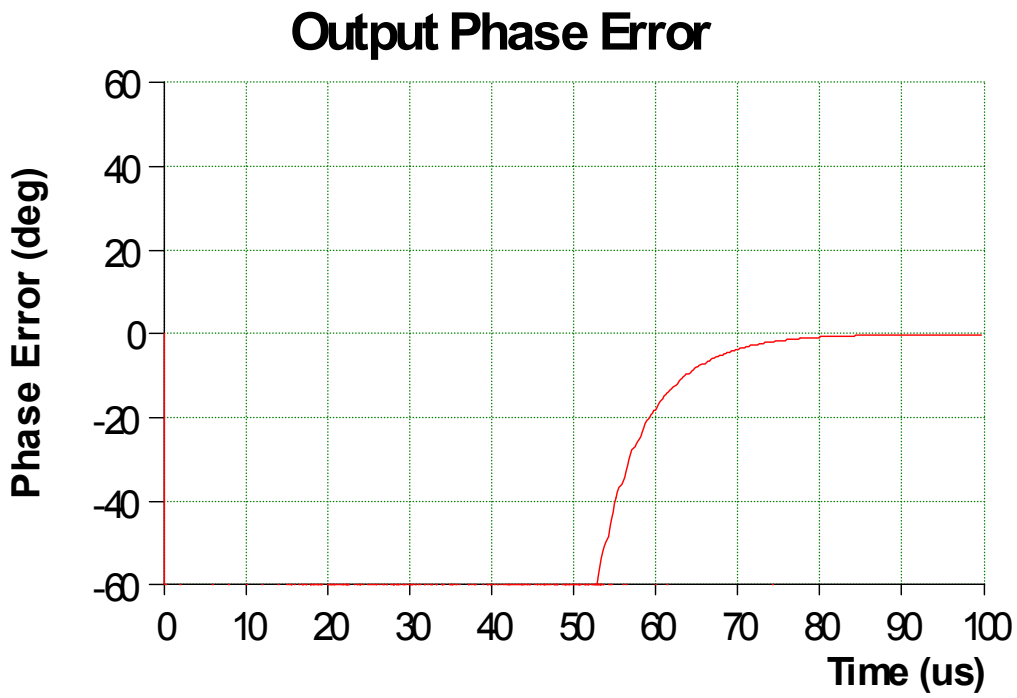

Figure 8. Phase settling time for loop BW of 40 kHz

Table 1 summarizes the results of the PLL requirements and PLL simulations to meet the frequency step and settling requirements of an HD-FDD IEEE 802.16a ñOFDM low cost radio implemented in a TDD radio architecture.

Table 1

Channel BW	Maximum allowable Demodulator Frequency error	PLL Settling time required (Fstep=100MHz) (Figure 5)		Phase Error at Max allowable Demodulator Frequency error (Figure 6)
		Loop BW=40KHz	Loop BW=50KHz	
1.25 MHz	55 Hz	92 uSec	75 uSec	0.085 degrees
1.75 MHz	75 Hz	90 uSec	75 uSec	0.085 degrees
3.5 MHz	150 Hz	86 uSec	71 uSec	0.18 degrees
10 MHz	450 Hz	80 uSec	65 uSec	0.6 degrees

Conclusion

Aside from the obvious technical requirements, a very important part of all product developments is the product cost of goods. From the radio transceiver architectures discussed in this document, the TDD duplex approach is the lowest cost architecture. By correctly specifying RTG and TTG times, the TDD radio architecture can provide a low cost HD-FDD radio solution.

A cost effective IEEE 802.16a HD-FDD radio transceiver can be implemented using a TDD radio transceiver architecture designed for IEEE 802.11. SSTTG and SSRTG times in the order of 90 uSec are required. This will allow the phase-locked loop just enough time to accurately frequency settle, while stepping the RF synthesizer between the transmit and receive offset frequency. Due to manufacturing tolerances of components a recommended SSTTG and SSRTG time of 100uSec is suggested.