Project	**IEEE 802.16 Broadband Wireless Access Working Group** <http://ieee802.org/16>
Title	**Proposed 802.16m Frame Structure**
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Source(s)	Jaeweon Cho, Hokyu Choi, Jaehee Cho, DS Park, Heewon Kang, Yungsoo Kim Samsung Electronics Co., Ltd. 416 Maetan-3, Suwon, 442-600, Korea Voice: +82-31-279-5796 E-mail: jaeweon.cho@samsung.com Rakesh Taori Samsung Advanced Institute of Technology Thierry Lestable, Alain Mourad, Ming Jiang Samsung Electronics Research Institute, UK
Re:	IEEE 802.16m-07/047, "Call for Contributions on Project 802.16m System Description Document (SDD)". Target topic: "Proposed 802.16m Frame Structure with special attention to legacy support".
Abstract	The contribution proposes the frame structure to be included in the 802.16m System Description Document (SDD).
Purpose	To be discussed and adopted by TGm for the 802.16m SDD.
Notice	
Release	
Patent Policy	

Proposed 802.16m Frame Structure

Jaeweon Cho, Hokyu Choi, Jaehee Cho, …
Samsung Electronics Co., Ltd.

Rakesh Taori
Samsung Advanced Institute of Technology

Thierry Lestable, Alain Mourad, Ming Jiang
Samsung Electronics Research Institute, UK

1 Introduction

The contribution proposes the frame structure to be included in the 802.16m System Description Document (SDD).

2 Design Considerations

According to P802.16m System Requirement document (SRD) [1], the 802.16m frame should be able to operate in different modes and scenarios, provide a high system throughput, incur low transmission latency, as well as fully support legacy MSs.

With the above design requirements taken into account, in this contribution a unified frame structure is proposed, which is capable of:

- Operating in various modes and scenarios, e.g. FDD, H-FDD, TDD, and legacy support modes.
- Providing a high throughout (low system overhead) by adopting the super-frame concept, whilst maintaining low data latency by introducing the mini-frame concept. This meets or exceeds the requirements specified in P802.16m SRD.
- Fully supporting backward compatibility. This is achieved without compromising the performance of legacy systems, and provides efficient legacy turn-off feature for supporting green field deployment. It also maximizes the commonality between 16m/legacy-mixed and 16m-only deployment scenarios from the 16m design perspectives.

3 Proposed Frame Structure

3.1 Generic frame structure

The generic frame structure is illustrated in Figure 1. More specifically, a super-frame of 20ms duration is constituted by four frames, each having a duration of 5ms. Each frame consists of eight mini-frames, whilst each mini-frame is further divided by a number of OFDMA symbols (the default value is 6, for 1/8 cyclic prefix

(CP) length). A mini-frame is either dedicated to downlink or uplink. The header of each super-frame is accommodated in the first mini-frame of every super-frame.

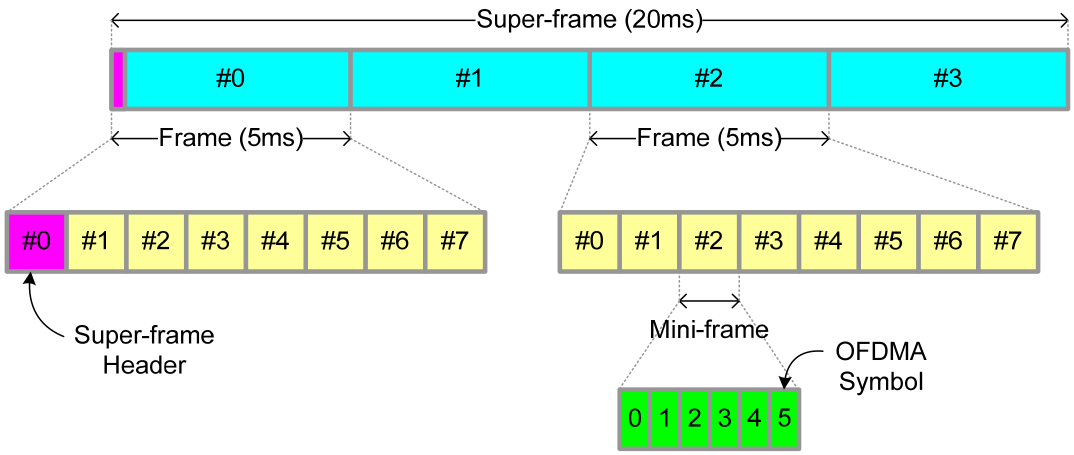


Figure 1: Generic frame structure

3.2 Super-frame Header

A super-frame header is a set of dedicated physical subchannels used for broadcasting slowly varying system information. As there is only one header for each super-frame, the overhead is effectively reduced and the network entry procedure is greatly simplified. Since the information in the header is transmitted through dedicated physical subchannels, no further resource assignment is needed and thus increases handling efficiency.

Super-frame header occupies the first mini-frame of every super-frame. It includes Synchronization Channel (SCH) and Broadcasting Channel (BCH). SCH is mainly used for synchronization, acquisition, BS identification, etc. BCH mainly delivers information related to receiver configuration (e.g. DL/UL ratio, mini-frame parameters…), network configuration (e.g. BS loading, self-organization…), 16m/legacy-mixed mode ratio, and so on.

3.3 Mini-Frame Approaches

The data transmission is on a mini-frame basis. The data burst is allocated to a portion of DL/UL subframe (i.e. one or a few mini-frames). This enables the fast HARQ operation within the 5ms frame.

Depending on the requirement, several Transmission Time Interval (TTI) options can be used:

- Default option (for low latency): TTI is set to be one mini-frame, as seen in Figure 2(a).

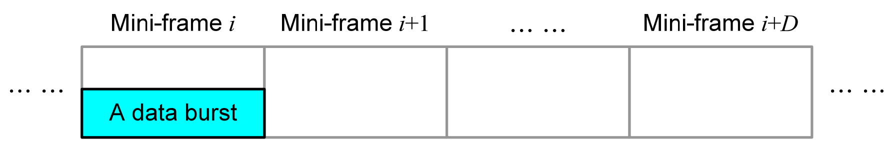


Figure 2(a): Sinlge mini-frame transmission

- Additional options: TTI is set to be multiple consecutive mini-frames.
  - For a large FEC packet, as seen in Figure 2(b).

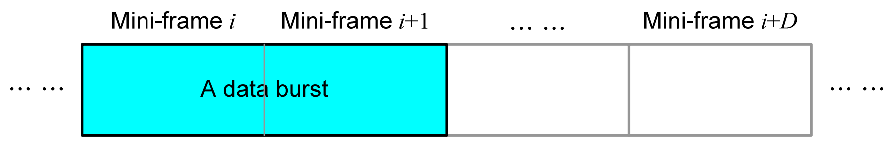


Figure 2(b): Muliple mini-frame transmission (2 mini-frames)

  - For a better link budget, as seen in Figure 2(c).

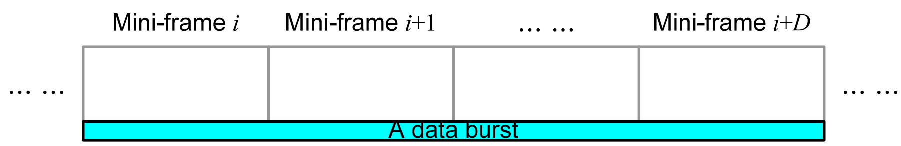


Figure 2(c) : Multiple mini-frame transmission (D+1 mini-frames)

4 Rationale for the proposal

The design of the frame structure has been based on the following considerations.

4.1 Flexible operations for FDD, H-FDD, TDD modes

A unified frame structure is necessary for a flexible system which P802.16m aims at. The proposed generic frame structure is applicable to various duplex modes such as FDD, H-FDD, and TDD, while keeping maximizing the commonality.

Frame configuration for the FDD mode is shown in Figure 3.

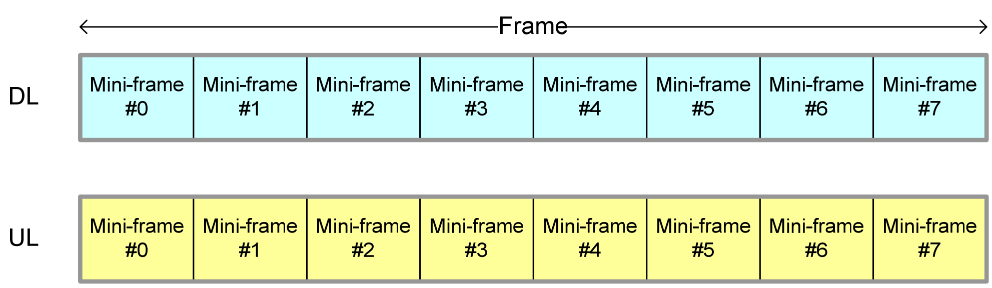


Figure 3: FDD frame configuration

The FDD frame configuration based on the proposed generic frame structure enables co-operation of the FDD and the H-FDD modes in the same frame. Figure 4 shows frame configuration for the H-FDD MS. From the BS' perspective, the same frame structure as in the FDD mode can be exploited, while from the MS' perspective, a half set of collected HARQ interlaces is used. Therefore, the BS can support the FDD MS and the H-FDD MS in a frame.

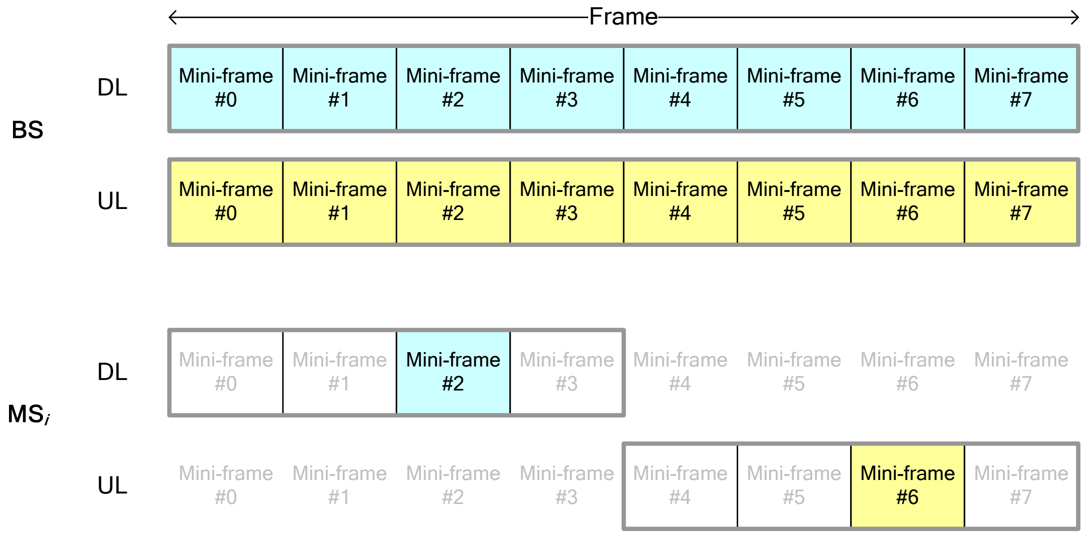


Figure 4: H-FDD frame configuration

For the TDD mode, the proposed frame structure enables various and flexible partitions of DL and UL subframes in units of mini-frames. The ratio of DL mini-frames to UL mini-frames should be one of 8:0, 6:2, 5:3 or 4:4. Note that the DL:UL ratio of 8:0 is applicable to E-MBS delivery via a dedicated carrier. Figure 5 shows those four DL/UL partitions in TDD frame configuration.

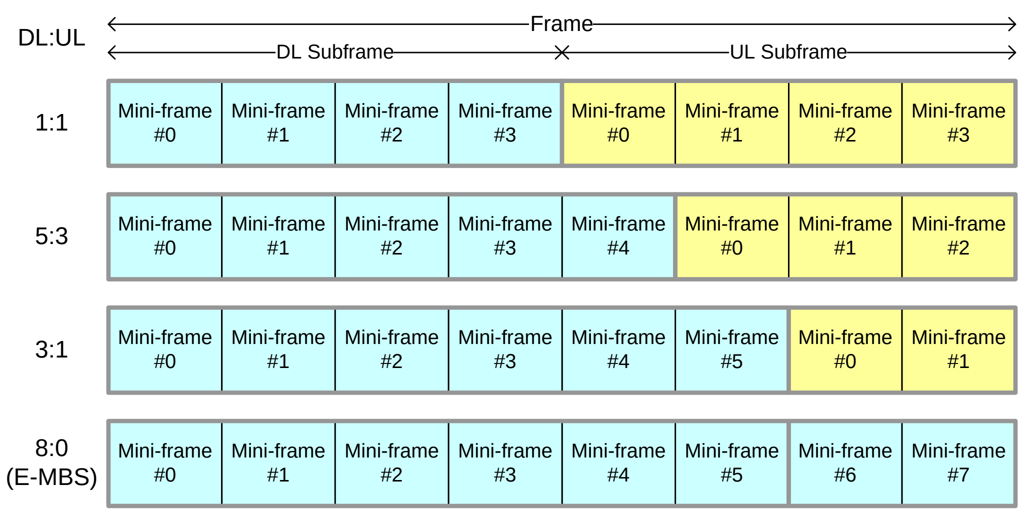


Figure 5: TDD frame configuration

4.2 Efficient legacy support

The proposed generic frame structure efficiently supports legacy MSs while satisfying the backward compatibility requirements specified in P802.16m SRD (i.e. subclause 5.1) [1]. In particular, the proposed configuration enable to support a legacy MS while also supporting new MSs on the same RF carrier, at a level of performance equivalent to that a legacy BS provides to a legacy MS.

In addition, by allowing various partitions of 16m and legacy, a smooth migration from legacy only operation to 16m only operation is provided. The legacy support frame configurations with the various partitions of 16m and legacy are shown in Figure 6.

In the frame configuration in Figure 6, a subset of DL mini-frames is dedicated to the legacy operation to enable one ore more DL legacy time zones. The subset includes the 1st DL mini-frame to support the transmission of the legacy preamble, FCH, and MAP. In UL subframe, a group of subcarriers (subchannels), spanning the entire UL subframe, are dedicated to the legacy operation. The remaining subcarriers, forming the new UL subframe, are dedicated to the new operation. In the new UL subframe, mini-frames are defined and all the mini-frames are used for the new operation. For more detailed explanation of frame configuration for legacy support, see contribution [2].

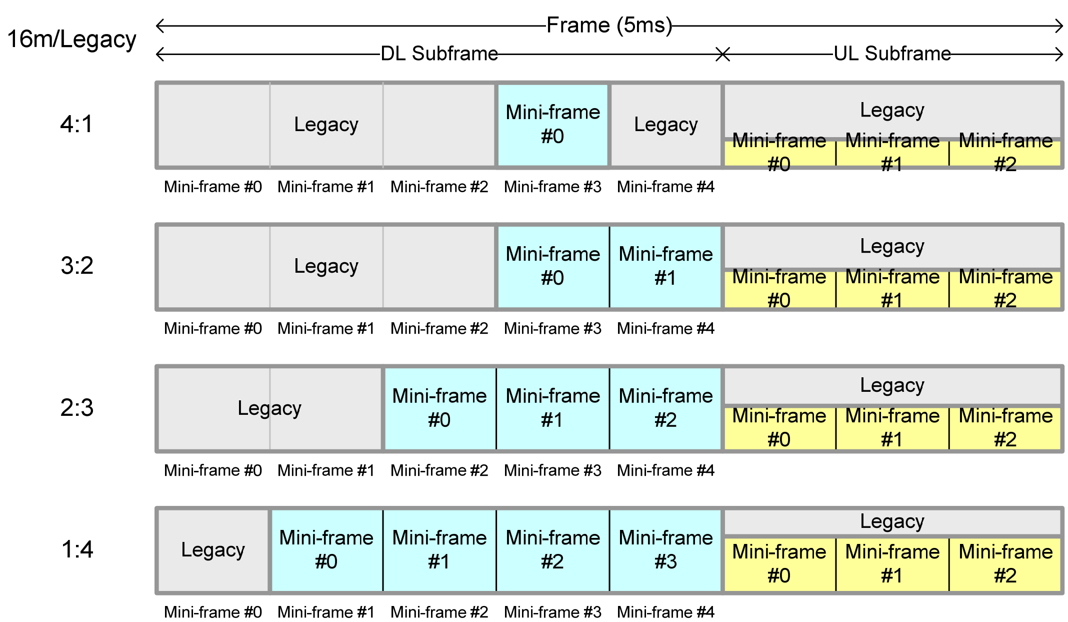


Figure 6: Frame configuration for legacy support (DL:UL = 29:18)

4.3 Low data latency

The data latency in P802.16m SRD [1] is defined in terms of the one-way transit time between a packet being available at the IP layer (Tx reference point) in either the MS/Radio Access Network and the availability of this packet at IP layer (Rx reference point) in the Radio Access Network/MS. This is illustrated in Figure 7

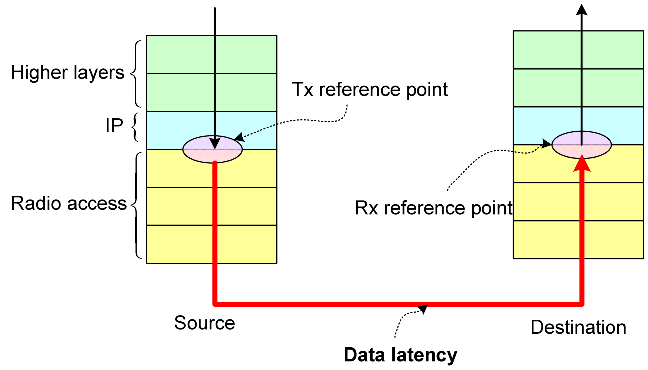


Figure 7. HARQ operation in a frame

In P802.16m SRD, the data latency requirement is specified to be less than 10 ms. In our proposal, various ways can be envisaged to lower down the latency and make it fulfill the 10 ms requirement. A first way consists in shortening the Transmission Time Interval (TTI) to one or few mini-frames. For delay-sensitive data, a short TTI is set to one mini-frame.

A second way consists in speeding up the HARQ operation within 5ms frame. This can be done by associating a data transmission and HARQ feedback in the same frame. Note that the two mini-frames containing respectively the data transmission and the associated feedback, are apart enough to ensure both Rx processing time and retransmission Tx processing time. The example of HARQ operation within a frame for TDD 5:3 mode is shown in Figure 8.

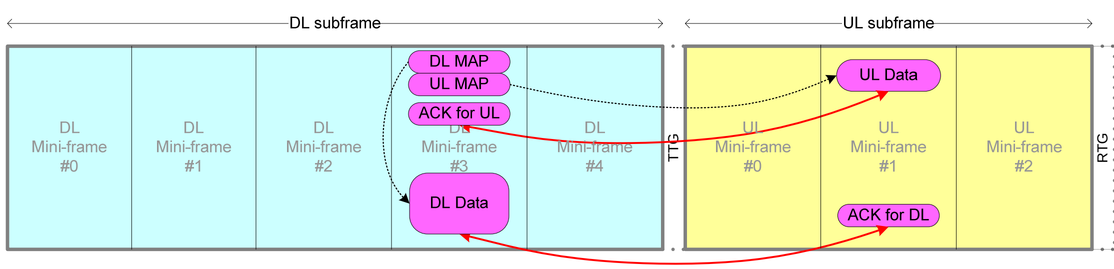


Figure 8. Example of HARQ operation in a TDD frame.

On the basis of the two approaches described above, synchronous HARQ interlace structure ensuring low data latency is developed in both FDD and TDD modes and in both DL and UL directions.

For the FDD mode, an eight interlace structure is used for each DL and UL. Figure 9 and 10 illustrate transmissions timing associated with one of interlace in DL and UL, respectively. The timing of the other interlaces is the same but with data burst and feedback transmissions shifted by the same number of mini-frames. The DL and the UL interlace structures are the same except that MAP in the DL interlace is transmitted with data burst.

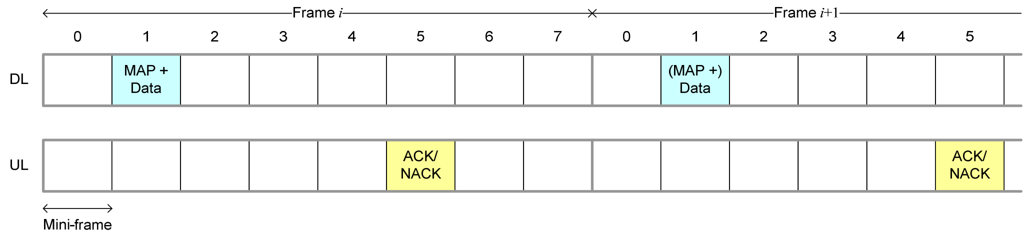


Figure 9. FDD DL HARQ interlace.

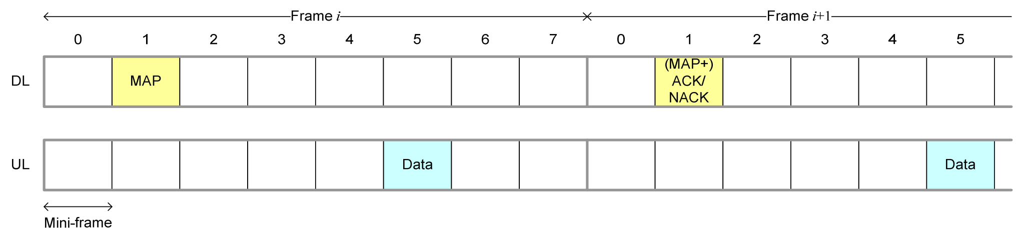


Figure 10. FDD UL HARQ interlace.

The corresponding structured transmission timings of data burst and HARQ feedback in DL and UL are given in Table 1 and 2, respectively. Frame index i and min-frame index m in the two tables take the values i = 0~3 and m = 0~7, respectively.

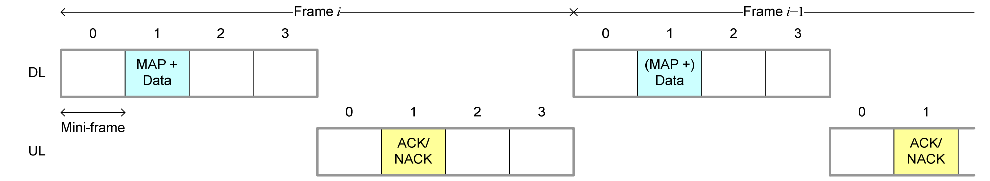
Table 1. Transmission timing of data and feedback in FDD DL.

Type	Direction	Frame index	Mini-frame index
MAP + Data Tx	DL	i	m
ACK Tx	UL	(i + floor((m+4)/8)) mod 4	(m+4) mod 8
Data ReTx	DL	(i + 1) mod 4	m

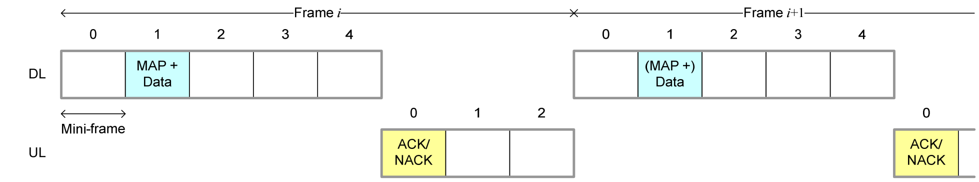
Table 2. Transmission timing of data and feedback in FDD UL.

Type	Direction	Frame index	Mini-frame index
MAP	DL	i	m
Data	UL	(i + floor((m+4)/8)) mod 4	(m+4) mod 8
ACK Tx	DL	(i + 1) mod 4	m
Data ReTx	UL	(i + 1 + floor((m+4)/8)) mod 4	(m+4) mod 8

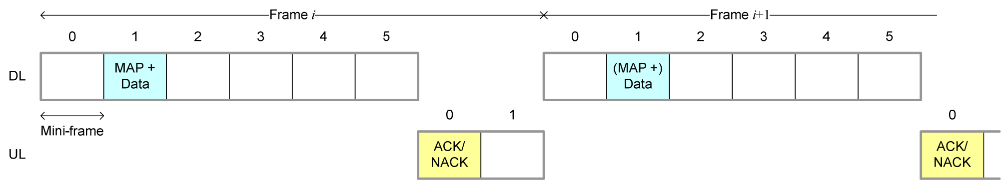
For the TDD mode, an eight interlace structure is divided into DL and UL interlaces according to the ratio of DL and UL. Figure 11 and 12 illustrate transmissions timing associated with one of interlace in DL and UL, respectively. The DL and the UL interlace structures are the same except that MAP in the DL interlace is transmitted with data burst. It is found in Figure 9, 10, 11, and 12 that the TDD interlace structure is very similar to the FDD interlace, in particular for TDD 1:1 mode.



(a) D:U = 4:4

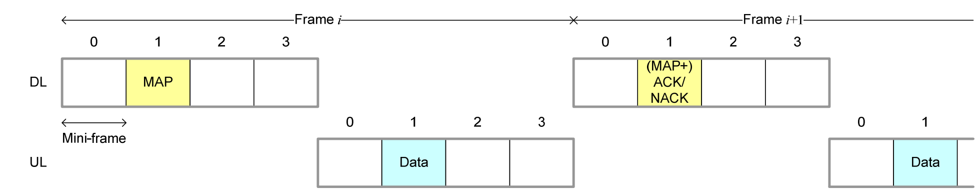


(b) D:U = 5:3

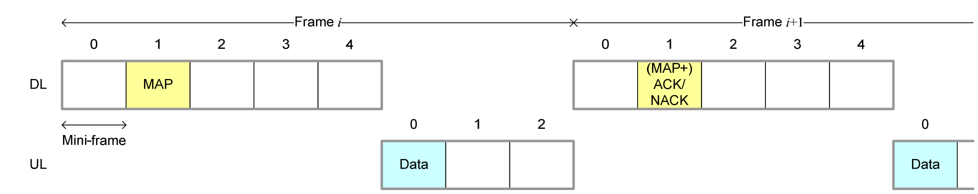


(c) D:U = 6:2

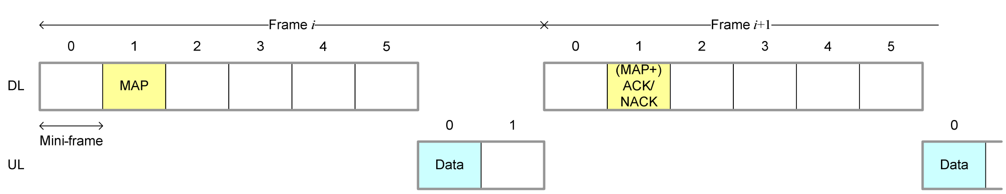
Figure 11. TDD DL HARQ interlace.



(a) D:U = 4:4



(b) D:U = 5:3



(c) D:U = 6:2

Figure 12. TDD UL HARQ interlace.

The corresponding structured transmission timings of data burst and HARQ feedback in DL and UL are given in Table 3 and 4, respectively. Frame index i in the two tables take the values i = 0~3. Mini-frame index m does m = 0~D-1 (for the DL interlace) or 0~U-1 (for the UL interlace), where D and U is the numbers of DL mini-frames and UL mini-frames, respectively. The parameter K is given by = D/U, so the equations provided in the two tables are applicable to all three DL/UL partitions of 4:4, 5:3, and 6:2.

For the TDD 6:2 mode, a slow interlace such that re-transmission timing is extended to the frame after the next, may be applied to data transmission in DL mini-frame #0 or #5, for the case when an enough time for Rx/Tx processing cannot be secured. The slow interlace may be also applied to UL data transmission assigned by MAP in DL mini-frame #0 or #5.

Table 3. Transmission timing of data and feedback in TDD DL.

Type	Direction	Frame index	Mini-frame index
MAP + Data Tx	DL	i	m
ACK Tx	UL	i	floor(m/K)
Data ReTx	DL	(i + 1) mod 4	m

Table 4. Transmission timing of data and feedback in TDD UL.

Type	Direction	Frame index	Mini-frame index
MAP	DL	i	m
Data Tx	UL	i	floor(m/K)
ACK Tx	DL	(i + 1) mod 4	m
Data ReTx	UL	(i + 1) mod 4	floor(m/K)

Now, data latency performance of the proposed frame structure with the HARQ interlace is to be provided.

The calculation of data latency is done according to U-plan latency concept employed in [2]:

Data latency = Initial Tx delay + Pr(ReTx) x HARQ ReTx delay

In above equation, ReTx refers to an HARQ retransmission and Pr(ReTx) is the probability of the initial transmission error rate. Note that the data latency can be represented by a function of the TTI.

In FDD DL, the calculation of data latency is illustrated in Figure 12 below and results are summarized in Table 5 hereafter. In the calculation, it is assumed that Tx/Rx processing time is approximately 2 mini-frames (2 TTIs) and Pr(ReTx) is 30%.

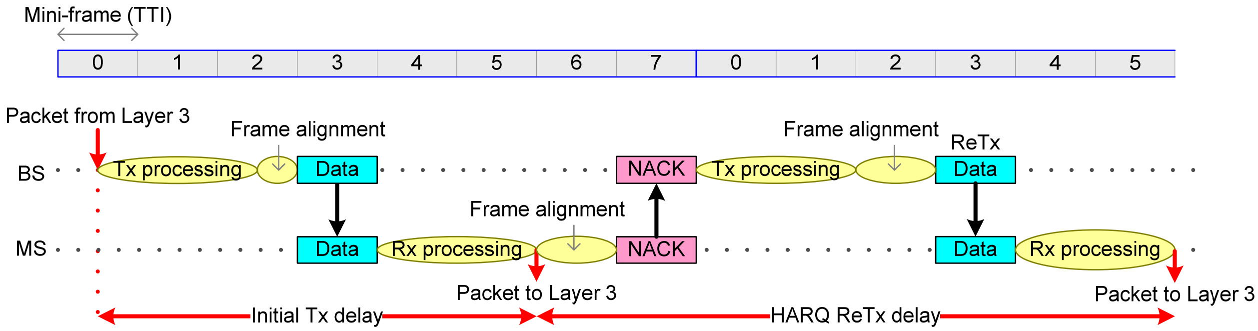


Figure 13. Transmission Data latency in FDD DL.

Table 5. Data latency calculation in FDD DL.

Delay type		Value
Initial Tx Delay	Tx Processing Delay	2 TTI
	Frame Alignment Delay	0.5 TTI
	Transmission Interval	1 TTI
	Rx Processing Delay	2 TTI
HARQ ReTX Delay		8 TTI
Data Latency with TTI = 0.617ms, Pr(ReTX) = 30%		5.5 TTI + Pr(ReTx) x 8 TTI = 4.87ms

The calculation procedure and results for TDD 5:3 DL are given in Figure 13 and Table 6 below. In this analysis, an interlace in which a packet arrives in DL mini-frame #0 and it is transmitted at DL mini-frame #3, is considered.

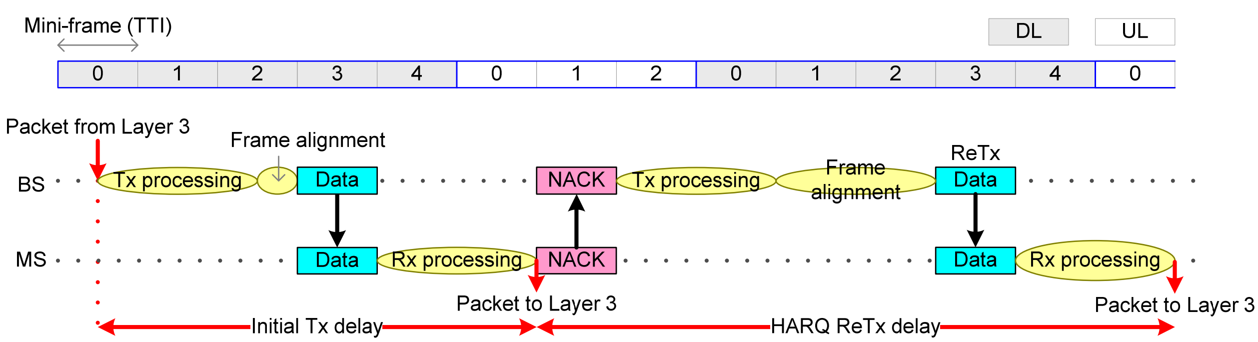


Figure 14. Transmission Data latency in TDD DL.

Table 6. Data latency calculation in TDD DL.

Delay type		Value
Initial Tx Delay	Tx Processing Delay	2 TTI
	Frame Alignment Delay	0.5 TTI
	Transmission Interval	1 TTI
	Rx Processing Delay	2 TTI
HARQ ReTX Delay		8 TTI
Data Latency with TTI = 0.617ms, Pr(ReTX) = 30%		5.5 TTI + Pr(ReTx) x 8 TTI = 4.87ms

The overall latency performance of our proposal is summarized in Table 7 below for FDD and TDD in both DL and UL directions. In the analysis, it is assumed that layer 3 packets arrive uniformly over 5ms frame, and the probability of the initial transmission error rate is equal to 30%. For UL data transmission, pre-scheduling such as UGS service is assumed. In case of TDD 6:2, the slow interlace such that re-transmission timing is extended to the frame after the next, is considered for data transmission in DL mini-frame #0 or #5 .

Table 7. Latency performance of the proposed structure.

Mode	Data latency	
	DL	UL
FDD	4.87 ms	
TDD 4:4	5.65 ms	
TDD 5:3	5.34 ms	6.03 ms
TDD 6:2	5.85 ms	6.49 ms

As a conclusion from Table 7 above, the latency results for all cases are much less than 10 ms requirement specified in P802.16m SRD [1].

5 Proposed Text for SDD

Insert the following text into Physical Layer clause (i.e. Chapter 11 in [3]):

------------------------------- Text Start ---

11.1 Frame structure

11.1.1 Generic frame structure

The generic frame structure, which shall apply to TDD as well as FDD mode of operation, is defined on the basis of a super-frame as illustrated in Figure xx. The super-frame shall be built up using four 5ms frames. Each

5ms frame in the super-frame shall comprise eight mini-frames. A mini-frame is either dedicated to downlink or uplink.

A single burst may span across more than one contiguous mini-frames.
[Note: The maximum number of contiguous mini-frames that a burst may span is TBD].

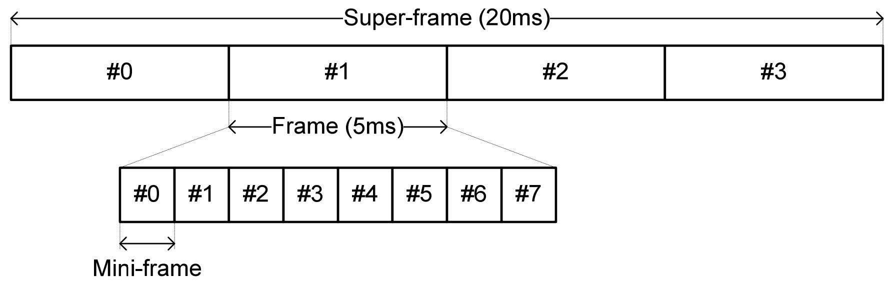


Figure xx. Generic frame structure

For TDD mode, the ratio of DL mini-frames to UL mini-frames shall be one of 8:0, 6:2, 5:3 or 4:4.

11.1.2 Super-frame header

Every super-frame shall contain a super-frame header. The super-frame header shall be located in the first downlink mini-frame of the super-frame. A super-frame header shall include synchronization sequence and system configuration information.

------------------------------- Text End ---

6 References

[1] IEEE 80216m-07/002r4, “IEEE 802.16m System Requirements.”

[2] 3GPP TS 25.912, “Feasibility study for evolved Universal Terrestrial Radio Access (UTRA) and Universal Terrestrial Radio Access Network (UTRAN) (Release 7).”

[3] IEEE C802.16m-07/320r1, “Draft Table of Content for the IEEE 802.16m System Description Document.”