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Re:	IEEE 802.16m-07/047, "Call for Contributions on Project 802.16m System Description Document (SDD)" for the following topic: Proposed 802.16m Protocol Architecture and main functionalities per protocol layer
Abstract	We show the basic concept of LDPC-CC proposed as a new class of LDPC, and compare LDPC-CC with the conventional FEC classes such as Convolutional Turbo Codes (CTC) and LDPC-BC. From the result of the comparison, we show LDPC-CC have advantages of encoder complexity and decoder latency. Hence, we propose LDPC-CC as one of the candidates of FEC scheme, because LDPC-CC are most likely to achieve the peak data rate required for 16m, with low complexity and low latency.
Purpose	For discussion of FEC scheme
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LDPC-Convolutional Codes for IEEE 802.16m FEC Scheme

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1. Introduction

802.16m system shall support the peak data rate as specified in Table 1 as described in 802.16m system requirements [1]. When operating bandwidth is 20MHz, it is necessary to achieve 160Mbps as the baseline requirement and 300Mbps as the target requirement for the peak data rate. Moreover, it is required to achieve such high-speed data rates with low complexity and low latency as much as possible [1].

LDPC codes [2] are promising FEC classes for the next generation communication system. The reason is that LDPC codes enable not only to achieve as good performance as Turbo codes, but also to achieve high-speed decoding, thanks to parallel processing with message-passing decoding. LDPC codes have two classes, LDPC-Block Codes (BC) and LDPC-Convolutional Codes (CC). LDPC-BC [3], [4] have already been adopted as IEEE802.16e option and also have been decided to adopt in the next generation communication/broadcasting standards, such as 10GBASE-T, 802.11n and DVB-S2, while LDPC-CC have been proposed as a new class of LDPC codes in recent years [5] [6] [7].

In this contribution, we show the basic concept of LDPC-CC and compare LDPC-CC with the conventional FEC classes such as Convolutional Turbo Codes (CTC) [3] and LDPC-BC. From the result of the comparison, we show LDPC-CC have advantages of encoder complexity and decoder latency, compared with LDPC-BC. Hence, we propose LDPC-CC as one of the candidates of FEC scheme, because LDPC-CC are most likely to achieve the peak data rate required for 16m, with low complexity and low latency.

Table 1: Requirements of Peak Data Rate in Downlink.

Requirement Type	**MIMO Configuration**	**Normalized peak rate (bps/Hz)**	**Peak rate (bps) when operating bandwidth is 20MHz**
Baseline	2x2	8.0	160M
Target	4x4	15.0	300M

2. Basic Concept of LDPC-CC

In the late 1990's, LDPC-CC were proposed by Felstrom and Zigangirov [6]. LDPC-CC are Convolutional Codes defined by Low-Density Parity-Check matrix. Hereafter, a typical example of LDPC-CC scheme is shown in the literature of [6].

LDPC-CC can be defined by a parity-check matrix H, and the parity-check matrix H of LDPC-CC with coding rate R=1/2 is expressed as Eq. (1). The size of parity-check matrix H is $k \times 2k$. Each column corresponds to "Systematic Bits ($d_1,\ldots, d_k$)" and "Parity Bits ($p_1,\ldots,p_k$)", where order is : $d_1, p_1, d_2, p_2, \ldots, d_t, p_t, \ldots, d_k, p_k$, and M is memory length (constraint length) in LDPC-CC. Each raw represents a parity-check polynomial. $h_d^{(i)}(t)$ (i =0,…, M) represents Systematic Bit weight ("1(one)" or "0(zero)") at t-th order parity-check polynomial equation, $h_p^{(i)}(t)$ (i=0,…,M) represents Parity Bit weight ("1(one)" or "0(zero)") at t-th order parity-check polynomial equation. In the matrix H, all elements are "0(zero)" other than $h_d^{(i)}(t)$ and $h_p^{(i)}(t)$. As shown in Eq. (1), the parity-check matrix of LDPC-CC is configured "1" in a diagonal line and nearby. LDPC-

CC encoder outputs "Code Bits (a pair bits)", sequentially $\{d_1, p_1\}$, $\{d_2, p_2\}$, $\{d_3, p_3\}$, …, $\{d_k, p_k\}$. Systematic Bit (d_t) and Parity Bit (p_t) at t-th order outputs of LDPC-CC encoder are given by Eq. (2) by using $h_d^{(i)}(t)$, $h_p^{(i)}(t)$ and u_t. Here, u_t is Information Bit at t-th order input. The encoding of LDPC-CC can be realized with an arbitrary encoder as shown in Eq. (2).

$$\mathbf{H} = \begin{bmatrix}
h_d^{(0)}(0) & h_p^{(0)}(0) & 0 & 0 & \cdots & & & & \cdots & 0 & 0 \\
h_d^{(1)}(1) & h_p^{(1)}(1) & h_d^{(0)}(1) & h_p^{(0)}(1) & \cdots & & & & & \vdots & \vdots \\
\vdots & \vdots & \vdots & \vdots & \ddots & & & & & & \\
h_d^{(M)}(M) & h_p^{(M)}(M) & h_d^{(M-1)}(M) & h_p^{(M-1)}(M) & \cdots & & & & & & \\
0 & 0 & h_d^{(M)}(M+1) & h_p^{(M)}(M+1) & \cdots & & & & & \vdots & \vdots \\
\vdots & \vdots & & & \ddots & \ddots & & & \ddots & 0 & 0 \\
0 & 0 & \cdots & & \cdots & 0 & h_d^{(M)}(k) & h_p^{(M)}(k) & \cdots & h_d^{(0)}(k) & h_p^{(0)}(k)
\end{bmatrix}$$

--- Eq. (1)

$$\begin{cases} d_t = u_t \\ p_t = \sum_{i=0}^{M} h_d^{(i)}(t) u_{t-i} + \sum_{i=1}^{M} h_p^{(i)}(t) p_{t-i} \end{cases} \quad \text{--- Eq. (2)}$$

An example of encoder structure in LDPC-CC is shown in Fig. 1. LDPC-CC encoder consists of M pieces of shift register for u_t, M pieces of shift register for p_t and weight controller outputting bit weights shown as $h_d^{(i)}(t)$, $h_p^{(i)}(t)$. LDPC-CC encoder performs encoding process as shown in Eq. (2) by adopting such structure.

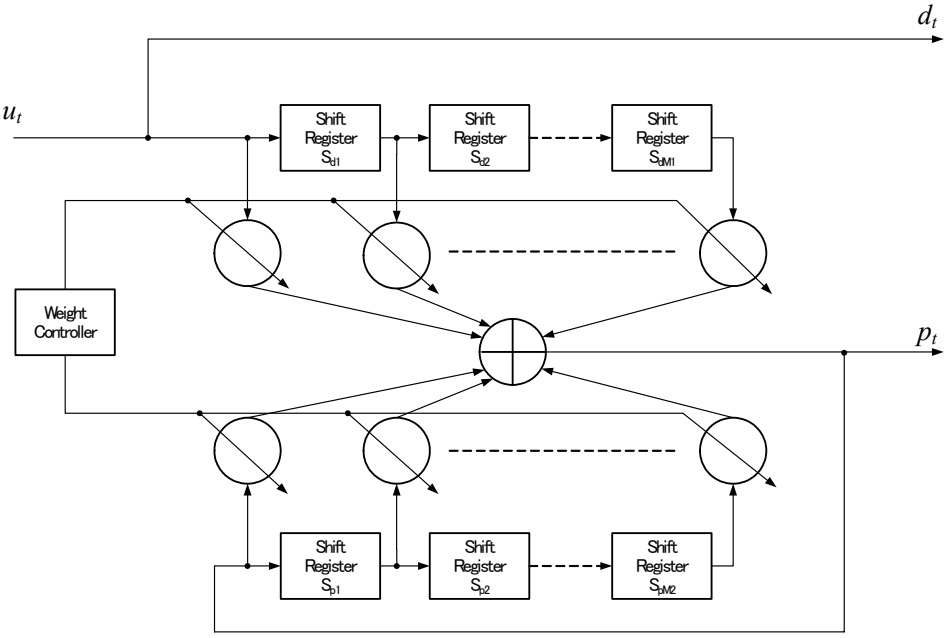

Fig. 1: Structure of LDPC-CC encoder [6].

3. The comparison between LDPC-CC and conventional FEC classes

We show the comparison results between the proposed LDPC-CC and the conventional FEC classes such as Convolutional Turbo codes (CTC) [3] and LDPC-BC [3] as follows：

Advantages of LDPC-CC with respect to CTC:

- Internal interleaver is *not* necessary in the encoder.
- Encoder can be composed of the only "shift register" and "adder".
- Low latency in decoding process, thanks to no interleaver and parallel processing with message-passing decoding. (CTC inherently require sequential process. Applying parallel processing techniques [e.g., windowing] for Turbo Codes will result in performance degradation [10].)
- Decoder can support achievement of high data rate with comparative ease, due to parallel processing decoding.
- The information data of arbitrary length can be encoded since the length of the information data is not limited by the interleaver length.

Advantages of LDPC-CC with respect to LDPC-BC:

- There is high possibility that the hardware complexity of LDPC-CC encoder is less than that of LDPC-BC encoder. The computational complexity of LDPC-CC encoding is proportional to the memory length (constraint length), meanwhile the computational complexity of LDPC-BC encoding is proportional to the information length（constraint length < information length）.
- Low latency in decoding process. Decoder outputs sequentially by using a decoding algorithm that utilizes the structure of parity check matrix of LDPC-CC.
- Information data of arbitrary length can be encoded since the length of the information data is not limited by the block length of parity check matrix.

Table 2 shows summaries of the comparison results between LDPC-CC, LDPC-BC and CTC.

Table 2: Comparison of FEC schemes.

<table>
<tr><th></th><th>LDPC–CC[6]</th><th>LDPC –BC</th><th>Turbo code (CTC)</th></tr>
<tr><td rowspan="2">Decoder latency</td><td colspan="2">LDPC can adopt parallel processing decoding.
Channel interleaver and internal interleaver are not necessary.</td><td>Turbo Codes inherently require sequential process.
Channel interleaver and internal interleaver are necessary.</td></tr>
<tr><td>Decoder outputs sequentially.</td><td>Decoder outputs the data of each code word length.</td><td>Decoder outputs the data of each internal interleaver length in the encoder.</td></tr>
<tr><td>Encoder complexity</td><td>Encoder is composed of the only shift register and adder.
The complexity is proportional to the constraint length (constraint length < information length）.</td><td>The complexity is proportional to the information length.</td><td>Encoder is composed of shift register, adder and interleaver.</td></tr>
<tr><td>Decoder complexity</td><td colspan="3">Similar[6] [9]</td></tr>
<tr><td>Variable block length support</td><td>The information data of arbitrary length can be encoded.</td><td>Parity check matrixes of different cord word length are necessary.</td><td>The length of the information data is limited by multiples of the internal interleaver length.</td></tr>
</table>

4. The performance of LDPC-CC

The performance of LDPC-CC is close to the "Shannon Limit", similarly as "CTC (Convolutional Turbo Codes)" and "LDPC-BC (Block Codes)" in case of using sufficient cord word length [6] [8].

An example of performance in LDPC-CC based on the literature of [7] is shown. Figure 2 shows BER and WER (Word Error Rate) performances under AWGN channels. Information bit length is 600 bits. The performance of LDPC-BC is shown in [4] for example. We can confirm the LDPC-CC performance is as good as LDPC-BC, as shown in Fig. 2.

As for the comparison of performance between LDPC-BC and CTC, it is shown that the performance of the two codes is almost equal in [9].

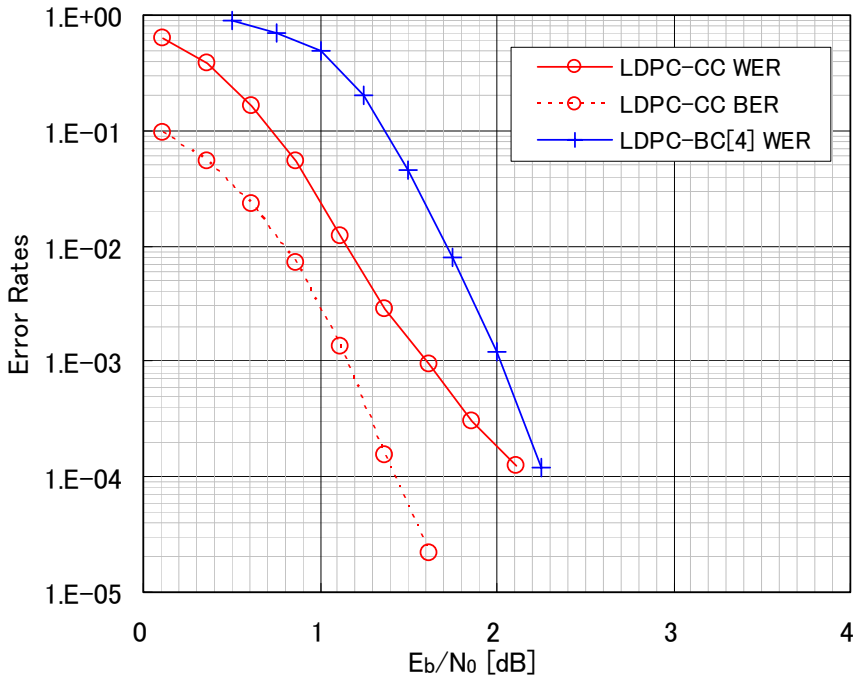

Fig. 2: An example of performance in LDPC-CC. (Information bit length = 600bits)

5. Conclusions

We compared LDPC-CC with LDPC-BC and CTC. From the result of the comparison, we showed advantages of LDPC-CC as follows:

- The performance of LDPC-CC is as good as LDPC-BC and CTC.
- LDPC-CC have the major advantage in enabling decoder to adopt parallel decoding process, as compared with CTC.
- LDPC-CC have advantages of encoder complexity, decoder latency, as compared with LDPC-BC.

Hence, we propose LDPC-CC as one of the candidates of FEC scheme, because LDPC-CC are most likely to achieve the peak data rate required for 16m, with low complexity and low latency.

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