

Project	IEEE 802.16 Broadband Wireless Access Working Group < http://ieee802.org/16 >
Title	Rate Compatibility and Incremental Redundancy HARQ for 802.16m LDPC
Date	2008-07-07
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Re:	Response to the Call for Contributions IEEE 802.16m-08/016 — Link Adaptation, HARQ
Abstract	This contribution proposes a link adaptation technique for 802.16m system description document (SDD).
Purpose	To enhance the current IEEE 802.16e LDPC as suggested in this contribution into the IEEE 802.16m.
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Table of contents

1. Introduction	2
2. Summary of Proposal	2
3. Performance Results	3
4. Proposed Text Additions	5
6.3.2.3.43.7.9 MIMO Compact UL	5
6.3.2.3.43.7.10 SDMA Compact UL-MAP IE format	5
6.3.17 No change necessary	5
6.3.17.1 <i>No change necessary</i>	5
6.3.17.2 <i>No change necessary</i>	5
6.3.17.3 <i>No change necessary</i>	5
8.4.5.3.21 HARQ DL MAP IE	5
8.4.5.4.24 HARQ UL MAP IE	6
8.4.9.2.5.1 Code description	6
8.4.9.2.5.2 Code block size adjustment	7
8.4.9.2.5.3.1 Packet encoding for HARQ	8
8.4.9.2.5.4 Subpacket generation for LDPC	8
8.4.9.2.5.4.1 Symbol separation	8
8.4.9.2.5.4.2 Symbol selection	8
8.4.9.2.5.5 Optional H-ARQ Optional IR HARQ	9
8.4.15 Optional HARQ support	9
8.4.15.2.2 Optional IR HARQ for LDPC	10
11.8.3.7.19 HARQ buffer capability	10
11.8.3.7.19.1 HARQ incremental redundancy buffer capability	10
5. Conclusions	11

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1. Introduction

One of the most important advantages of LDPC is its higher decoding efficiency compared to Turbo codes. Therefore, a high throughput link such as BS-MS could be achieved with lower hardware cost. Unfortunately, current 802.16e LDPC is not rate compatible and does not support 1/3 code rate. In addition, the current LDPC only support HARQ with chase combining but not incremental redundancy (IR).

1/3 code rate and IR HARQ are known to improve reliability or robustness in links with hostile channel conditions.

We proposed an enhanced version of 802.16 LDPC using the current 802.16e LDPC as the baseline. We called rate compatible RC-LDPC will support 1/3 rate code and also provide the means to support HARQ with incremental redundancy to provide the BS-MS links operating in hostile channel condition, with high throughput, improved robustness and increased decoding efficiency.

2. Summary of Proposal

We proposed the construction of an extended parity-check matrix of the RC (Rate-Compatible)-LDPC codes to achieve good performance for wide range of code word length and code rate. The parity-check matrix construction method can support code rates ranging from 1/3 to 4/5 and codeword lengths ranging from 288 bits to 2304bits. The RC-LDPC codes are constructed using a code-rate 1/2 parity-check matrix for code-rate greater than or equal to 1/2. For code rate smaller than 1/2 an additional parity check matrix is being extended to the 1/2 parity-check matrix.

The proposed RC-LDPC uses the current 802.16 LDPC as the baseline matrix. It also uses the same four sub-packets protocol for its HARQ operation. The proposal provides some small additions and requires no change to the current 802.16e LDPC.

3. Performance Results

We show the complexity comparison between LDPC and CTC decoder in table 1 and the performance of the proposed RC-LDPC codes as shown in figures 1 and 2. As for the complexity comparison, under the condition of same constraint length as the 3GPP turbo code in [1] [2], the total cost of CTC is twice than that of 3GPP turbo codes. So, from the reference paper [2], we calculate the cost value of LDPC vs CTC as shown in table 1.

Table 1: Operations count comparison of sub-optimal decoders LDPC and CTC decoders

	LDPC	CTC	Complexity of LDPC / Complexity of CTC
Algorithm	LBP Min-Sum+Offset	Max Log Map +extrinsic scaling	
Number of Iterations	20	8	
Total cost (R=1/2)	28.8K x 20 = 576K	171K x 8 x 2 = 2736K	21%
Total cost (R=3/4)	20.6K x 20 = 412K	171K x 8 x 2 = 2736K	15%

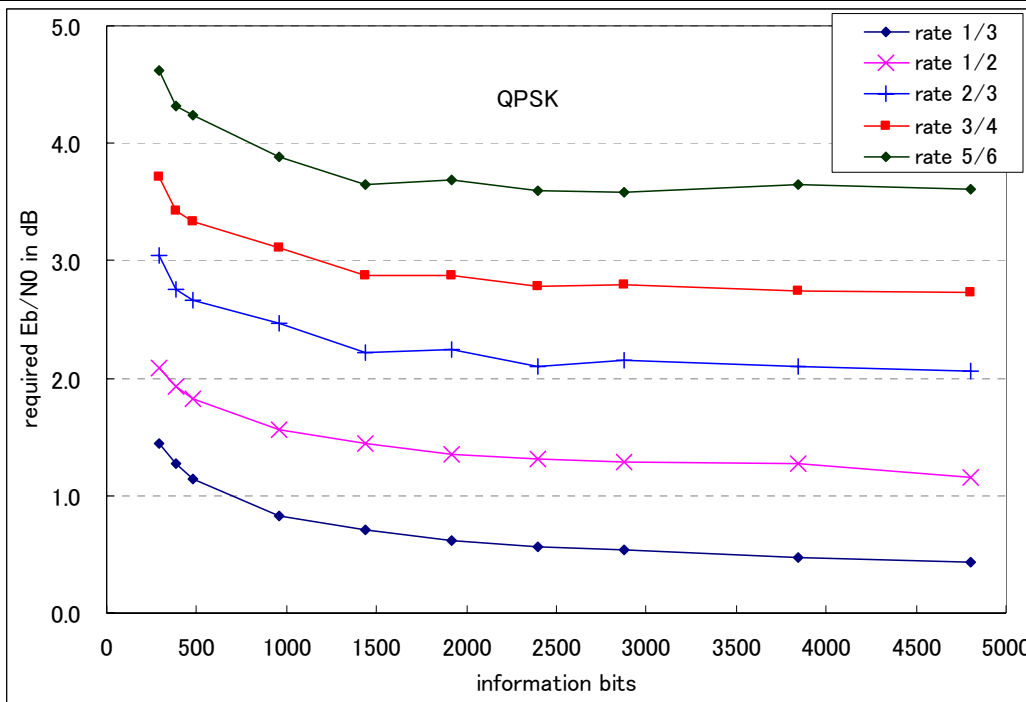


Figure 1: Performance for RC LDPC codes based on the 16e LDPC codes
(Sum-product decoding , iteration:30)

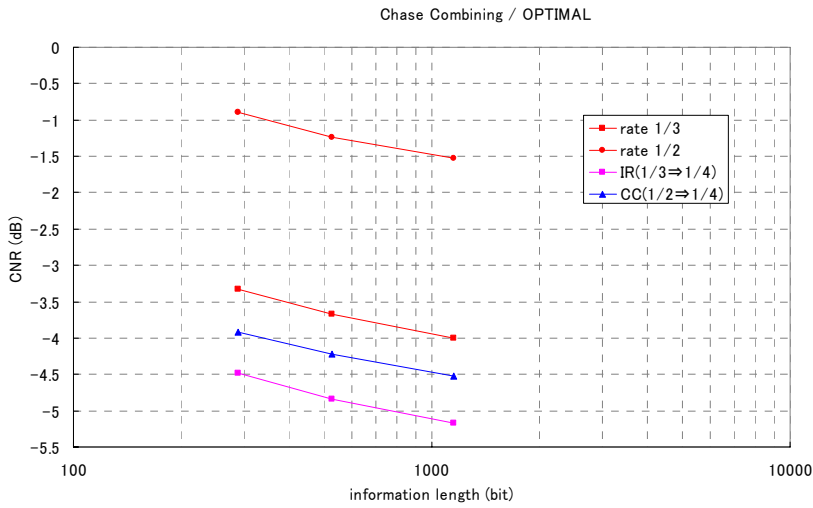


Figure 2: Performance of RC LDPC codes based on the 16e LDPC

The codeword with less than code-rate 1/3 can be constructed by cyclically repeated from the rate 1/3 codeword.

Figure 2 show the performance comparison between a IR code (cyclically repeated code) and a CC code (simple repeat code).

The IR code with rate 1/4 (cyclically repeat from rate 1/3 code) out performs the CC code with rate 1/4(simple repeat of rate 1/2 code) by 0.5dB. So we should make low-rate code by RC-LDPC codes based on the 1/3 code.

4. Proposed Text Additions

6.3.2.3.43.7.9 MIMO Compact UL

Insert into Table 109a – MIMO Compact UL-MAP IE format

Syntax	Size	Notes
If (HARQ Mode=CTC Incremental Redundancy) { If (HARQ Mode=LDPC Incremental Redundancy	-	HARQ Mode is specified in the HARQ compact UL_MAP IE format for Switch HARQ Mode hardware

6.3.2.3.43.7.10 SDMA Compact UL-MAP IE format

Insert into Table 109b – SDMA compact UL-MAP IE format

Syntax	Size	Notes
If (HARQ Mode=CTC Incremental Redundancy) { If (HARQ Mode=LDPC Incremental Redundancy	-	HARQ Mode is specified in the HARQ compact UL_MAP IE format for Switch HARQ Mode hardware

6.3.17 No change necessary

6.3.17.1 No change necessary

6.3.17.2 No change necessary

6.3.17.3 No change necessary

8.4.5.3.21 HARQ DL MAP IE

Insert:

Incremental redundancy HARQ for LDPC (HARQ LDPC-IR)

Insert into Table 2861 – HARQ DL MAP IE format

Syntax	Size	Notes
Mode	4 bits	0b0111=Incremental redundancy HARQ for LDPC

systematic codeword such that:

$$\mathbf{v} := (u_1 \ u_2 \ \cdots \ u_K \ r_1 \ r_2 \ \cdots \ r_M) \text{ satisfying } \mathbf{H}_M \cdot \mathbf{v}^T = \mathbf{0}.$$

The RC-LDPC encoder consists of a common LDPC encoder and a puncturing device that punctures the parity bits. The systematic bits are not punctured. The decoder for RC-LDPC codes is the same as an ordinary LDPC decoding algorithm with received LLR=0 for puncturing bits.

A set of code rates and un-puncturing parity bits set $\hat{\mathbf{r}}$ for RC-LDPC codes can be represented by:

For the number of un-puncturing bits $i (\leq M/2)$, $\hat{\mathbf{r}} = \{\hat{r}_i\}$,

For $p = 0$ to 11 { $c(p) = 0$ }

For $p = 0$ to 11 {

For $q = 0$ to $z-1$ {

$w_{j,c(j)} = r_{k+1}$ where $j = (p \cdot z + q) \bmod 8$, $k = p \cdot z + ((p+q) \bmod 8)$,

$c(j) = c(j) + 1$

}

}

$\mathbf{l} = (0,4,2,6,1,5,3,7)$, $k = 1$

For $p = 0$ to 7 {

For $q = 0$ to $c(p) - 1$ {

$\hat{r}_k = w_{l(p),q}$,

If $k = i$ then exit

$k = k + 1$

}

}

For the number of un-puncturing bits $i (> M/2)$,

$\hat{\mathbf{r}} = \{\mathbf{r}_l\}$, for $M/2 \leq l \leq i$,

where, \mathbf{l} is a vector such that $\mathbf{l} = (l(0), l(1), \dots, l(i), \dots, l(7))$, $0 \leq i \leq 7$.

8.4.9.2.5.2 Code block size adjustment

The LDPC code flexibly supports different block sizes for each code rate through the use of an expansion factor.

Each base model matrix has $n_b=24$ columns, and the expansion factor (z factor) is equal to $n/24$ for code length n . In each case, the number of information bits is equal to the code rate times the coded length n .

Insert into RC-LDPC block Sizes and the number of subchannels.

The code length N shall cover from 576 bits to 14400 bits for the RC-LDPC code. The supported code-rate shall be equal to and more than 1/3.

The number of slots shall be calculated as follows,

If N (bits) is a multiple of 96,

QPSK can be used as $N_{subchannels} = N/96$,

else if N (bits) is a multiple of 96x2,

16QAM can be used as $N_{subchannels} = N/(96 \times 2)$,

else if N (bits) is a multiple of 96×3 ,
 64QAM can be used as $N_{\text{subchannels}} = N/(96 \times 3)$,
 end.

8.4.9.2.5.3.1 Packet encoding for HARQ

Insert.

The reordered codeword for RC-LDPC codes are defined such as

$$\bar{\mathbf{V}} := (\bar{v}_1 \quad \bar{v}_2 \quad \cdots \quad \bar{v}_{K+M}) = (u_1 \quad u_2 \quad \cdots \quad u_K \quad \hat{r}_1 \quad \hat{r}_2 \quad \cdots \quad \hat{r}_M).$$

Insert this subclause

8.4.9.2.5.4 Subpacket generation for LDPC

Proposed FEC structure punctures the reordered codeword to generate a subpacket with various coding rates. The subpacket is also used as HARQ packet transmission. 1/3 LDPC encoded codeword puncturing is performed. The puncturing is performed to select the consecutive bit sequence that starts at any point of the whole reordered codeword. For the first transmission, the subpacket is generated to select the consecutive bit sequence that starts from the first bit of the systematic part of the reordered codeword. The length of the subpacket is chosen according to the needed coding rate reflecting the channel condition. The first subpacket can also be used as a codeword with the needed coding rate for a burst where HARQ is not applied.

Insert this subclause

8.4.9.2.5.4.1 Symbol separation

Insert.

All of the encoded symbols shall be demultiplexed into three subblocks denoted A, Y, and W as shown in Figure 5.

A, Y, and W subblocks are defined as

$$\mathbf{A} := (u_1 \quad u_2 \quad \cdots \quad u_K), \mathbf{Y} := (\hat{r}_1 \quad \hat{r}_2 \quad \cdots \quad \hat{r}_{M/2}), \text{ and } \mathbf{W} := (\hat{r}_{M/2+1} \quad \hat{r}_{M/2+2} \quad \cdots \quad \hat{r}_M).$$

The encoder output symbols shall be sequentially distributed into 3 subblocks with the first encoded output symbols going to the A subblock, the second encoder output going to the Y subblock and the third to the W subblock, etc.

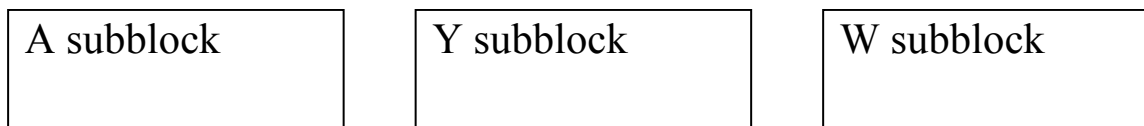


Figure 5: Subblocks for RC-LDPC codes

Insert this subclause

8.4.9.2.5.4.2 Symbol selection

Lastly, symbol selection is performed to generate the subpacket. The puncturing block is referred as symbols selection from the viewpoint of subpacket generation.

The reordered code is transmitted with one of the subpackets. The symbols in a subpacket are formed by selecting specific sequences of symbols from the LDPC encoder output sequence. The resulting subpacket sequence is a binary sequence of symbols for the modulator.

Let k be the subpacket index when HARQ is enabled $k=0$ for the first transmission and increases by one for the next subpacket. $k=0$ when HARQ is not used

N_{EP} be the number of bits in the encoder packet (before encoding)

N_{SCHk} be the number of subchannel(s) allocated for the k -th subpacket

m_k be the modulation order for the k th subpacket ($m_k=2$ for QPSK , 4 for 16-QAM, and 6 for 64-QAM)

S_{PIDk} be the subpacket ID for the k -th subpacket, (for the first subpacket, $S_{PID_{k=0}}=0$)

Also, let the scrambled and selected symbols be numbered from zero with the 0^{th} symbol being the first symbol in the sequence. Then, the index of the i -th symbol of the k th subpacket shall be:

$$S_{k,i} = (F_{k+i}) \bmod (3 \cdot N_{EP})$$

where,

$$T=0 \dots L_{k-1},$$

$$L_k = 48 \cdot N_{SCHk} \cdot m_k,$$

$$F_k = (S_{PIDk} \cdot L_k) \bmod (3 \cdot N_{EP})$$

The N_{EP} , N_{SCHk} , m_k , and S_{PID} values are determined by the BS and can be inferred by the SS through the allocation size in the DL-MAP and UL-MAP. The above symbol selection makes the following possible:

1. The first transmission includes the systematic part of the reordered code. Thus it can be used as the codeword for a burst where the HARQ is not applied.
2. The location of the subpacket can be determined by the SPID itself without the knowledge of previous subpacket. It is a very important property for HARQ retransmission.

8.4.9.7 Multiple HARQ (optional)

Insert into Table 333c – HARQ Modes definition

HARQ Mode	Definition
3	LDPC Incremental Redundancy

Insert this subclause.

8.4.9.2.5.5 Optional H-ARQ Optional IR HARQ

The procedure of HARQ LDPC subpacket generation is as follows: Padding, CRC addition, Fragmentation, Randomization and LDPC encoding. HARQ implementation is optional.

8.4.15 Optional HARQ support

Insert.

Incremental redundancy for LDPC codes – specified in section 6.3.17 and in 8.4.9.2.3.5

8.4.15.2.2 Optional IR HARQ for LDPC

Insert.

The following optional modes exist for HARQ.

Incremental redundancy for LDPC codes –specified in section 8.4.9.2.5.4

11.8.3.7.19 HARQ buffer capability

Insert.

Downlink/Uplink HARQ buffering capability indicates the maximal number of data bits the SS is able to store for downlink/uplink HARQ. The buffering capability is separately indicated for NEP/HSCH based incremental redundancy used for CTC and LDPC, and for DIUC/duration based HARQ methods (Chase combining and CC-IR) and separately for uplink and downlink transmissions.

- For incremental redundancy LDPC (NEP based): Number of bits is indicated by NEP code, according to Table 330

The IR-CTC and IR-LDPC HARQ buffer capability shall also be applied to bursts for which ACK channel is not allocated (ACK disable is set).

11.8.3.7.19.1 HARQ incremental redundancy buffer capability

Insert into Table: HARQ incremental redundancy buffer capability

		Value	Scope
		Bits #0-3;N _{EP} value indicating downlink HARQ buffering capability for incremental redundancy LDPC. Bits #4;Aggregation Flag for DL Bits #5-7;Reserved Bits #8-11;N _{EP} value indicating uplink HARQ buffering capability for incremental redundancy LDPC. Bits #12;Aggregation Flag for UL Bits #13-15;Reserved	SBC-REQ SBC-RSP

5. Conclusions

LDPC support high throughput with less hardware complexity and lower cost compared to Turbo Codes. Our RC-LDPC is an enhanced version of the current 802.16e LDPC. It uses the 802.16e LDPC as a baseline. RC-LDPC is rate compatible and can provide 1/3 code rate and Hybrid ARQ with incremental redundancy. For operation in very hostile channel conditions as shown in Figure 3, such as those encountered by mobile MS or non-LOS MS and nomadic MS, RC-LDPC would be able to provide improved robustness to the BS-MS links.

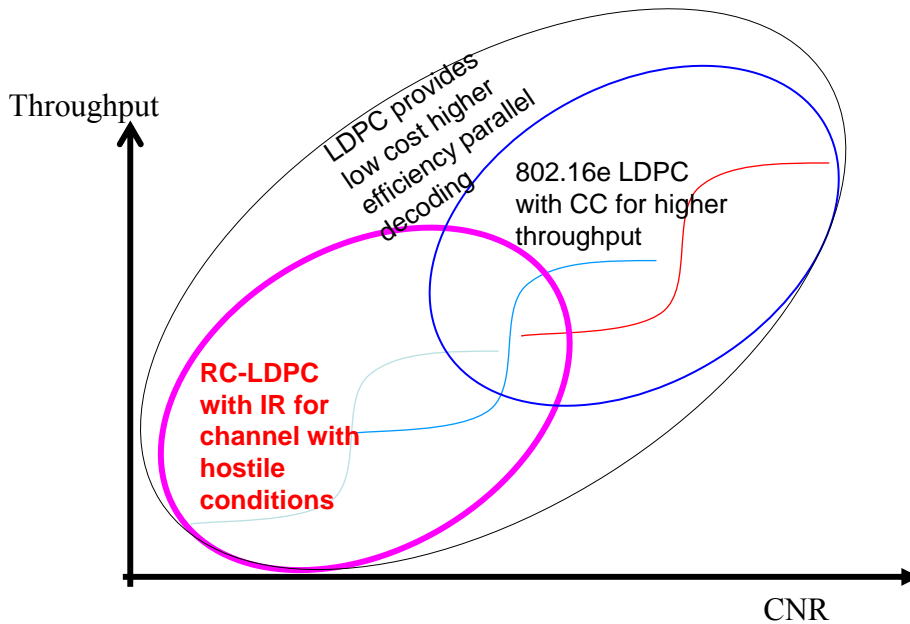


Figure 6: RC-LDPC is best for hostile channel conditions

[References]

- [1] TS 25.222 V3.1.1 multiplexing and channel coding (FDD), 3GPP TSG RAN WG1, Dec. 1999
- [2] R1-060874, Intel ,ITRI, LGE, Mitsubishi, Motorola, Samsung, ZTE, "Complexity Comparison of LDPC Codes and Turbo Codes", 3GPP TSG RAN WG1 #44bis, Athens, Greece, Mar 27-31, 2006.