16m Power Control Channel Design

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None
Purpose:
To be discussed and adopted by TGm for use in stage 3 document development

Outline

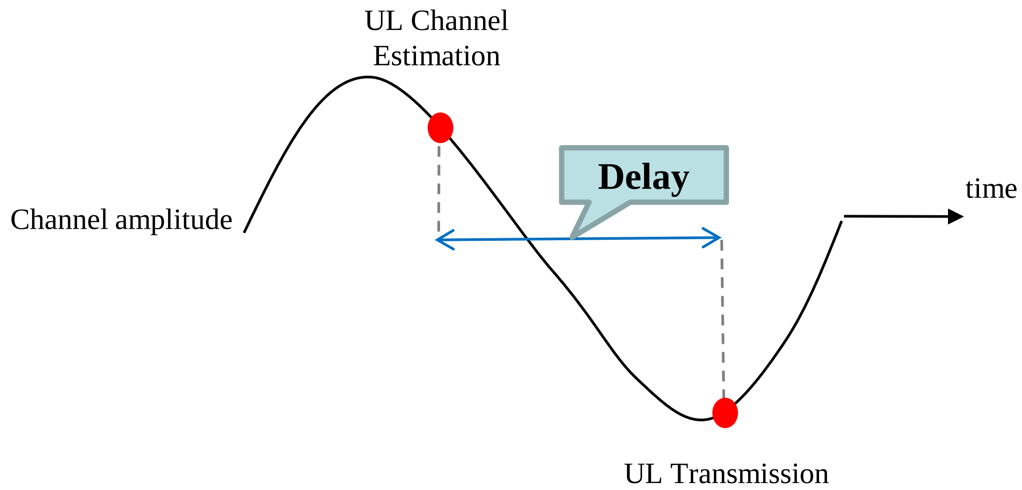
- Uplink Power Control
  - Slow power control
  - Fast power control
  - Gain of fast power control
- Gain of Fast Power Control
  - Link level verification
  - Effect of MS Speed and Delay
  - Effect of TPC bit size
- DL Power Control Channel Design
- Simulation Results
- Conclusions and Proposed Text
- Appendix

Uplink Power Control

- Slow Power Control
  - To compensate longterm pathloss and shadowing
  - MS estimates by using DL reference signal and information
- Fast Power Control
  - To compensate fast fading as well as pathloss and shodowing
  - In FDD systems, BS estimates UL channel and send TPC to MS
  - In TDD systems, MS can estimate UL channel thanks to DL/UL reciprocity
- Gain of Fast Power Control is dependent on
  - *Delay btw channel estimation and UL transmission
    - *Delay is described in the next page
  - MS speed impacts on gain
  - UL channel estimation accuracy
  - TPC command error rate (FDD systems)

Uplink Power Control

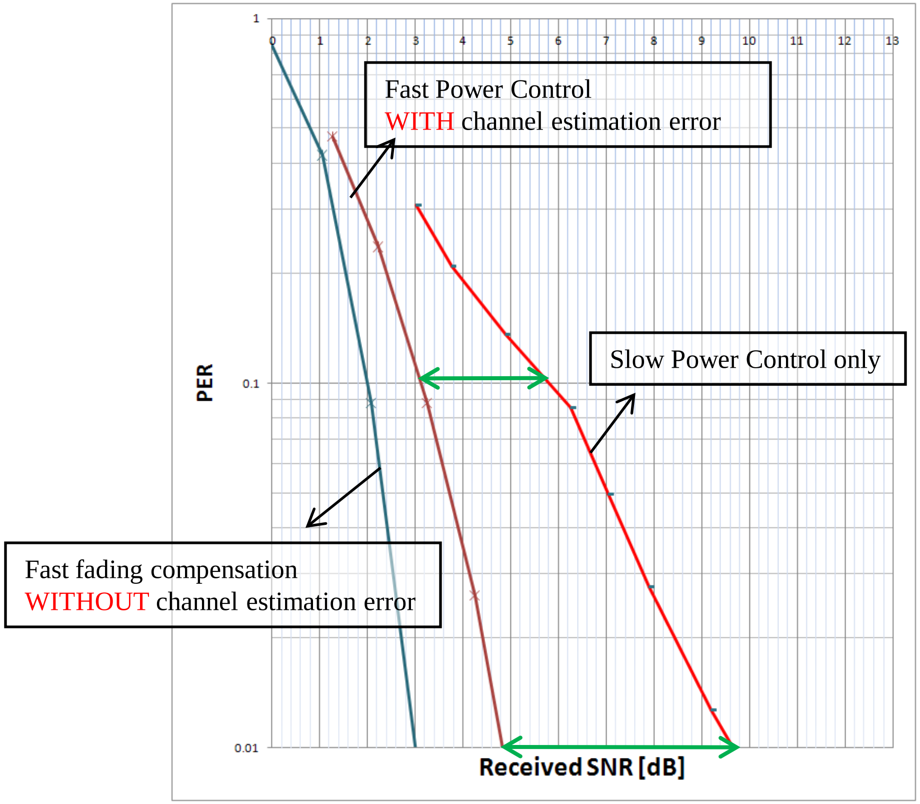
- Delay between CH Estimation and UL Transmission



  - In addition to MS speed, delay between estimation and UL Tx impacts on the gain of fast power control
  - In FDD systems, UL channel estimation can be based on UL reference signal, uplink control channel or pilot of latest transmitted packet
  - In TDD systems, UL channel estimation can be based on DL reference signal, or DL pilot thanks to DL/UL reciprocity

Gain of Fast Power Control

- Link Level Verification



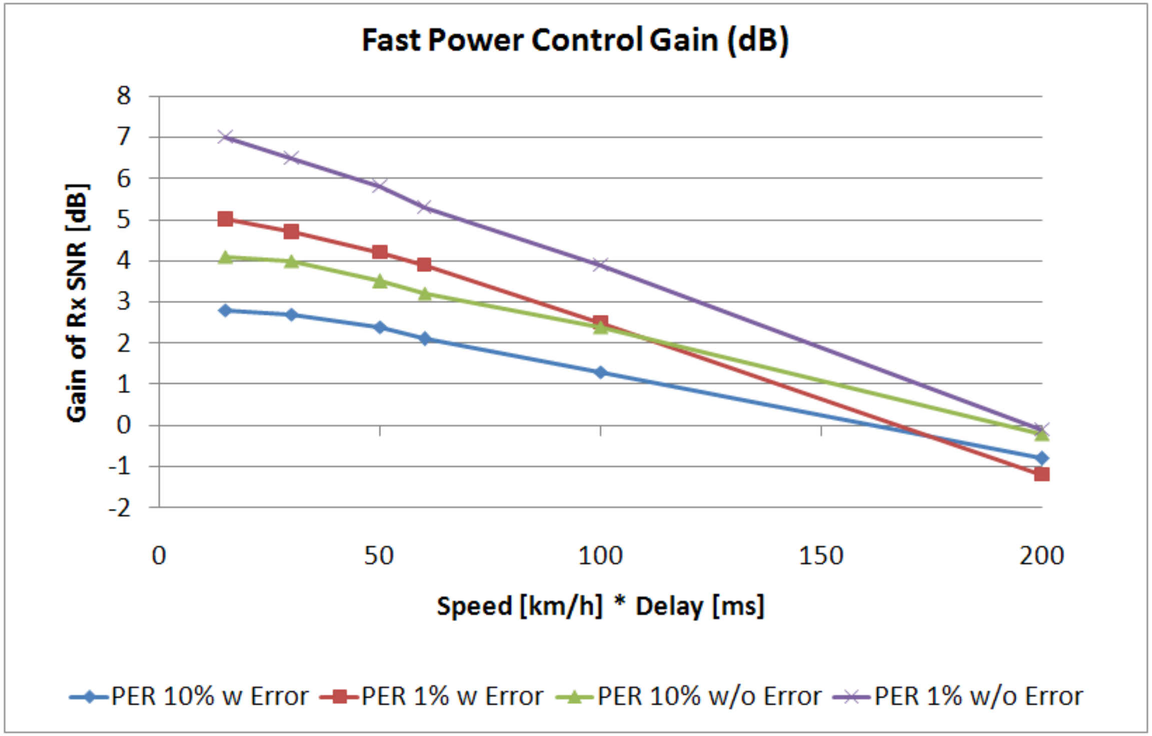
– Condition
  – Nep : 480
  – Code rate : 1/2 Repetition : no
  – Number of Rx Antenna : 2, MRC
  – Center freq. : 2.3GHz
  – MS speed : 3km/h
  – Channel : Ped A
  – Sampling rate : 10MHz
  – Num. of UL symbol for data : 15
  – Subchannelization : PUSC SR on
  – Delay btw estimation & Tx: 10ms
  – Estimation error model : Normal(0,1.3)*

→ *Even with realistic channel estimation error, link performance can benefit from power control (2.7dB @ PER 10%, 4.8dB @ PER 1%)*

* Refer to Appendix A for estimation error modeling

Gain of Fast Power Control

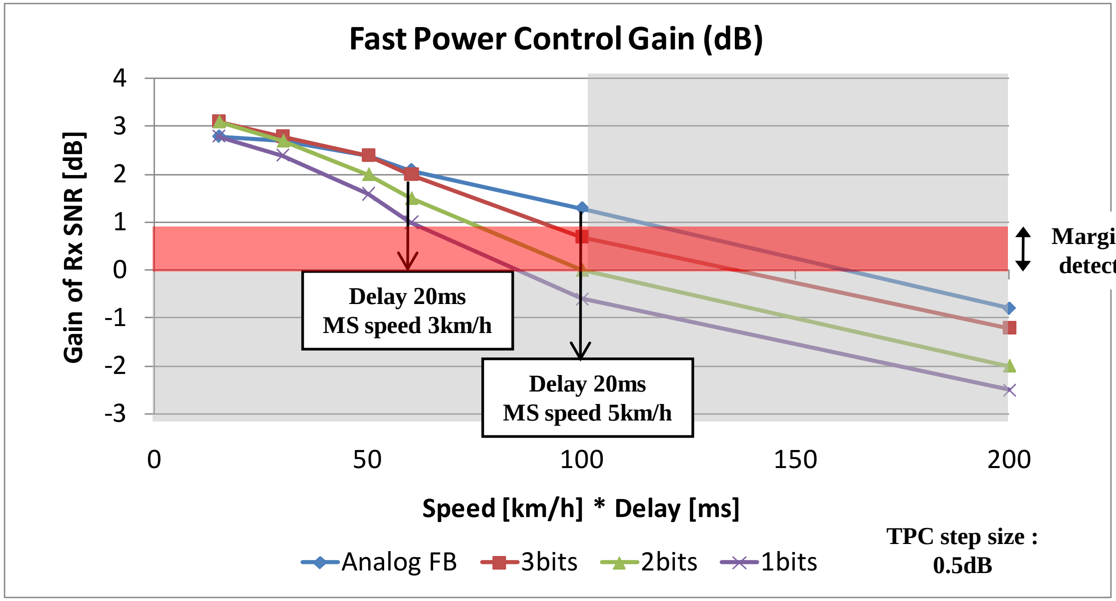
- Effect of MS Speed and Delay
  - Gain over slow power control



→ *As generally known, low speed and short delay between estimation and UL transmission can bring large gain of power control*

Gain of Fast Power Control

- Effect of TPC bit size



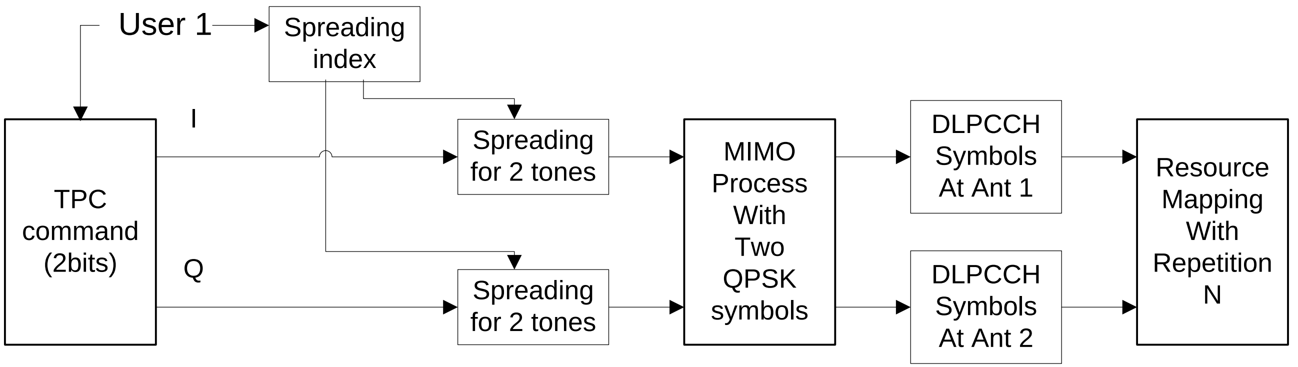
  - For VoIP case, max. delay can be assumed as 20ms
    - Because MS send VoIP packet at least with 20ms period
  - TPC step size is assumed to be 0.5dB*
  - Considering SNR margin for TPC detection error** @ MS, *2 bit is reasonable* for TPC size to retain gain of fast power control

* Refer to Appendix B

** Refer to Appendix C for estimation error modeling

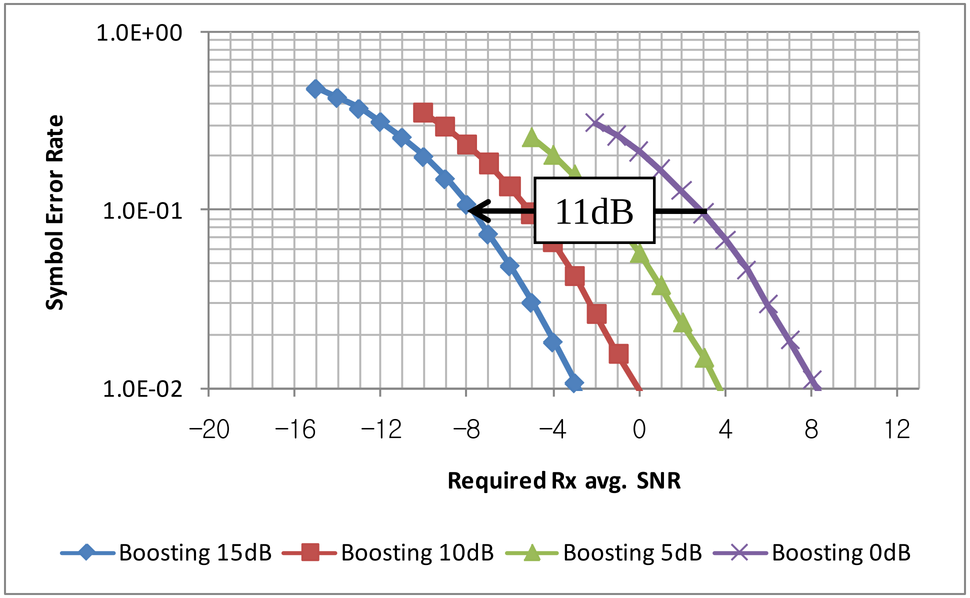
DL PC Channel Design

- Given conditions from SDD
  - Tone-pair subcarrier permutation
  - FDM with data
- Derived conditions from SDD
  - MIMO transmission is SFBC
  - USCCH uses power boosting and repetition to satisfy link performance
- Target Link Performance
  - 10% Symbol Error Rate
- Modulator



Simulation Results

- Conditions
  - MIMO : SFBC
  - Common pilot boosting : 3dB*
    - * If pilot boosting is 0dB, then pilot tone power is same to data tone power with 0dB boosting
  - Channel : PedB 3km/h
  - Channel estimation : averaging within 1 PRU

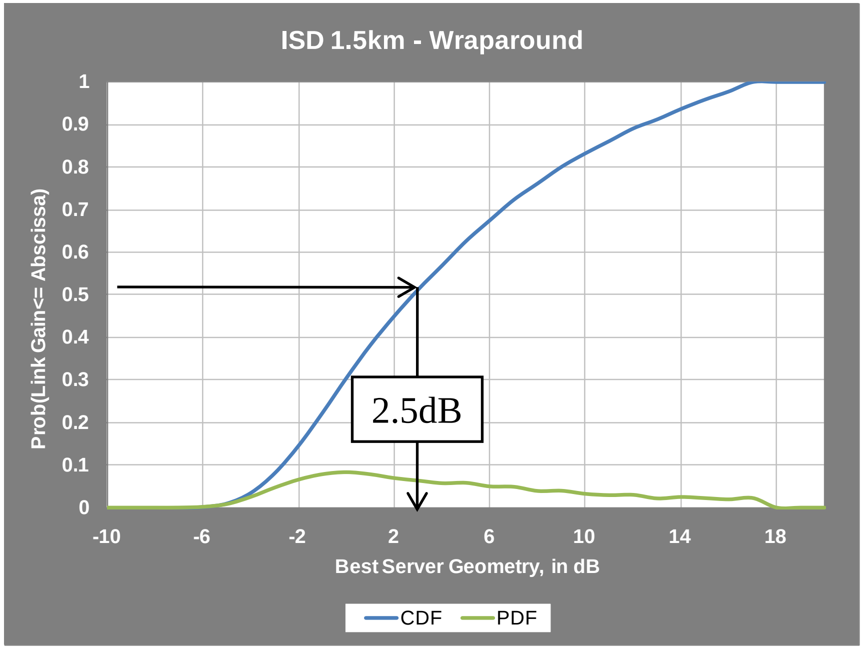


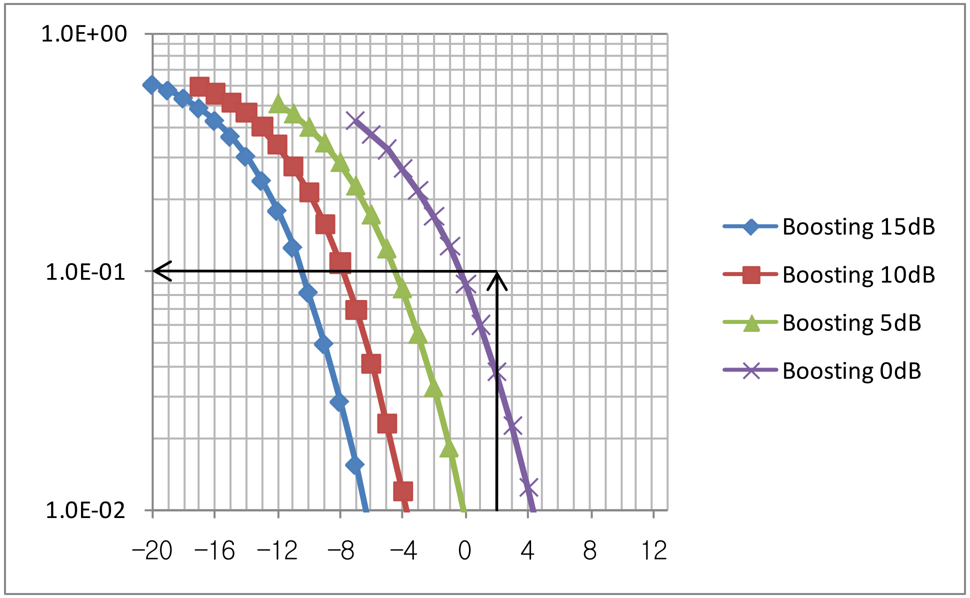
Comparing 0dB and 15dB boosting, only 11dB gain can be realized. This is because of channel estimation error.

Now, the question is how many repetition is required for 0dB boosting user to satisfy the requirement.

Simulation Results

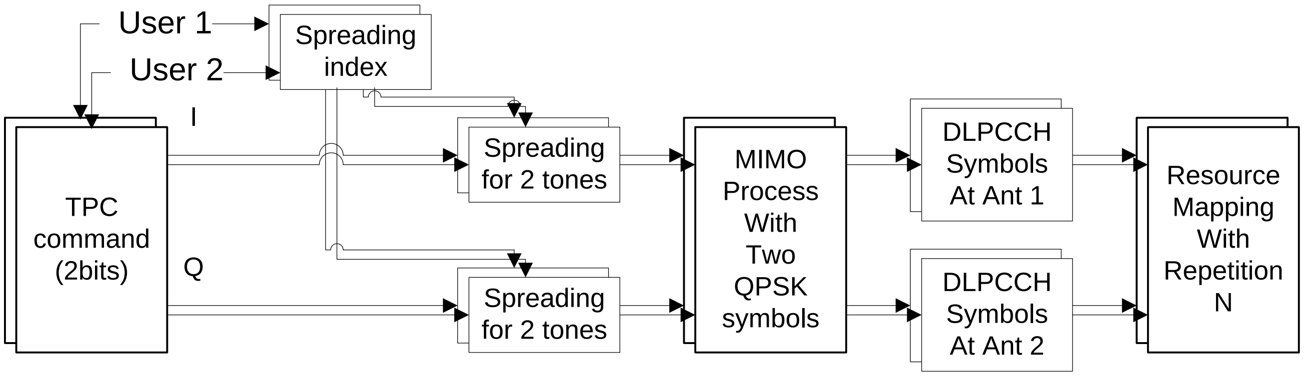
- Required Repetition N (example)
  - Assumptions
    - Reference SNR of 0dB boosting : 50% user
    - For given geometry of ISD 1.5km, approx. 2.5dB is necessary for 0dB boosting
  - To obtain 2.5dB of Rx SNR for 0dB boosting
    - two repetition is required to satisfy 10% SER
  - Repetition information is sent in BCH





Conclusions and Text Proposal

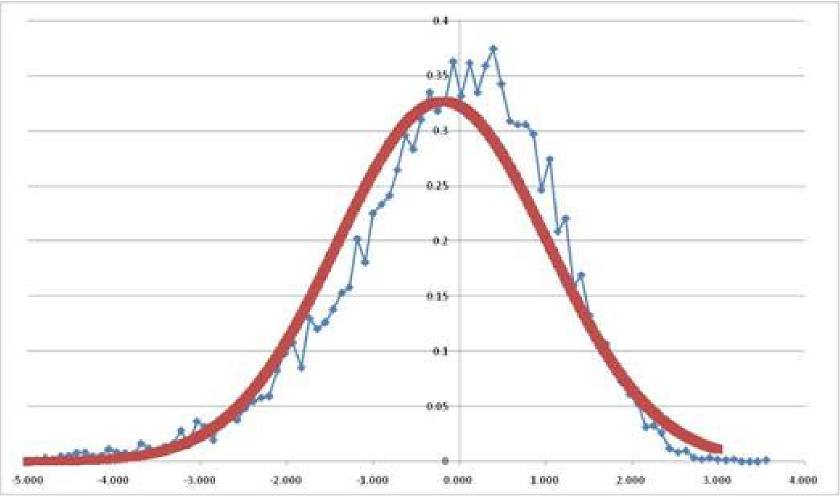
- TPC Command Step Size
  - 2 bit
  - Tx MIMO scheme : SFBC
  - Block diagram for TPC command symbol
  - User multiplexing : Max 2 user CDM



- Text Proposal
  - See C80216m-09/0208

Appendix A

- Uplink Channel Estimation Error Model
  - Reference signal for uplink channel estimation : 802.16e CQICH's pilots
  - Assumption of CQICH operating SNR : 0dB



  - Channel power estimation error can be modeled as Gaussian (0,1.3) in dB scale

* Refer to Appendix A for estimation error modeling

Appendix B

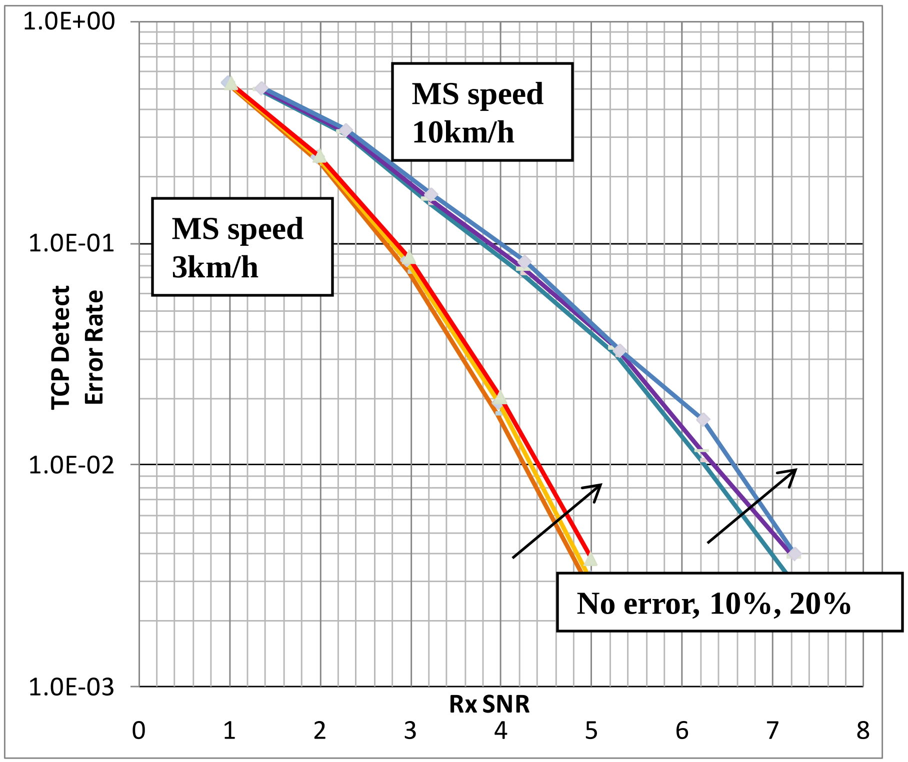
- TPC Command Step Size
  - As step size is smaller, the accurate adjustment is possible
  - As step size is larger, the fast adaptation to power fluctuation is possible

  - P802.16Rev2/D8 provides a requirement of power control algorithm, saying *"The power control algorithm shall be designed to support power attenuation due to distance loss or power fluctuations at rates of at most 30 dB/s"*
  - This can be interpreted as that maximum adaptation rate is 0.03dB/1ms
  - If the period of TPC command transmission is 20ms, then max. size of step should be 0.6dB.

  - Therefore, step size of 0.5dB is a reasonable assumption.

Appendix C

- Effect of TPC Detection Error



- Simulation Conditions
  - Nep : 480
  - Code rate : 1/2 Repetition : no
  - Number of Rx Antenna : 2, MRC
  - MS speed : 3km/h, 10km/h
  - Channel : Ped A
  - Delay btw estimation & Tx: 5ms
  - Estimation error model : Normal(0,1.3)*
  - TPC step size : 0.5dB
  - TPC bits : 2bits → (-0.5, 0, 0.5, 1)

→ TPC error rate is not very critical in typical UL transmission scenario (within 0.5dB)