| | |
|---|---|
| Project | **IEEE 802.16 Broadband Wireless Access Working Group** <http://ieee802.org/16> |
| Title | **Clarifications for the DL Control TBCC section of the IEEE 802.16m Amendment Working Document** |
| Date Submitted | **2009-07-06** |
| Source(s) | Vip Desai, Fred Vook E-mail: fred.vook@motorola.com<br>Motorola |
| Re: | IEEE 802.16m-09/0028r1 – Call for comments on IEEE 802.16m Amendment Working Document |
| Abstract | The contribution proposes some clarifications for the DL control channel coding portion of the specification. |
| Purpose | To be discussed and adopted by TGm for the 802.16m Amendment Working Document. |
| Notice | *This document does not represent the agreed views of the IEEE 802.16 Working Group or any of its subgroups*. It represents only the views of the participants listed in the "Source(s)" field above. It is offered as a basis for discussion. It is not binding on the contributor(s), who reserve(s) the right to add, amend or withdraw material contained herein. |
| Release | The contributor grants a free, irrevocable license to the IEEE to incorporate material contained in this contribution, and any modifications thereof, in the creation of an IEEE Standards publication; to copyright in the IEEE's name any IEEE Standards publication even though it may include portions of this contribution; and at the IEEE's sole discretion to permit others to reproduce in whole or in part the resulting IEEE Standards publication. The contributor also acknowledges and accepts that this contribution may be made public by IEEE 802.16. |
| Patent Policy | The contributor is familiar with the IEEE-SA Patent Policy and Procedures:<br><http://standards.ieee.org/guides/bylaws/sect6-7.html#6> and<br><http://standards.ieee.org/guides/opman/sect6.html#6.3>.<br>Further information is located at <http://standards.ieee.org/board/pat/pat-material.html> and <http://standards.ieee.org/board/pat>. |

# Clarifications for the DL Control Channel Coding section of the IEEE 802.16m Amendment Working Document

*Vip Desai, Fred Vook*

**Motorola**

## 1. Introduction

The contribution proposes some editorial modifications and technical clarifications to Section 15.3.6.3.3 – "Tail-biting convolutional code for the DL control channels"

## 2. References

[1] IEEE 802.16m-09/0010, "802.16m Amendment Working Document" (AWD)

## 3. Issues with the TBCC Description in the DL Control Section

**Section 15.3.6.3.3.1 – TBCC encoder with rate of 1/4**

This section has several issues:

The polynomial for subblock C stated in Figure 481 disagrees with the circuit for the polynomial. The corrected polynomial for subblock C should be 0165.

In Figure 481, the wiring from the last shift register is not connected to the wires entering the adders on the far right.

The operation of the encoder should be clarified.

**Section 15.3.6.3.3.3 – Subblock Interleaver**

The description for the interleaver requires clarification.

**Section 15.3.6.3.3.4 – Bit Grouping**

The description for bit grouping requires some modifications and clarifications

**Section 15.3.6.3.3.5 – Bit Selection**

The indexing for di should be 0. … 4L-1. The indexing for cj should be 0, …, M-1.

# 4. Proposed Text Modifications for the 802.16m Amendment Working Document

***[ ---------- Begin proposed text changes: ----------]***

***[MODIFICATION 1: In Figure 481, change the "C[175]" to "C[165]" ]***

***[MODIFICATION 2: Add the following text at the end of Section 15.3.6.3.3.1 – TBCC Encoder with rate of 1/4]***

The input sequence is denoted by $u[0],...,u[L-1]$

$$y^A[k]=u[k-6]+u[k-3]+u[k-2]+u[k-1]+u[k]$$

$$y^B[k]=u[k-6]+u[k-5]+u[k-3]+u[k-2]+u[k]$$

$$y^C[k]=u[k-6]+u[k-4]+u[k-2]+u[k-1]+u[k]$$

$$y^D[k]=u[k-6]+u[k-5]+u[k-4]+u[k-3]+u[k]$$

for k=0, …, L-1, where the superscripts "A", "B", "C", and "D" denote the output from each particular encoder.

The initial state is given by $u[k]=u[L+k] \quad \text{for} \quad k=-6,\ldots,-1$

***[MODIFICATION 3: In the Section heading for Section 15.3.6.3.3.2 – Change "Bit Seperation" to Bit "Separation"]***

***[MODIFICATION 4: Add the following text at the end of Section 15.3.6.3.3.3 – Subblock Interleaver***

The output for the subblock interleaver, $z^i[k]$ i=A, B, C, D and for k=0, …, L-1 is related to the input $y^i[k]$,

$$z^i[j_k]=y^i[k]$$

where the interleaver j is a function of the interleaver index function $\Pi_k$

$$\Pi_k=(15k+32k^2)\bmod 128.$$

and the number of bits L.

***[MODIFICATION 5: Add the following text at the end of Section 15.3.6.3.3.4 – Bit Grouping]***

The subblock interleaver output sequence shall consist of the interleaved A and B subblock sequences, followed by interleaved C, and D subblock sequences.

Let the bit grouping output be denoted as $w[k]$ for $k = 0,\ldots,4L-1$ and the inputs be denoted as $z^A[k]$, $z^B[k]$, $z^C[k]$, and $z^D[k]$ for $k = 0,\ldots,L-1$. The relation between the input and output is given by

$$w[2k] = z^A[k],$$

$$w[2k+1] = z^B[k],$$

$$w[2k+2L] = z^C[k],$$

and

$$w[2k+2L+1] = z^D[k].$$

***[MODIFICATION 6: Make the following changes to Section 15.3.6.3.3.5 – Bit Selection]***

***[ On line 46, page 192: change* “i=0,1,…,4L” *to* “i=0,1,…,4L-1” ]**

***[ On line 48, page 192: change* “j=0,1,…,M” *to* “i=0,1,…,M-1” ]**

***[ ---------- End Proposed Text ----------]***