10GBASE-T Line Signaling

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Line Signaling Requirements

- Meet 10 Gb/s over a UTP CAT5e/6 channel with $BER=10^{-10}$
- Backward compatible with 1000BASE-T
  – Launch voltage of 2 V_{p-p}
  – Base-band signaling (no modulation)
  – Scrambling used to spread the TX spectrum
- Meet the EMI specification for emitted power (FCC Class A)

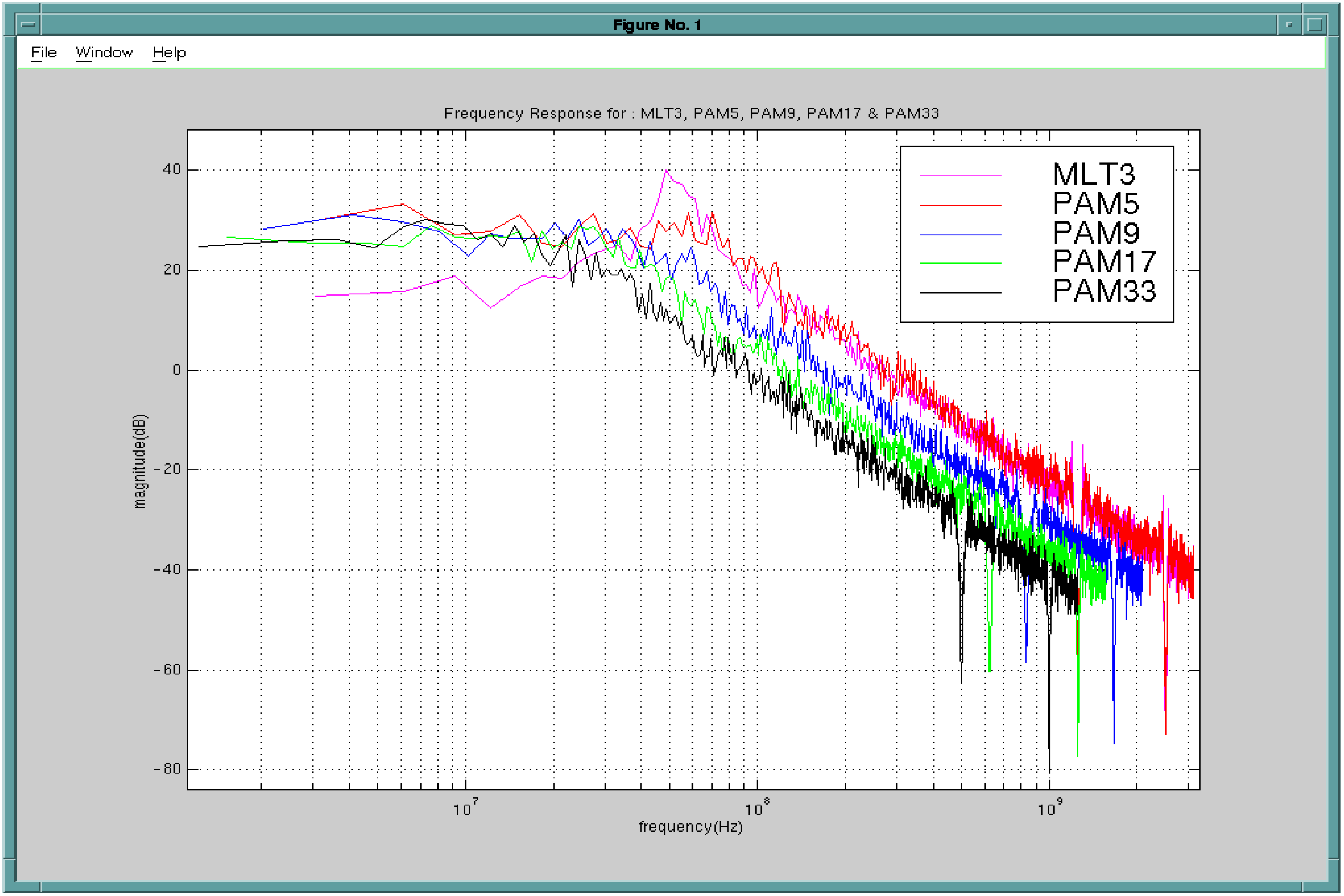
PAM signal requirement at BER = 10^{-10}

Line Code	bits/Baud	Signal bandwidth (MHz)	Baud rate (MS/s)	Detection SNR (dB)
MLT-3	1	1250	2500	21.01
PAM-5	2	625	1250	25.43
PAM-9	3	416	833	30.52
PAM-17	4	312.5	625	36.02
PAM-33	5	156.25	312.5	41.77

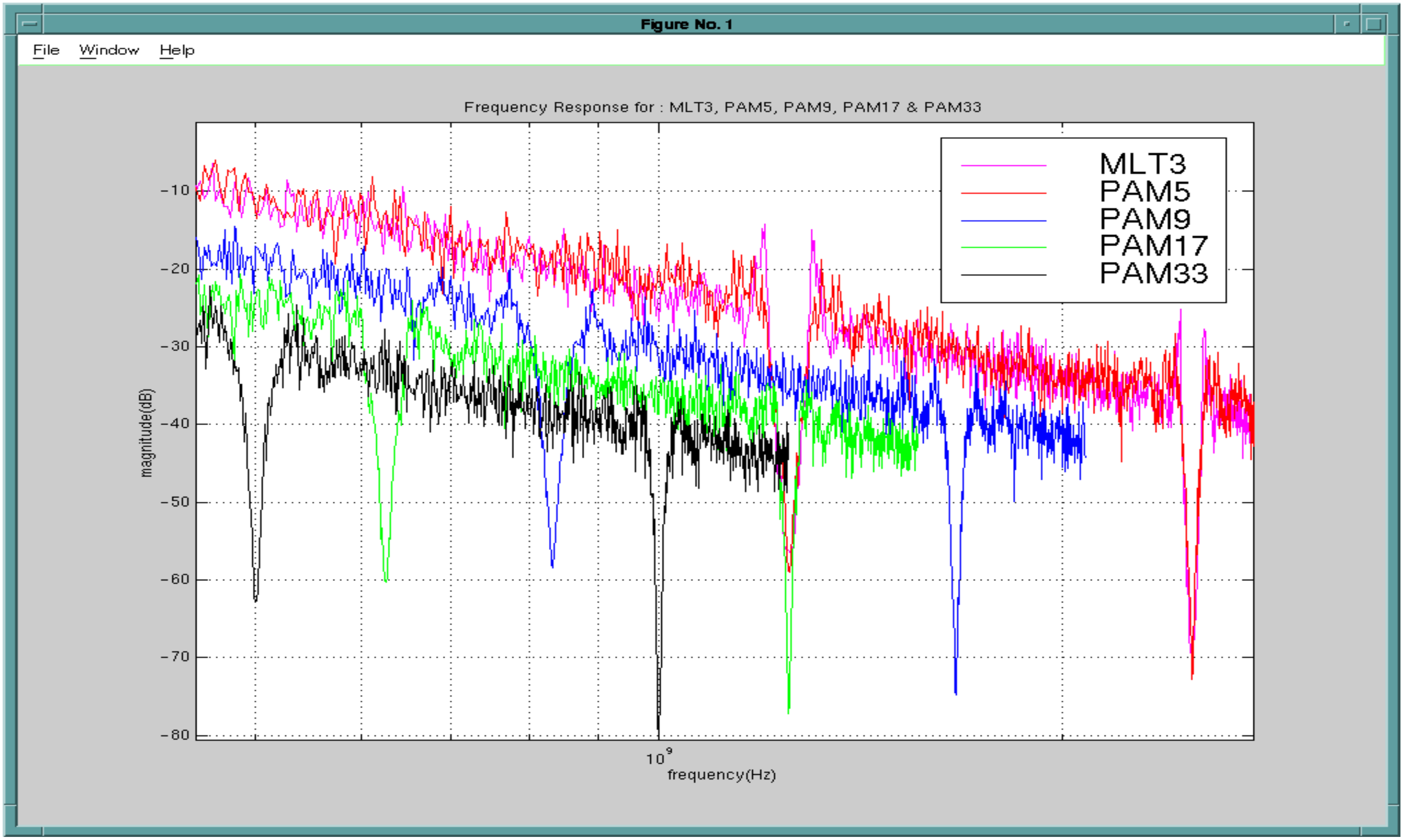
$$\mathrm{SNR} = 6\log_2(M) + \mathrm{Gap} - \mathrm{Coding\_Gain} + \mathrm{Margin}$$

Gap = 11.5dB   Coding_Gain = 6dB   Margin = 6dB

Spectrum of various Line Coding



Various Line Code Notches



Line Signaling Conclusions

- MLT-3 line-signal (used in 100BASE-T) causes considerable peaking around the pass-band and the notches
- PAM-5 requires the lowest detection SNR
- PAM-5 line-signal has been used before (100BASE-T2 & 1000BASE-T)
- PAM-5 allows line-signal's baud-rate to be a multiple of XGMII's baud-rate (not true of PAM-9 & PAM-33)

Class-E 4-Connector Channel Model

$$IL = 1.9910\sqrt{f} + 0.0177f + \frac{0.2625}{\sqrt{f}}$$

$$PSNEXT = 20\log\left(10^{\frac{72.3-15\log f}{20}} + 2\times10^{\frac{90-20\log f}{20}}\right)$$

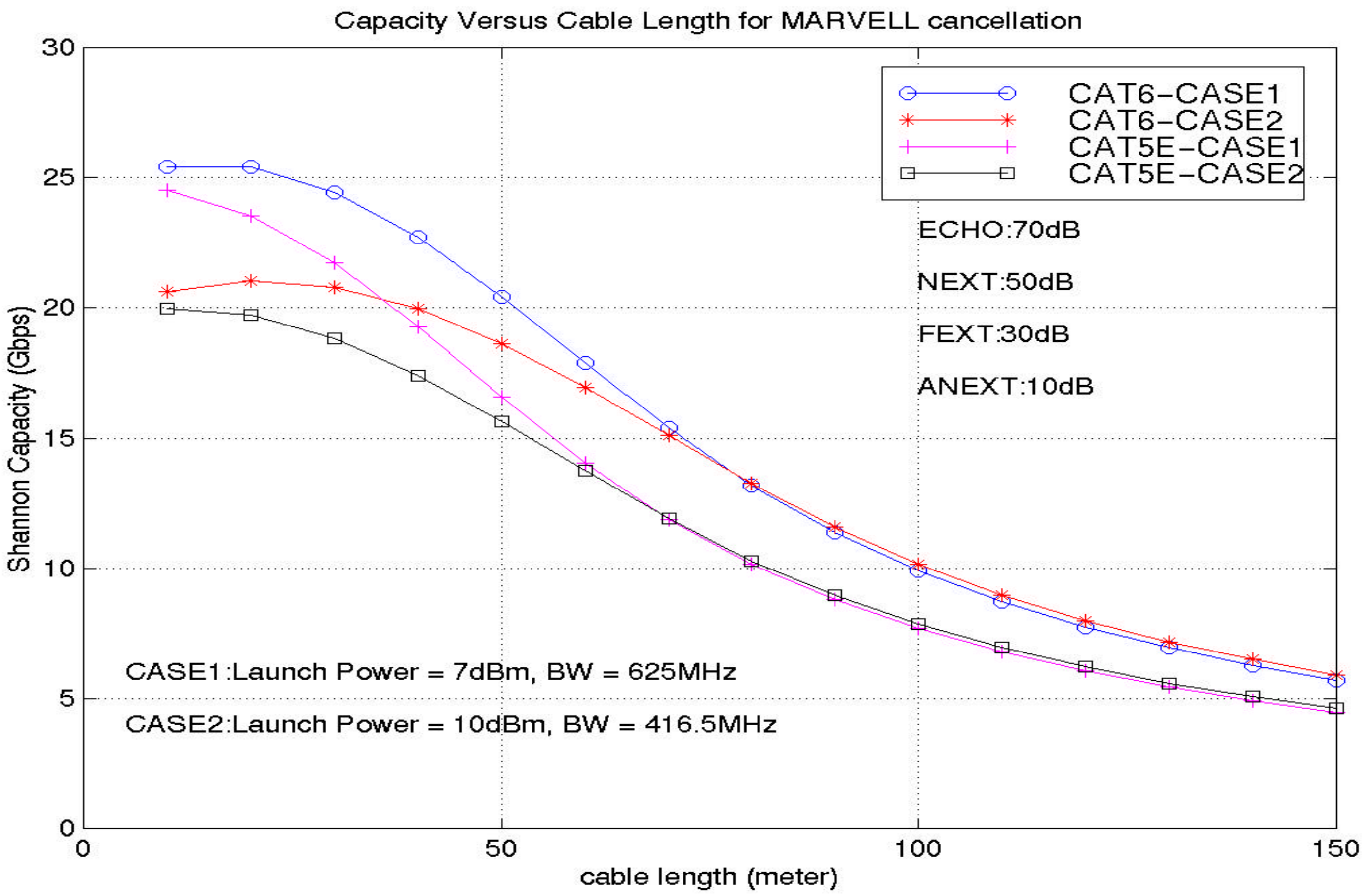
$$PSELFEXT = 20\log\left(10^{\frac{64.8-20\log f}{20}} + 4\times10^{\frac{80.1-20\log f}{20}}\right)$$

$$ANEXT = 41.1 - 15\log\left(\frac{f}{100}\right)$$

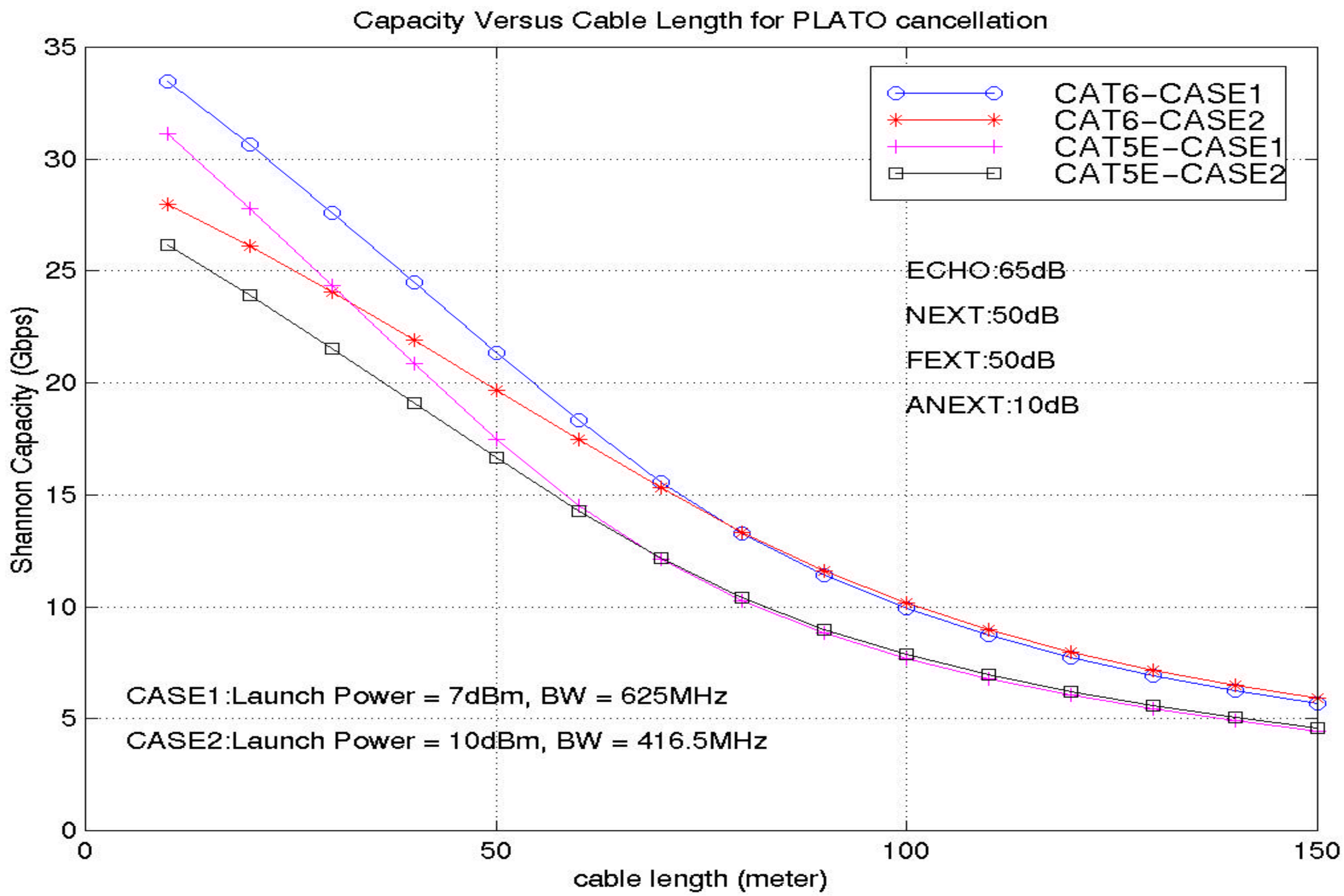
$$RL = 32 - 10\log(f)$$

$$NOISE = -140\frac{dBm}{Hz}$$

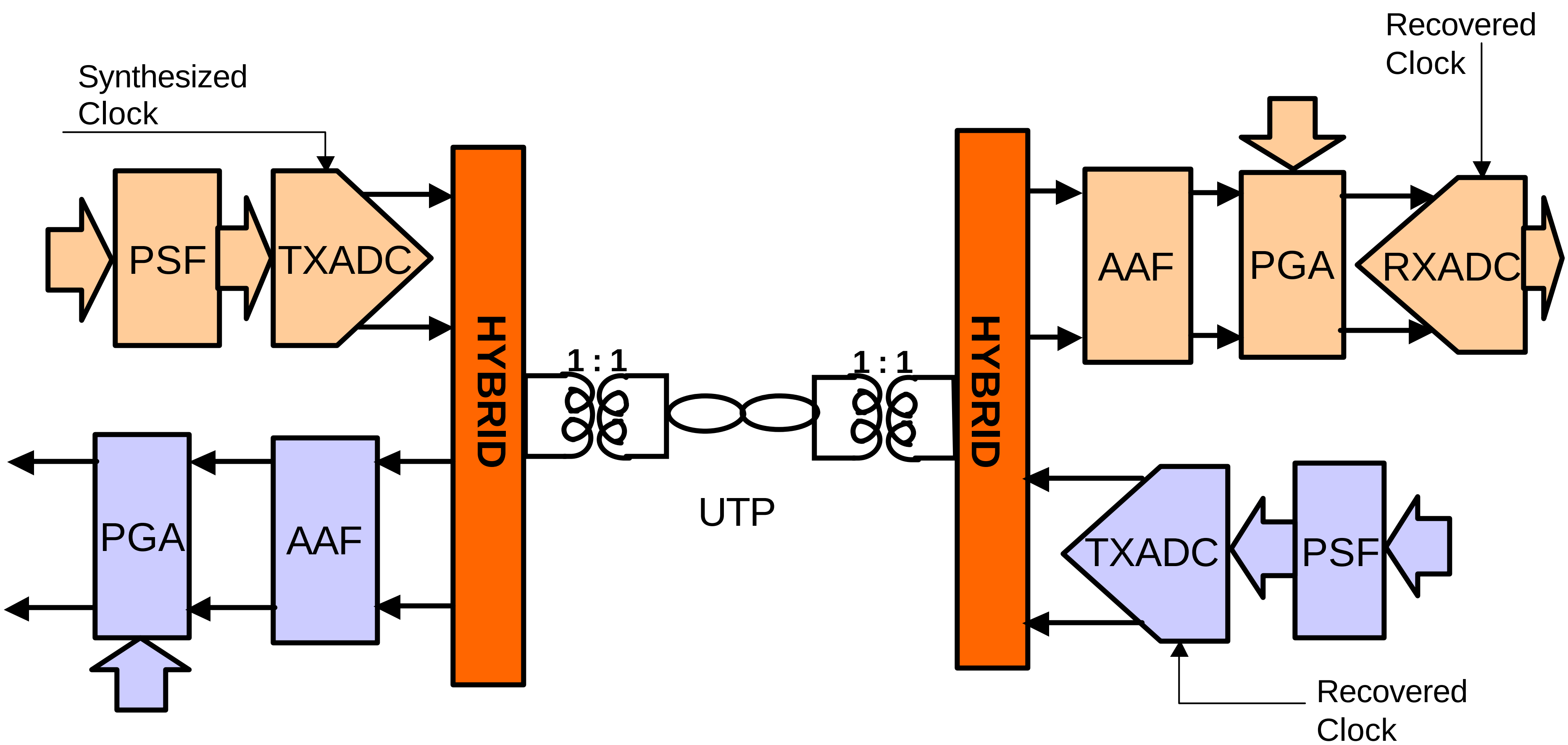
Rate-reach Using Cancellation Option1



Rate-reach Using Cancellation Option2



Analog Front End (AFE) model for DSP Solution



Assumptions for AFE Linearity Analysis

- **2 V_p peak-to-peak PAM-M launch signal**
- **Analog differential blocks have only odd non-linearity**
- **Analog blocks are characterized by:**

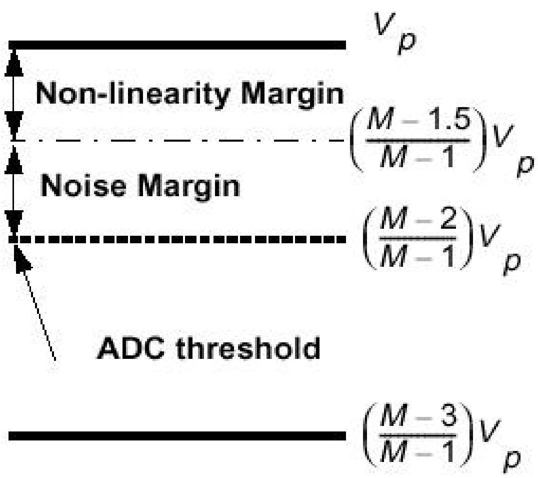
$$\mathbf{Y = b X(1+a X^2)}$$

- b **block gain**
- a **3rd order non-linearity coefficient**

Worst-case Non-linearity Error (0m)

1-When l (cable length)=0 for all analog blocks β=1. ADC input becomes:

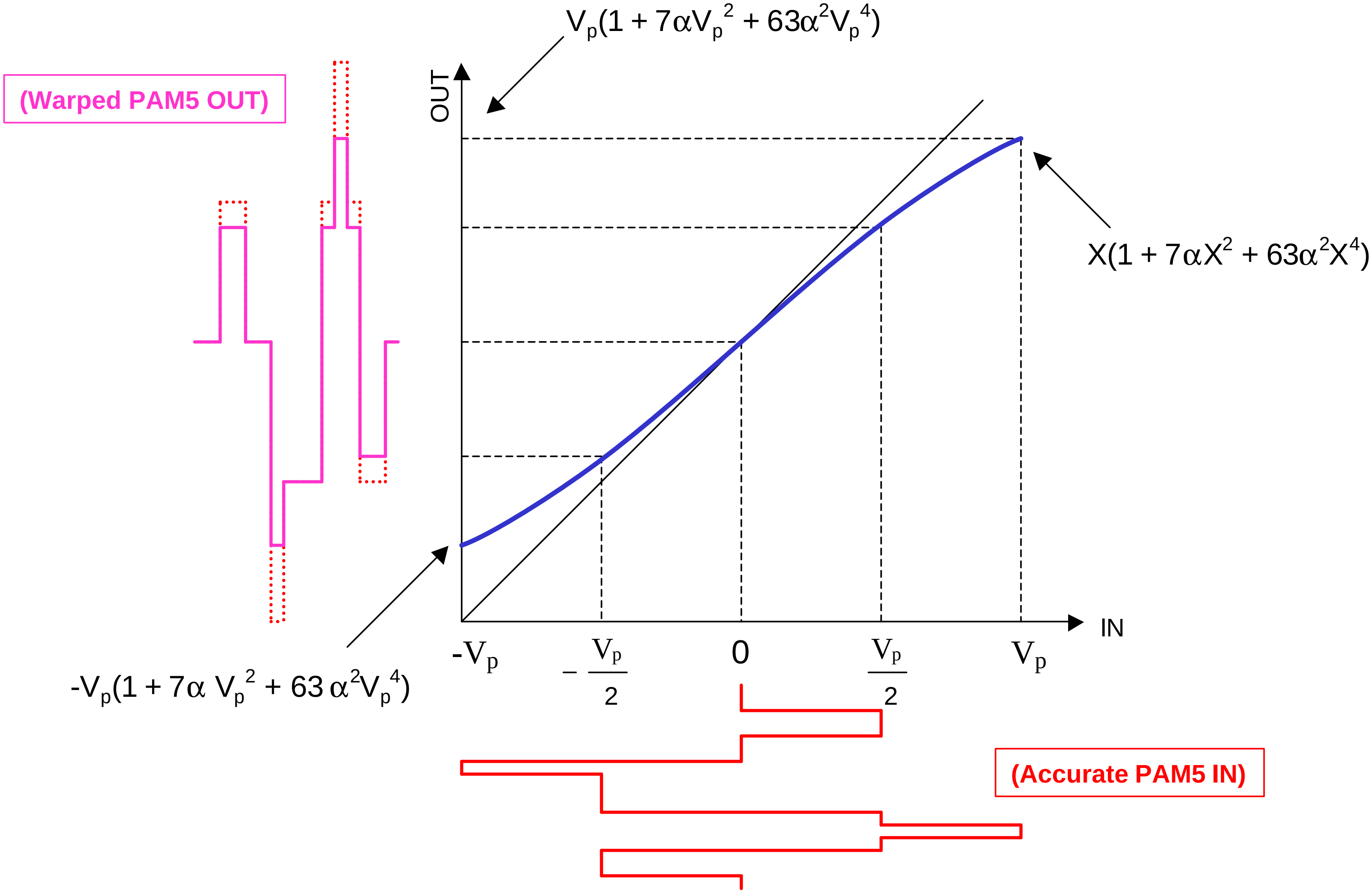
$$Y = X(1 + 7\alpha X^2 + 63\alpha^2 X^4) = X + error$$



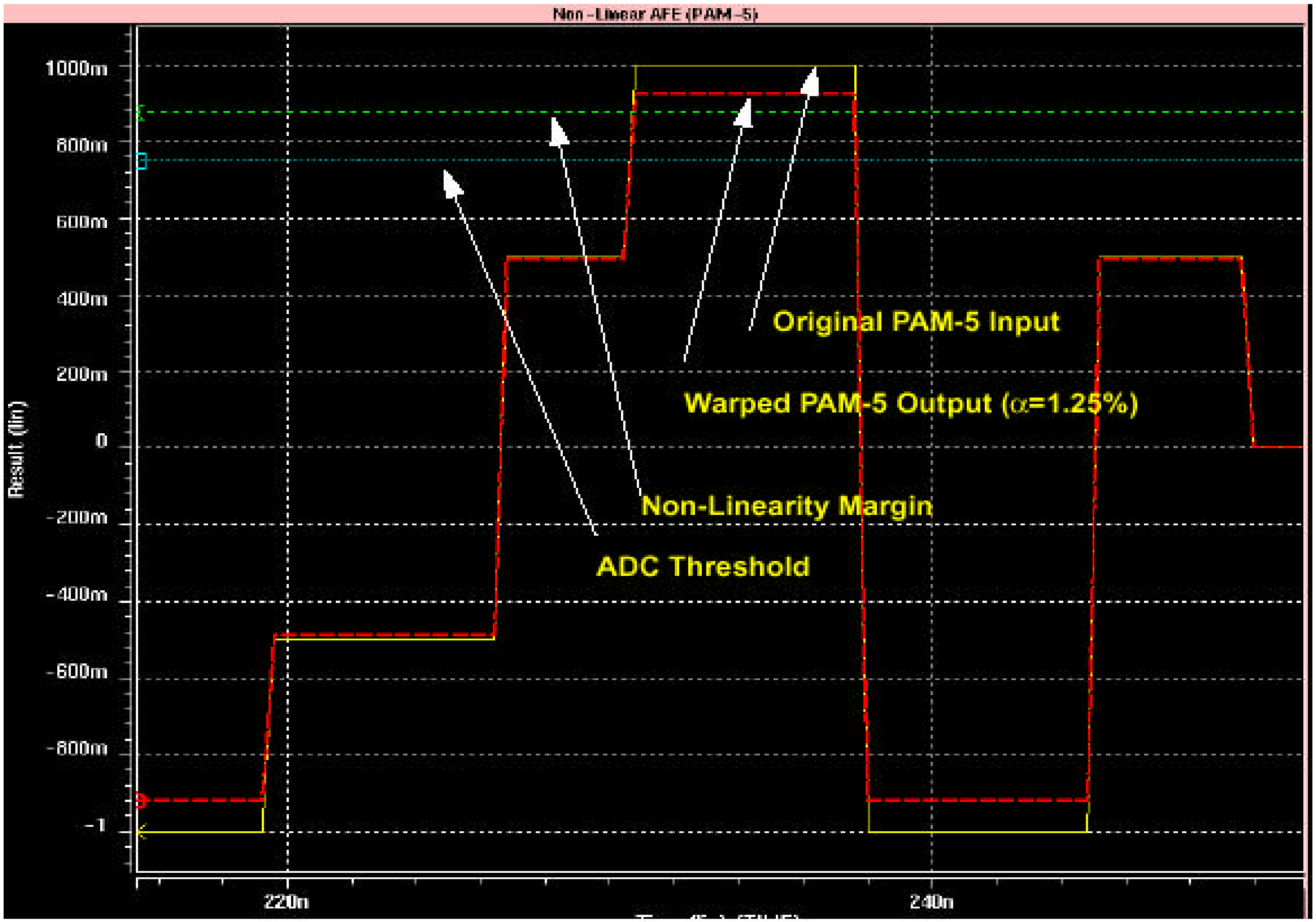
$$error \le \frac{V_p}{2(M-1)}$$ (non-linearity margin)

$$|\alpha| \le \frac{1}{14.4(M-1)V_P^2}$$

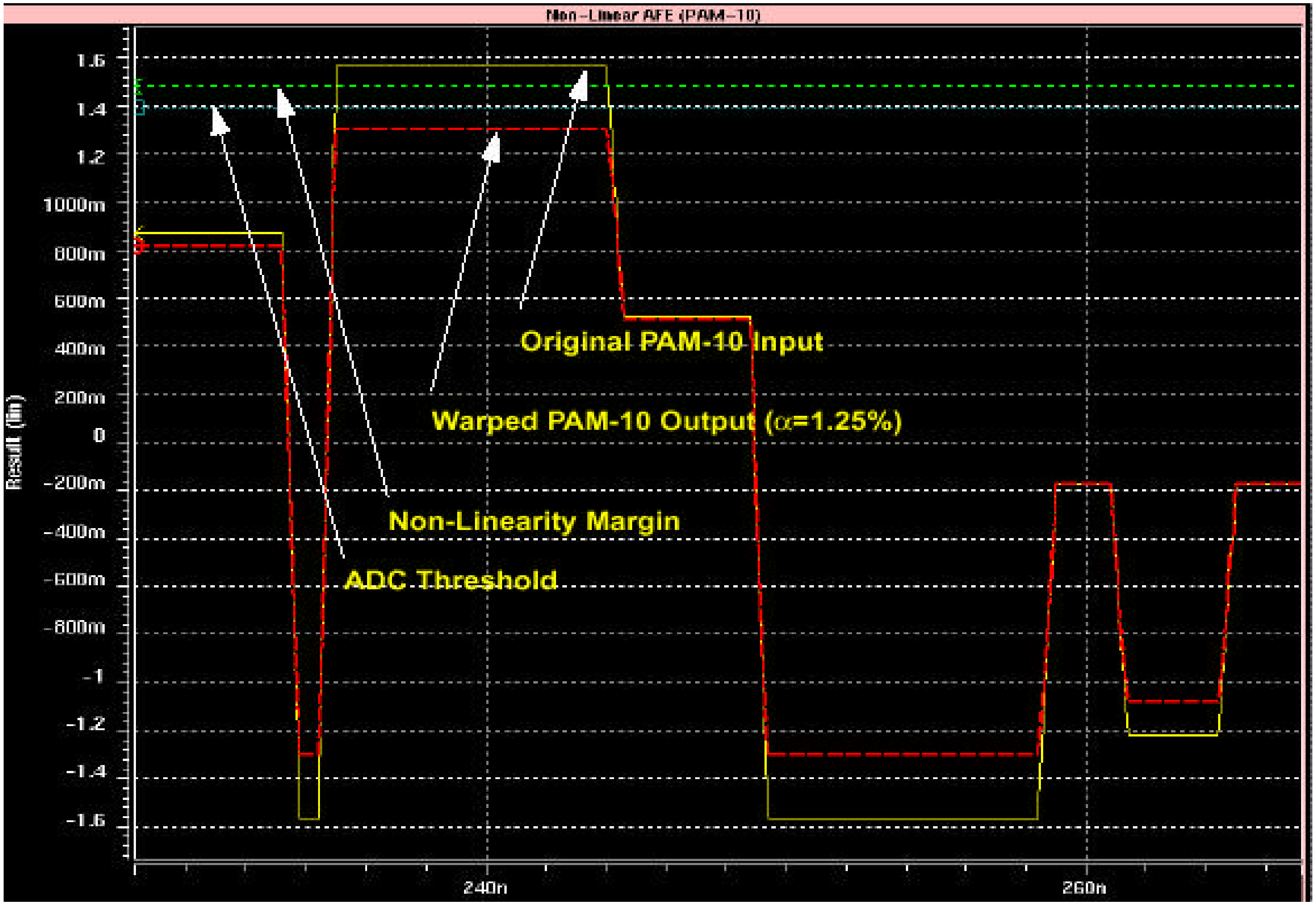
Combined AFE Non-linearity (7 blocks)



Non-linear AFE (PAM-5)



Non-linear AFE (PAM-10)



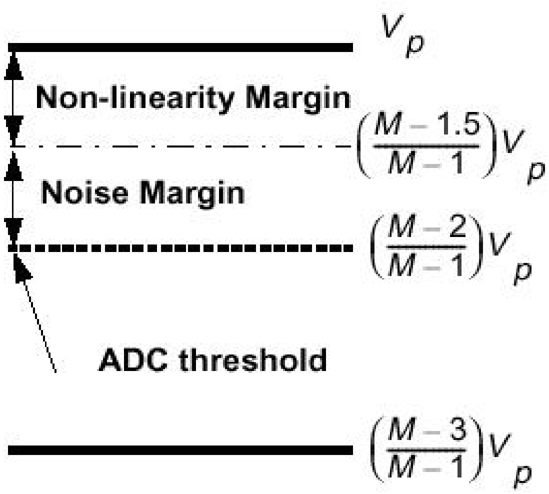
AFE Linearity Requirement vs. Line-Signal

Line Code	Peak-to-Peak (V)	Launch Power (dBm)	$\|a\|$ Formula (%)	$\|a\|$ Simulation (%)	Distortion ADC input (dB)
PAM-5 (Plato Labs)	**2.000**	**7.00**	**1.74**	**2.00**	**31.0**
PAM-10 (Solar Flare)	**3.134**	**10.00**	**0.31**	**0.35**	**44.5**
PAM-17 (Cicada 1/00)	**2.000**	**5.74**	**0.43**	**0.45**	**42.3**

Worst-case Non-linearity Error (100m)

1-When l=100 m for 1st six analog blocks β=1, for PGA β=2.08. Then:

$$Y = 2.08X(1 + 7\alpha X^2 + 63\alpha^2 X^4) = 2.08X + error$$



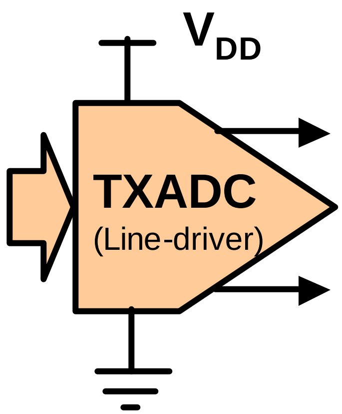
$$error \le \frac{V_p}{4.16(M-1)}$$ (non-linearity margin)

$$|\alpha| \le \frac{1}{29.12(M-1)V_P^2}$$

Non-linearity Analysis Conclusions

- **For a given PAM-M line-signal the 3rd order non-linearity coefficient (a) inversely depends on M and *square* of peak launch signal**
- **Smaller the a higher the AFE complexity (area and power)**
- **3.134V_{p-p} PAM-10 line-signal requires AFEs that are 5.7X more linear than that of 2V_{p-p} PAM-5**
- **Let's maintain 2V_{p-p} launch voltage (used in 100BASE-T and 1000BASE-T)**
- **Let's maintain PAM-5 line-signal (used in 100BASE-T2 and 1000BASE-T)**

Line-driver's Availability in Deep Sub-micron CMOS Process



$$(V_{Launch})_{pp}=2(V_{DD}-2V_{Headroom})$$

Process (CMOS)	Core Channel Length	Core V_{DD} (V)	I/O Channel Length	I/O V_{DD} (V)	TXDAC Can Use Core Device ($2.000V_{pp}$)	TXDAC Can Use Core Device ($3.134V_{pp}$)
0.35mm	0.35mm	3.3	0.35mm	3.3	YES	YES
0.18mm	0.18mm	1.8	0.35mm	3.3	YES	YES
0.15mm	0.15mm	1.5	0.35mm	3.3	YES	NO
0.13mm	0.13mm	1.2	0.35mm	3.3	YES	NO