An Overview of Electronic Dispersion Compensation Techniques for 10-Gbit/s over FDDI Grade MMF

Draft 1.3

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IEEE 802.3 Interim Meeting
Vancouver, BC, Canada
January 2004

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- EDC Overview
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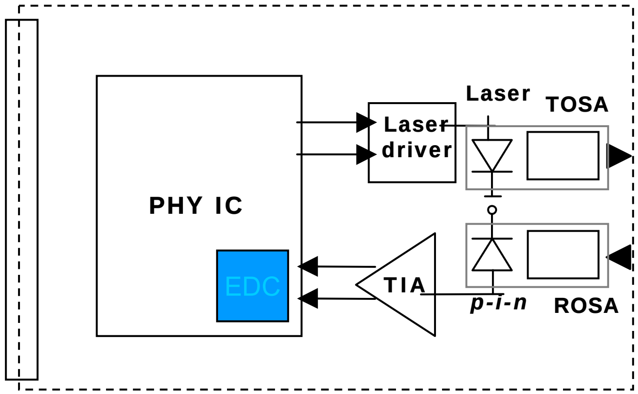
EDC Overview

Electronic Dispersion Compensation: Succinctly …



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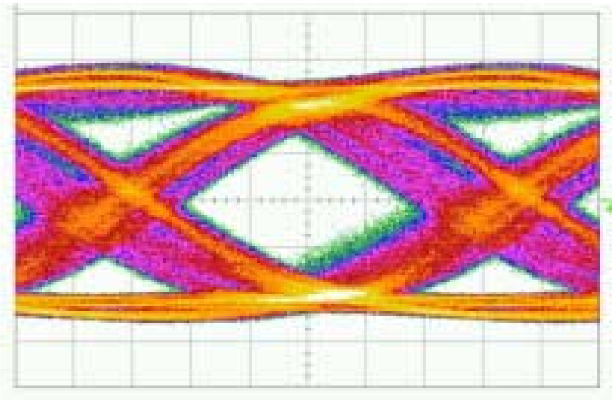
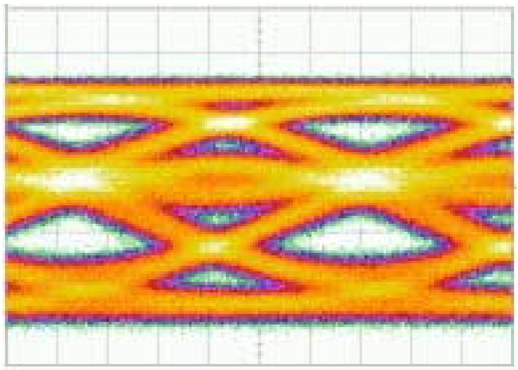


After EDC Compensation, before detection slicer …

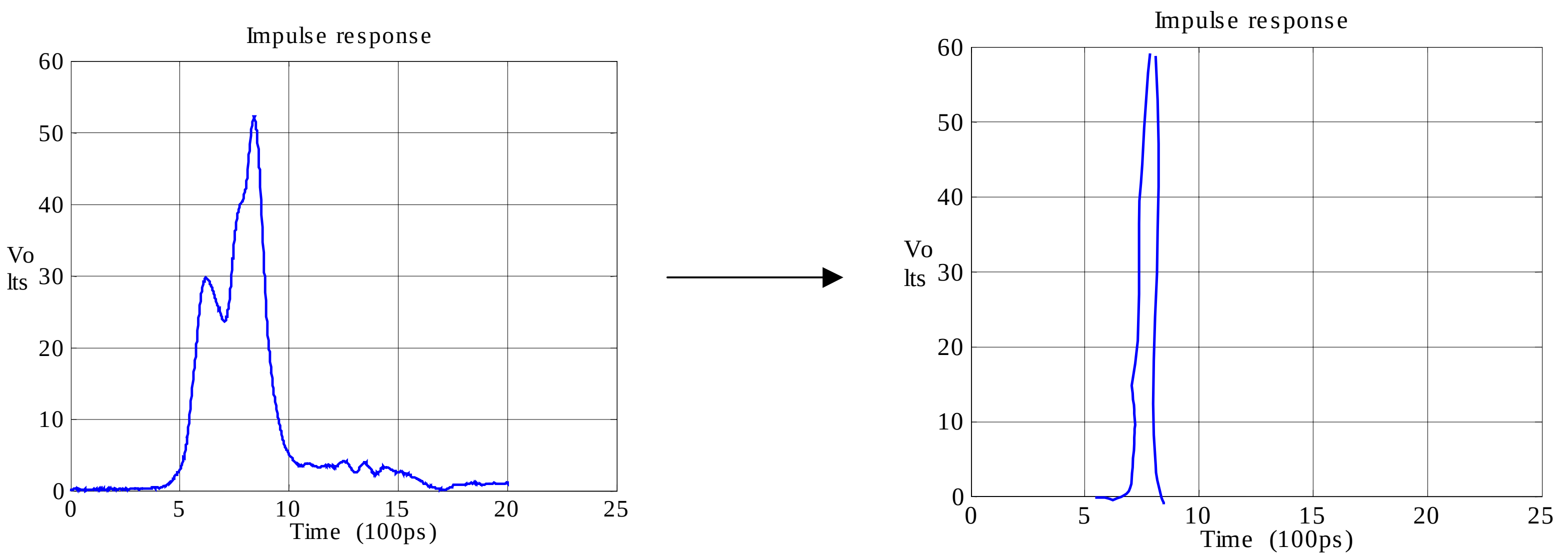
IN



10.3 Gb/s Signal after 330m over DMD-challenged MMF (DMD ~160ps), o/p from TIA (1310nm F-P)

Need for Equalization:
An Elementary Look (1)

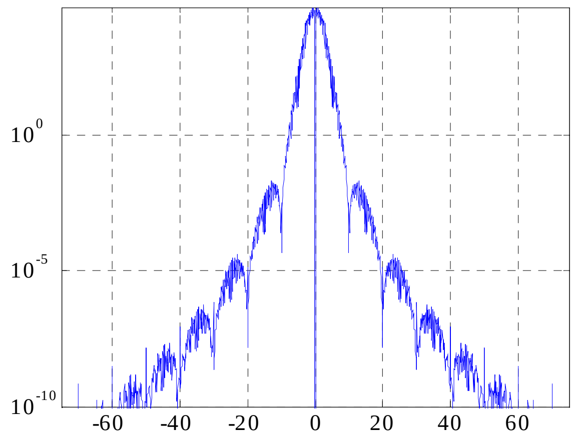
Time Domain Perspective

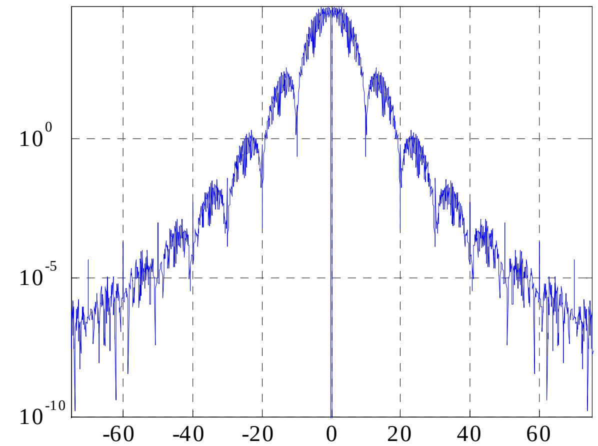


- Typical impulse response within a dispersive channel.
- Maximum ISI penalty (may be several dB loss) occurs when all interfering cursors add up negatively.
- Effective EDC ⟹ Transforms smeared pulse to impulse-like pulse

Need for Equalization: An Elementary Look (2)

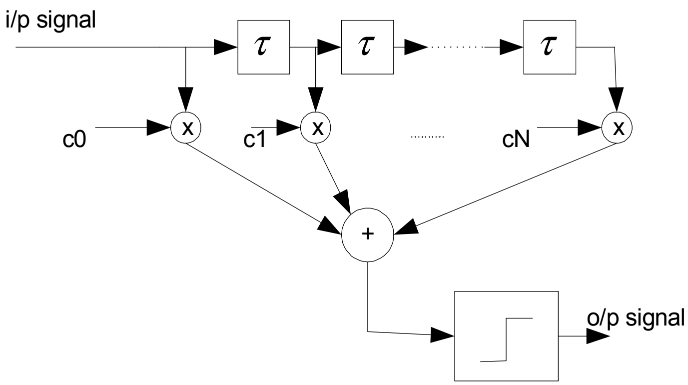
- **Frequency Domain Perspective**



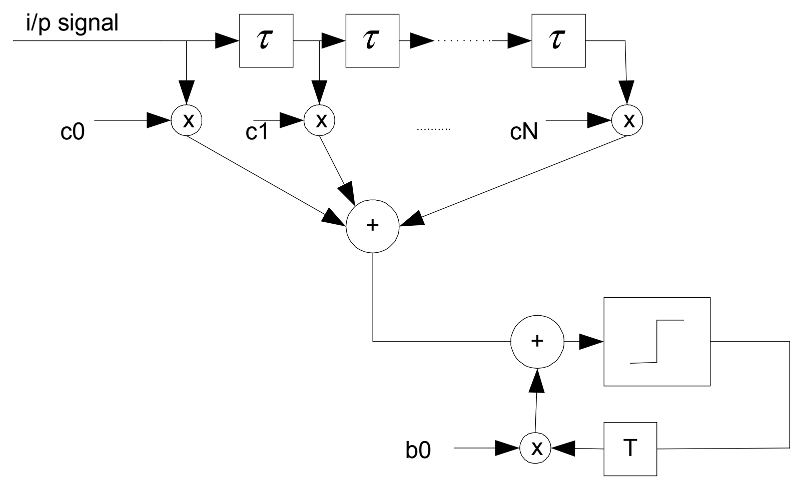


- Severe ISI, in frequency domain, leads to low frequency content in multiple signal frequencies of interest.
- Effective EDC ⟹ (1) Boosts dispersed signal spectrum to increase spectral flatness
  (2) Avoids significant noise enhancement
  (3) Optimizes system penalty in terms of residual ISI and noise

Equalization Techniques: Sample Architectures



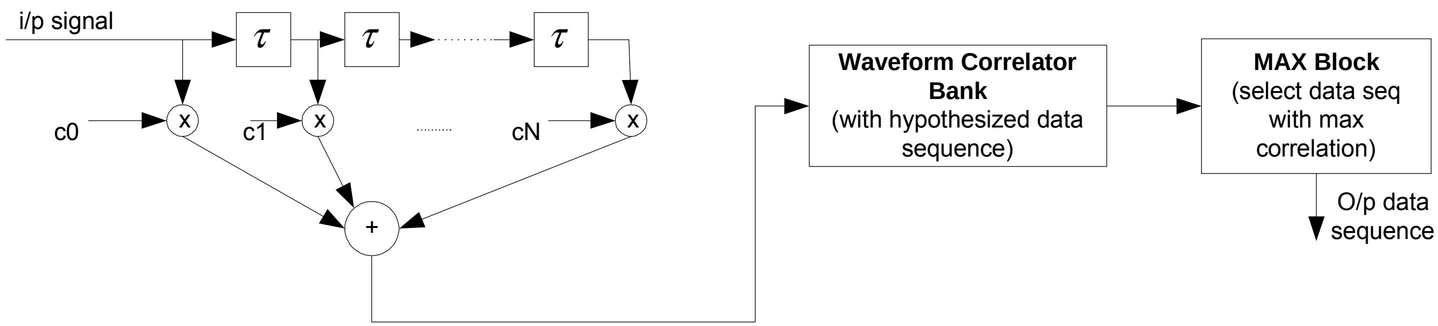
Linear Feedforward Equalizer (FIR)



Decision Feedback Equalizer

- EDC Architectures include the well-understood Feedforward Equalizer (FFE) and Decision Feedback Equalizer (DFE)
- Key design options include tap spacing within FFE filter, # of taps within FFE filter and # of feedback taps (for DFE)
- Another key issue is the adaptation criteria for adapting the multiple taps – a popular approach is LMS error-based and decision-directed

Equalization Techniques: Maximum Likelihood Sequence Detection

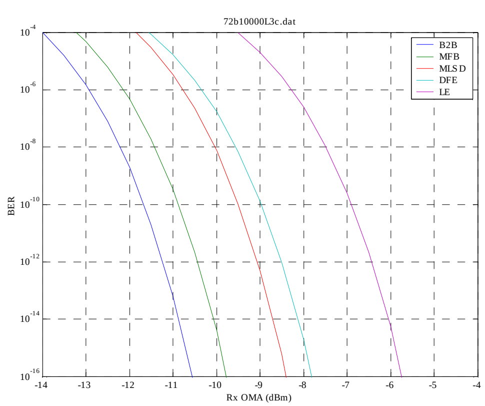


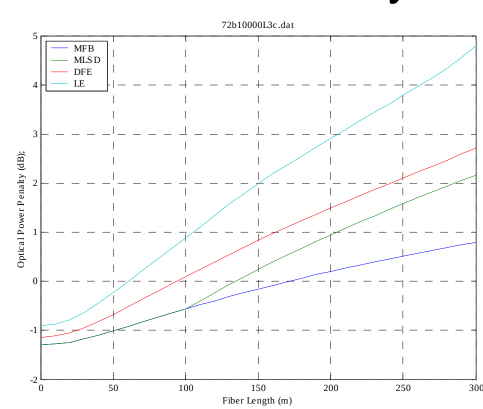
- Near-optimal approach but more challenging to implement at high speeds
- Design parameters include # of taps and tap spacing in FIR filter if used as front-end matched filter, # of hypothesized data sequences to be correlated with in the middle block.
- Other realizations for MLSD possible.
- Other architectures such as Fixed Delay Tree Search (FDTS) also have been used which can have performance/complexity trade-off between MLSD and DFE.

Specifying EDC Performance

EDC: Performance Figures of Merit

- Fundamental performance measure: Bit Error Rate (BER)
  - Can be (approximately) computed analytically
  - Target is 10^{-12}
- Presentation of BER performance
  - Waterfall Curve: Shows BER vs. Rx OMA at a particular fiber length
  - Power Penalty Plot: Shows increase in Rx OMA (relative to baseline) required to achieve target BER (10^{-12}). May have infinite power penalty in case of BER error floor
- Other important measures
  - Jitter: introduces colored amplitude noise and will degrade performance
  - Adaptation time constant: specifies how fast channel can vary





Computing BER

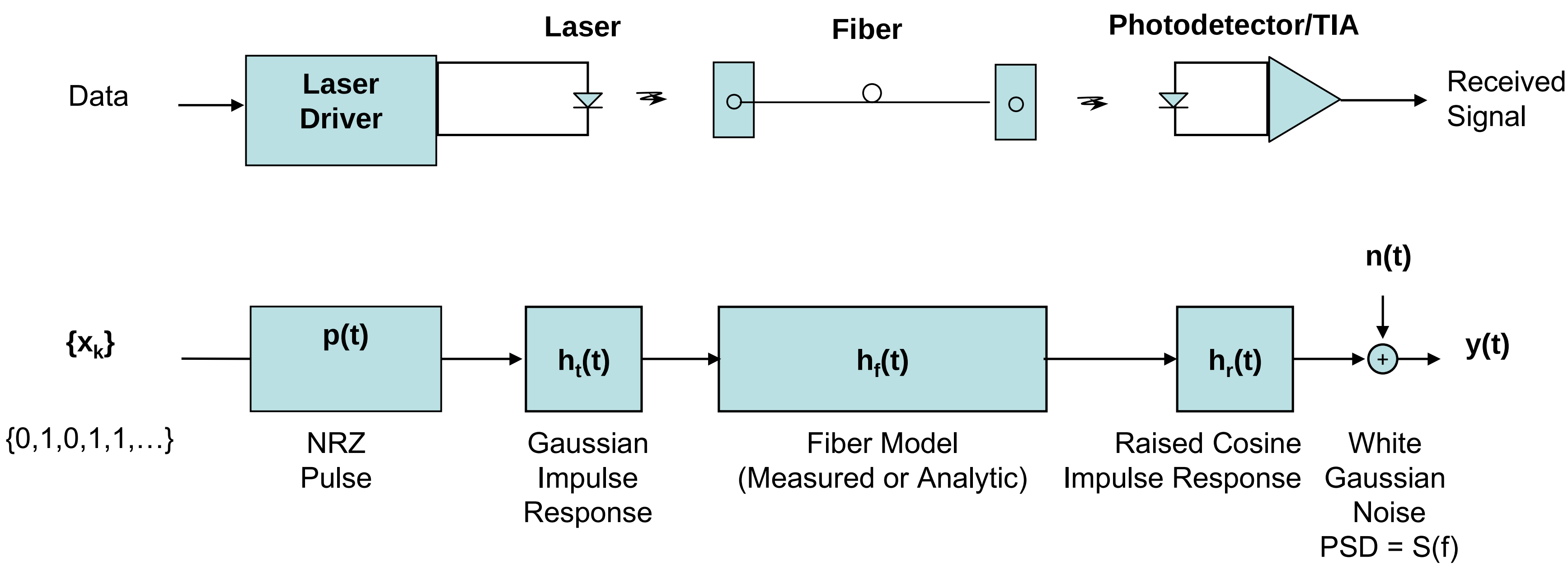
- BER can be approximated by assuming Gaussian noise and using the formula
  - BER = 0.5 * erfc (Q/sqrt(2))
  - $Q = d_{min}/2\sigma$ ($Q = 7.03$ gives $BER = 10^{-12}$)
  - d_{min} = Minimum distance between "symbols" at point where decision is made
  - σ = standard deviation (SDEV) of total noise
- d_{min}, σ depend on type of EDC
  - Unequalized case: d_{min} = worst case eye opening; σ = Rx noise SDEV
  - Equalized case: d_{min} = symbol spacing at equalizer; σ = SDEV of combined Rx noise and ISI
  - MLSD case: d_{min} = minimum Euclidean distance between all possible sequences seen by detector; σ = SDEV of Rx noise

Bounds on EDC Performance

- For this presentation we show bounds based on performance of ideal EDC structures
  - Perfect timing
  - Perfect knowledge of channel
  - Infinite complexity
- Matched filter bound (MFB)
  - Optimum "matched filter" receiver detecting a single bit (no ISI)
  - No EDC can do better for a given transmit scheme
- Linear Equalizer (LE), Decision feedback equalizer (DFE)
  - Matched filter receiver followed by infinite-length filters
  - Use minimum mean-squared error (not zero forcing) criterion
- Maximum Likelihood Sequence Detector (MLSD)
  - Unconstrained detector
  - Optimum receiver; maximizes probability of correct decision

Channel Models

Channel Model



- Laser, photodetector models are same as 802.3ae link model
- PSD of AWGN can be computed from assumed receiver sensitivity

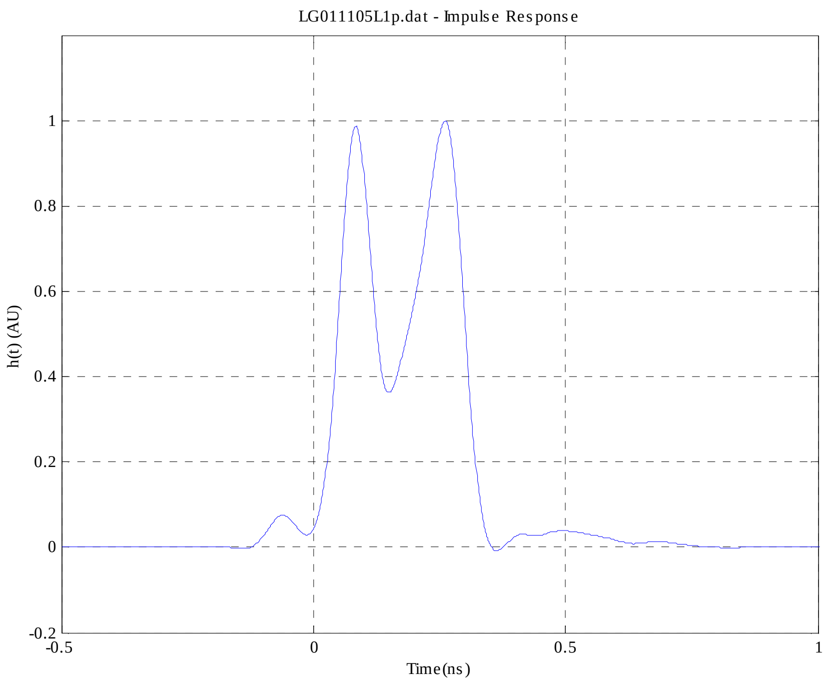
Noise Power Spectral Density

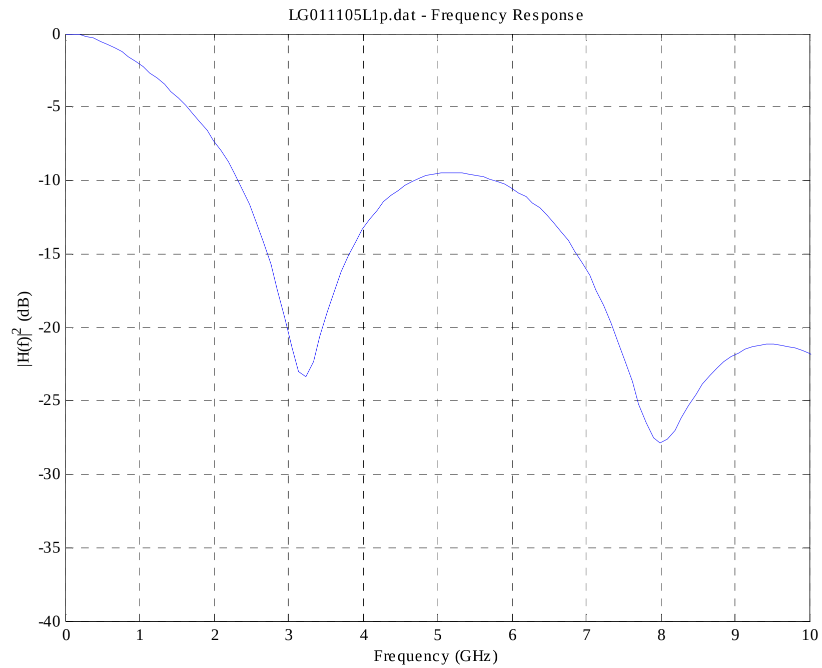
- Noise PSD S(f) assumed constant and computed from receiver sensitivity according to
  - $S(f) = S_{OMA}^2 / (8\ Q_0^2\ B_n)$, where
    - S_{OMA} = Sensitivity in OMA
    - $Q_0 = 7.03$ for BER = 10^{-12}
    - B_n = Noise equivalent bandwidth
  - S(f) is referred to optical domain; hence units are mW^2/GHz
- IEEE 802.3ae LR link model specifies
  - $S_{OMA} = -12.6$ dBm
  - B = 7.725 GHz (3-dB electrical BW)
  - $B_n = 1.032*B$
- Thus
  - $S(f) = 9.63 \times 10^{-7}\ mW^2/GHz$

Measured Fiber Responses

- Measured impulses from the 802.3z National Lab set of fibers
  - http://www.ieee802.org/3/z/mbi/index.html
- Fibers that had a modal bandwidth of ~500 MHz-Km were considered
- 3 fibers were chosen as representative “worst case” candidates
  - Equal power split which causes notch in spectrum
  - High DMD fiber and marginal modal bandwidth
  - Single wide pulse with monotonic frequency rolloff
- Transmit pulse was deconvolved from the measured impulse response
- Measured impulse responses were rescaled in time to simulate different fiber lengths

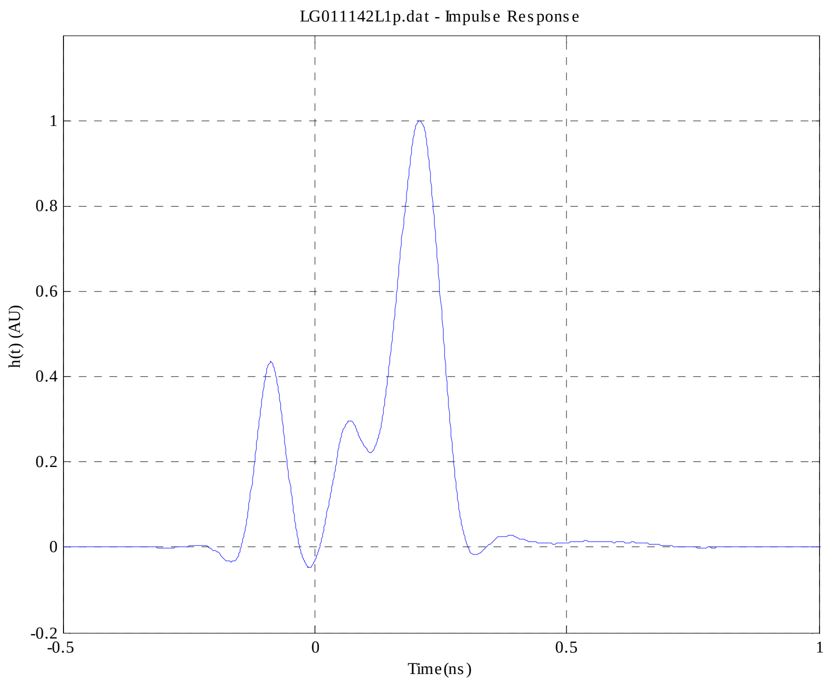
Fiber 1 - Equal Power Split

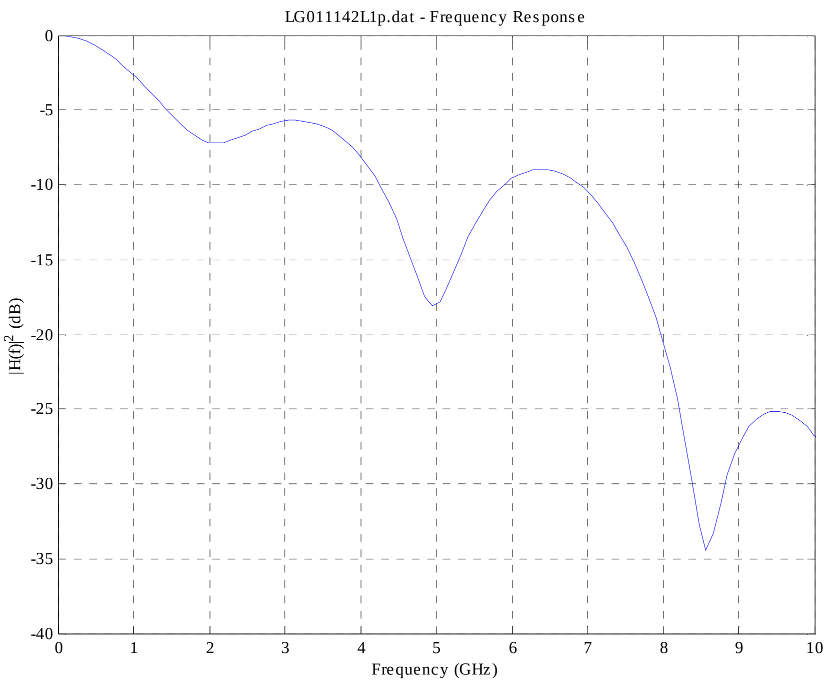




- LG011105L1p.dat - equal power split channel with a DMD of 260ps on a 457m fiber.
- Scaled to 300m

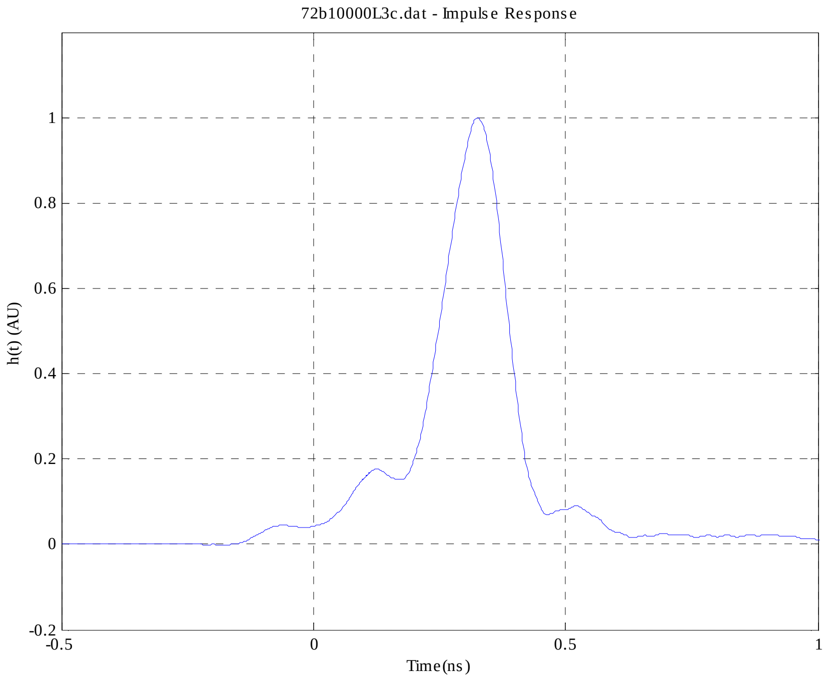
Fiber 2 - Worse DMD

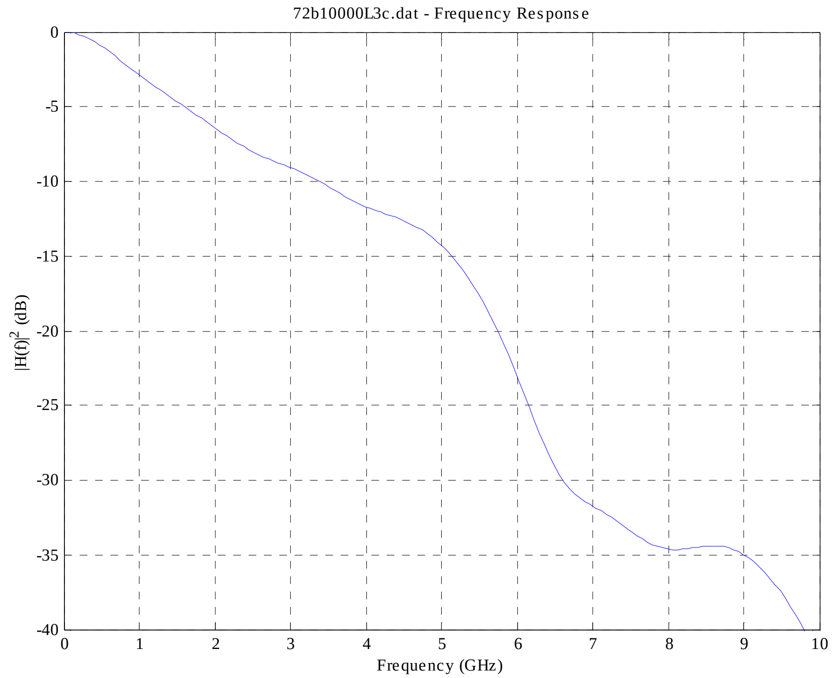




- LG011142L1p.dat - DMD of approximately 450ps on a 457m fiber
- Scaled to 300m

Fiber 3 - Single Pulse





- 72b10000L3c.dat - Single time-domain pulse with monotonic rolloff (no notches) in frequency domain
- Scaled to 300m

Additional Channel Impairments

- Relative Intensity Noise (RIN)
  – Due to fluctuations in laser intensity.
- Modal Noise
  – Time-varying ISI effect due to mode-selective components within link.
- Mode Partition Noise
  – Due to longitudinal and/or transverse modes in the laser sources.
- Interferometric Noise
  – Caused by reflections at optical interface.
- Jitter (random and deterministic)

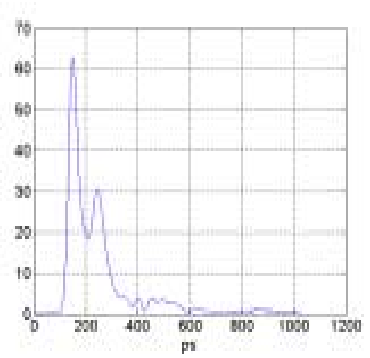
- All must be considered, but ISI penalty will dominate performance

Channel Model Abstraction for MMF

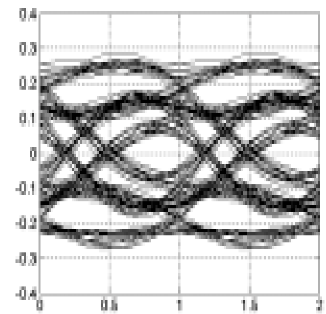
- Channel models easily simulated and/or for lab use that can closely resemble "worst-case" MMF channels
  - Reduce infinitude of possibilities to small # of parameters
  - Applications: use within lab-based or simulation-based compliance tests for EDC; also for architectural design of EDC.
- Possible Channel Models:
  - M-tap FIR Model
  - LPF model
  - Gaussian Impulse Response Model
  - LPF cascaded with N-Dirac Delta Function Model

Channel Waveform Generation for MMF :

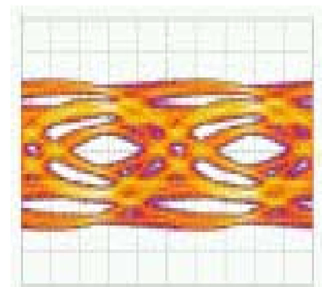
(LPF cascaded with 4-Dirac Delta Model)



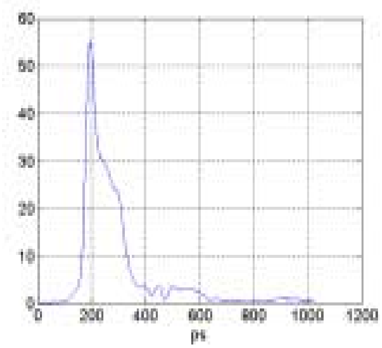
Fiber Impulse Response (N04A1002S3p.dat)



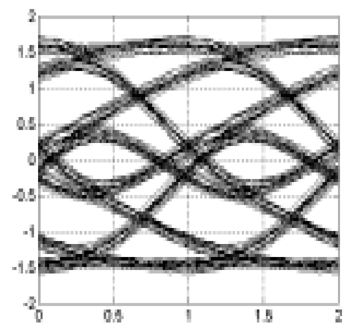
Simulated eye of waveform



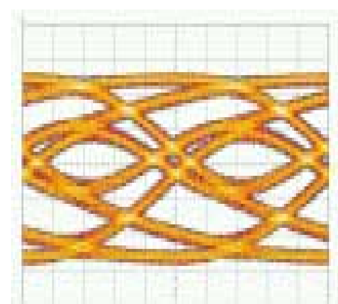
Emulated waveform eye using LPF with 4-tap FIR



Fiber Impulse Response (LG010401L4f.dat)



Simulated eye of waveform



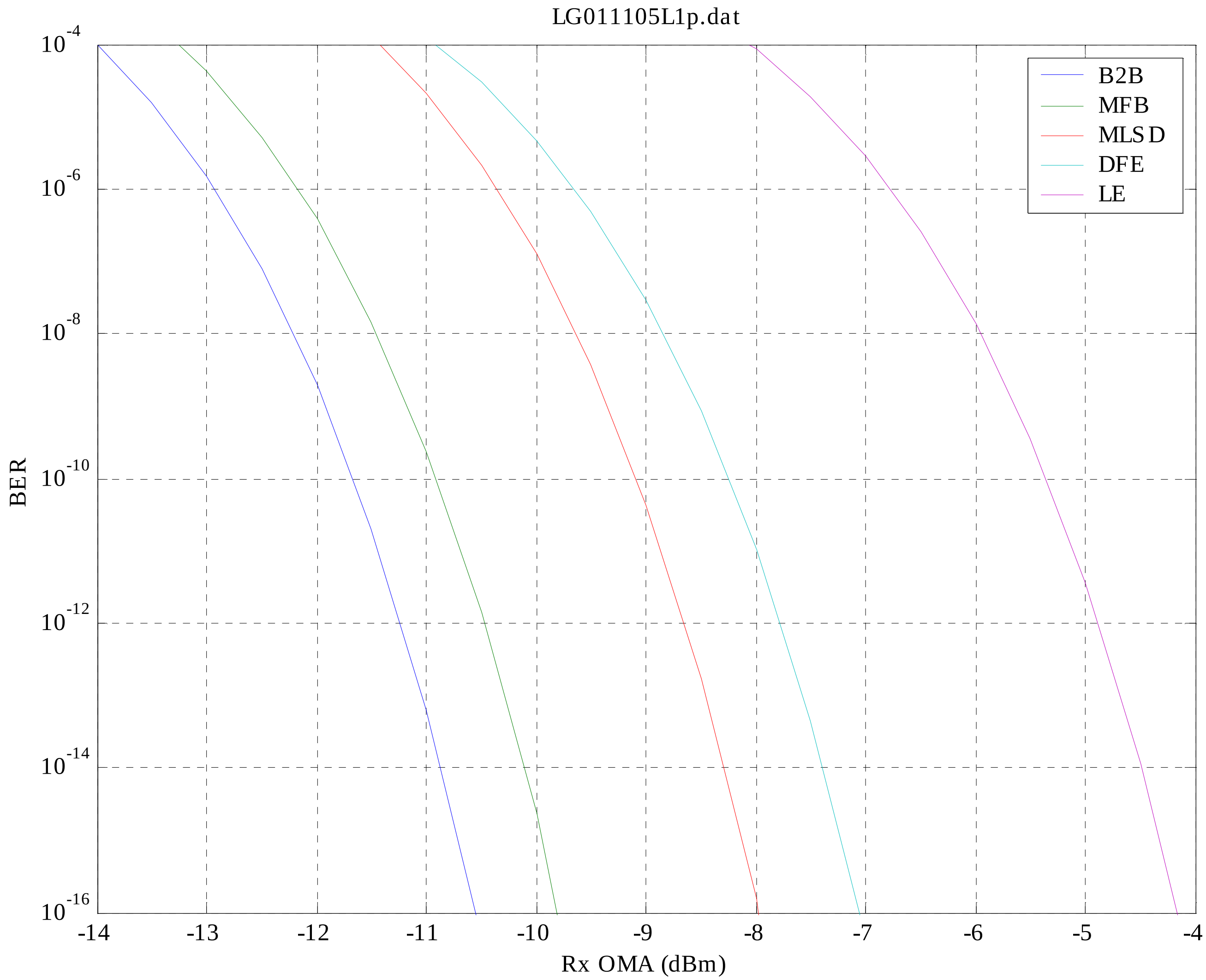
Emulated waveform eye using LPF with 4-tap FIR

Simulations of EDC Performance

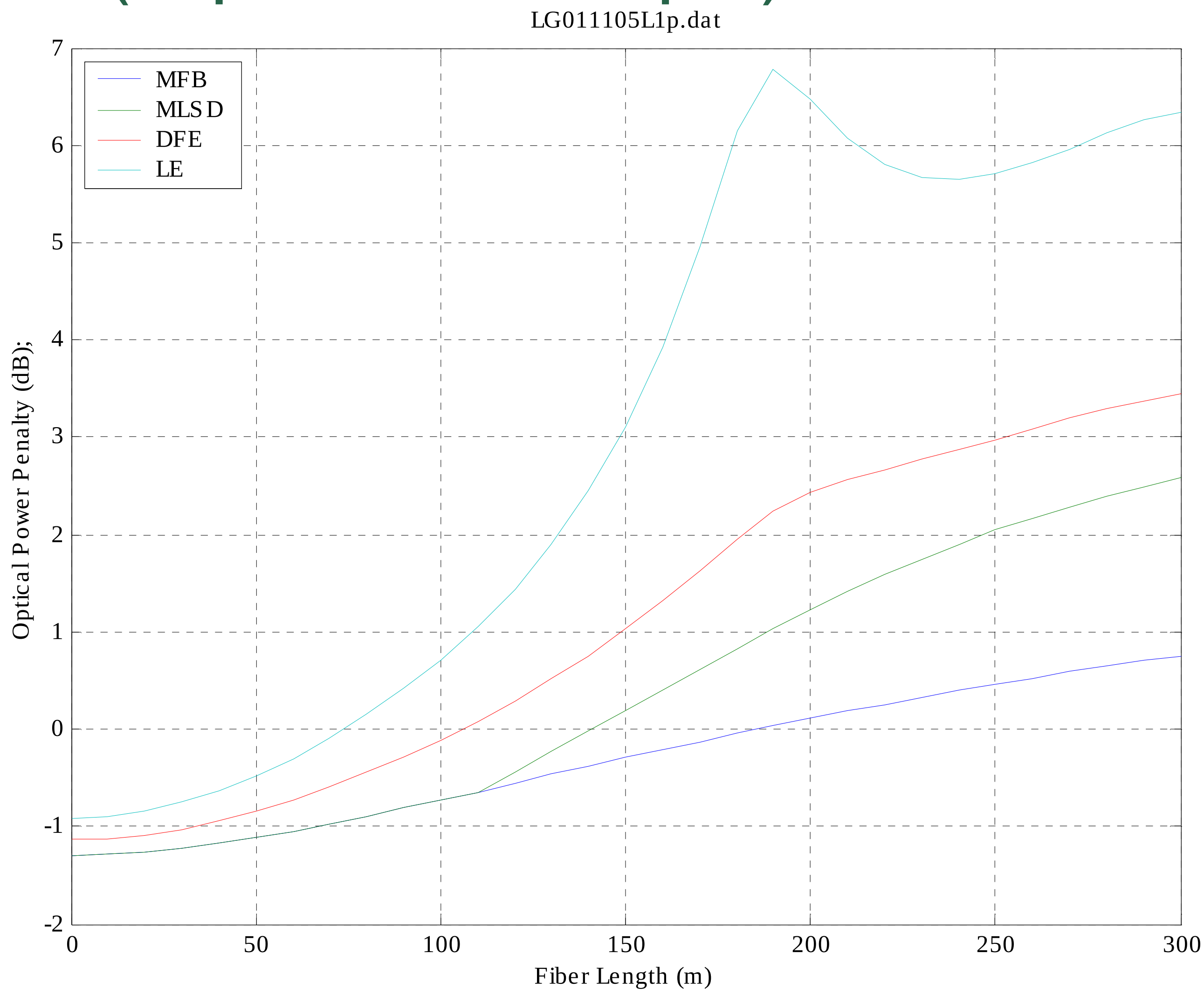
Performance Simulations

- Following plots show waterfall, power penalty curves for 3 selected fibers
- Power penalty curves use unequalized back-to-back case as baseline
  - Power penalty does not include ISI penalty caused by finite bandwidth of laser, photodetector
  - Need to add these ISI penalties for direct comparison to "Pisi" in 802.3ae link budget

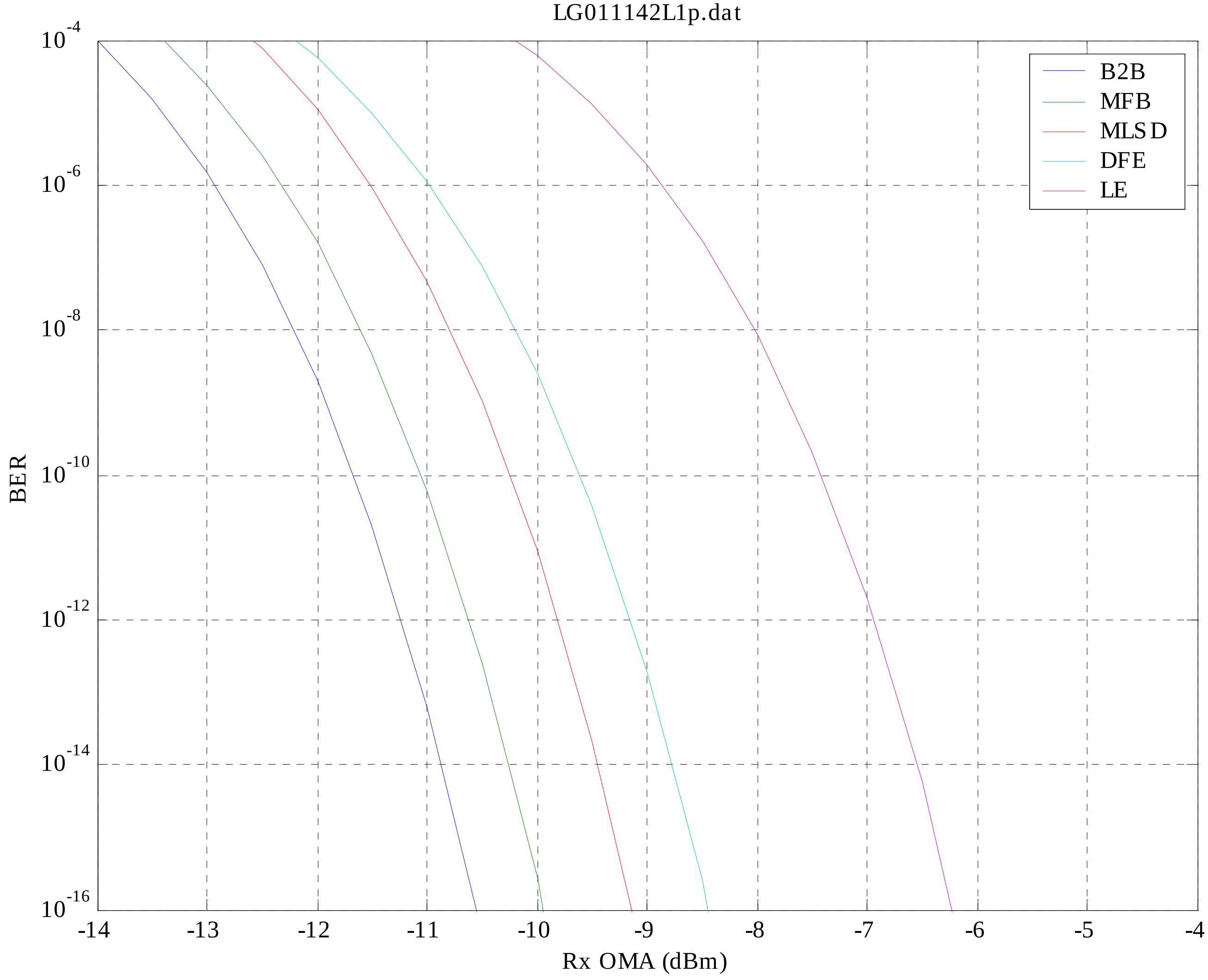
Fiber 1 (Equal Power Split) - Waterfall



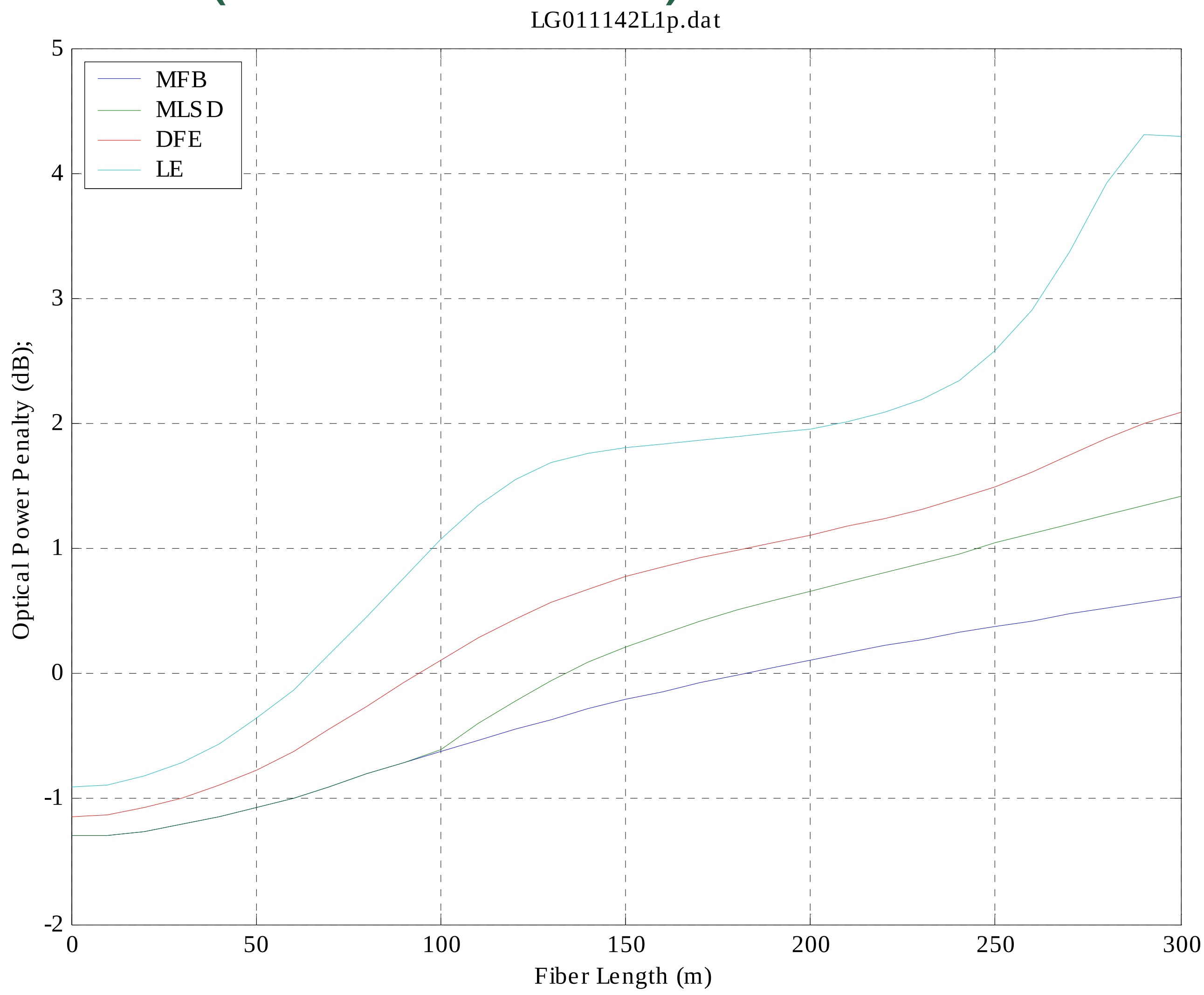
Fiber 1 (Equal Power Split) - Power Penalty



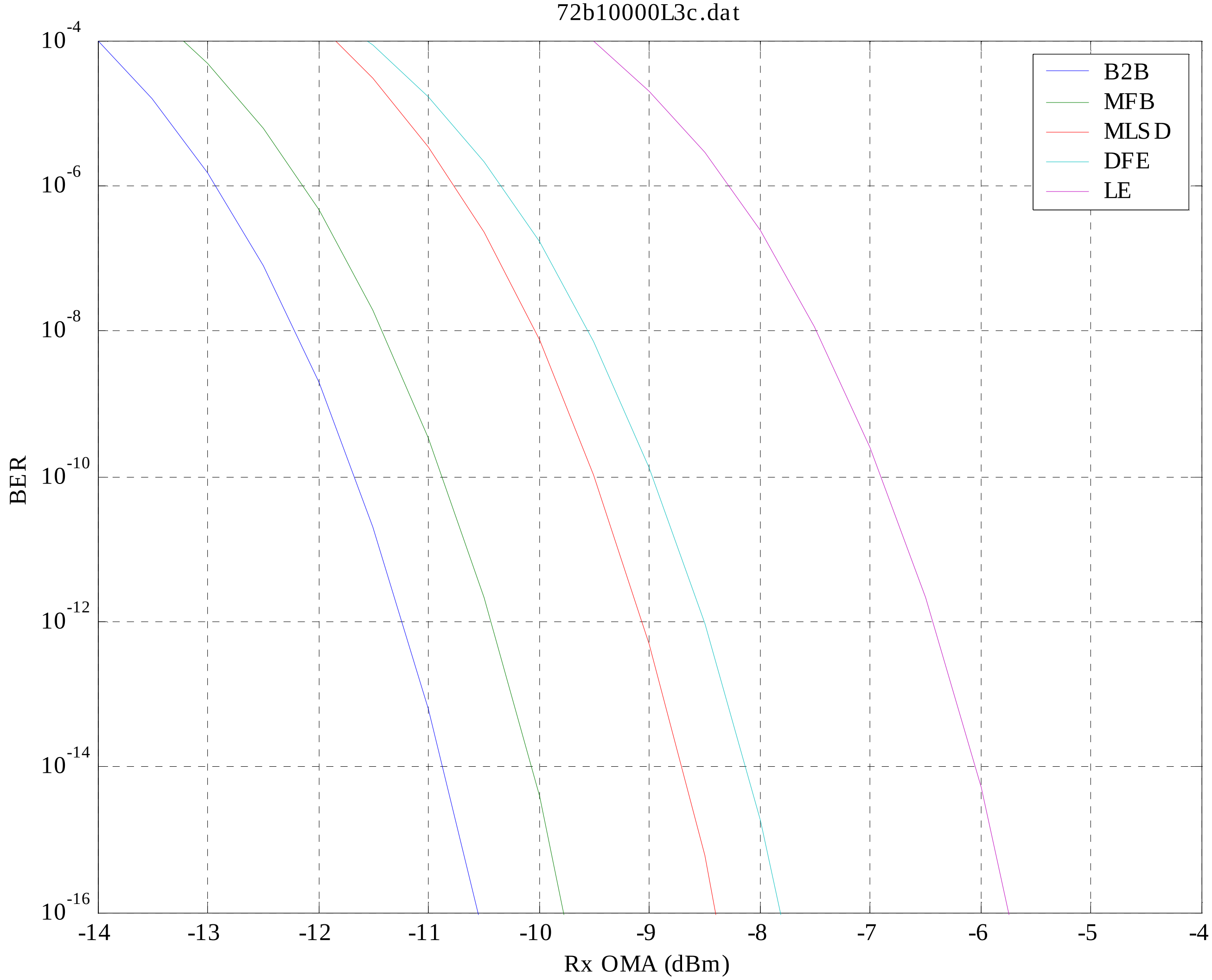
Fiber 2 (Worse DMD) - Waterfall



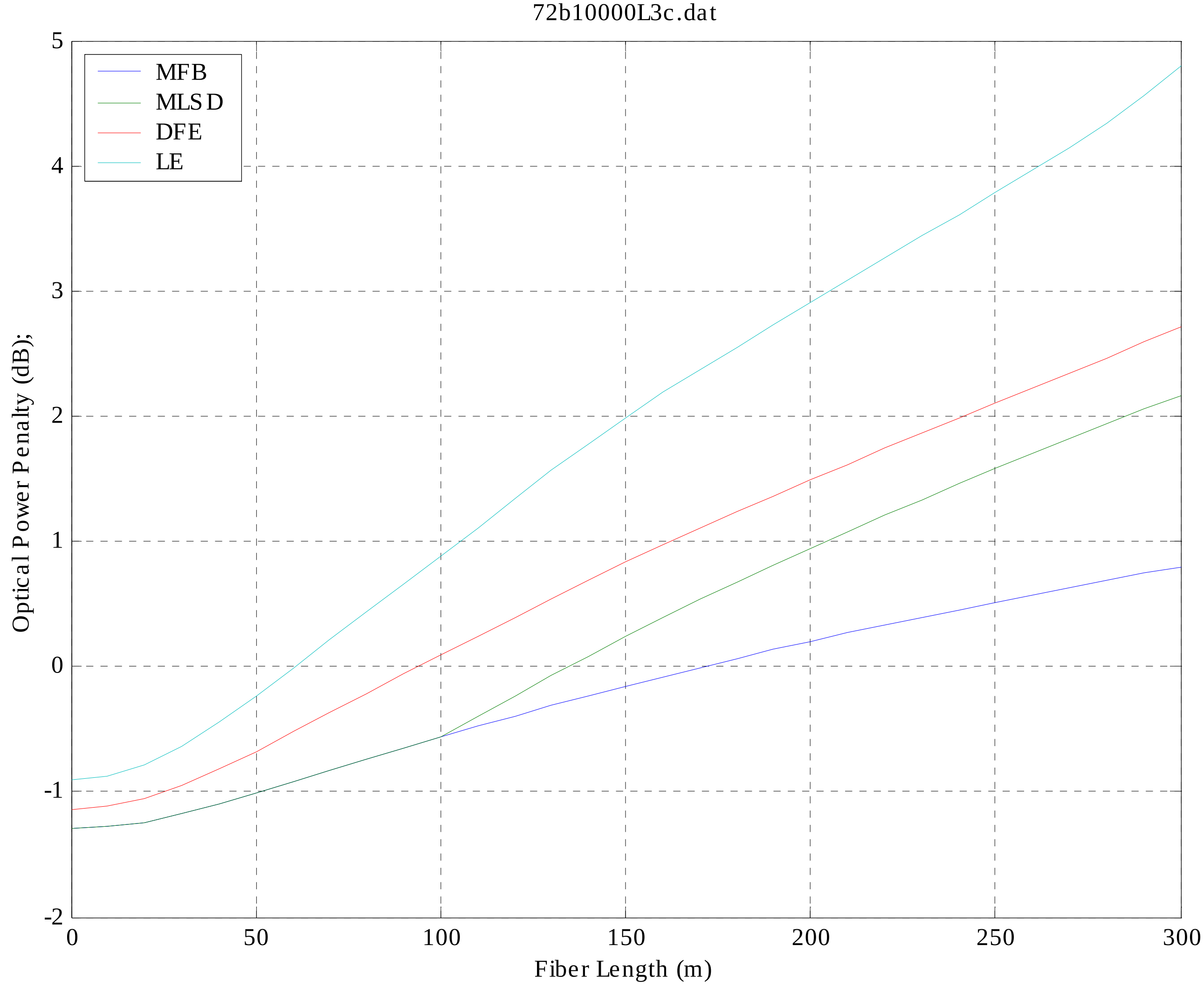
Fiber 2 (Worse DMD) - Power Penalty



Fiber 3 (Single Pulse) - Waterfall



Fiber 3 (Single Pulse) - Power Penalty



Sample Link Budget

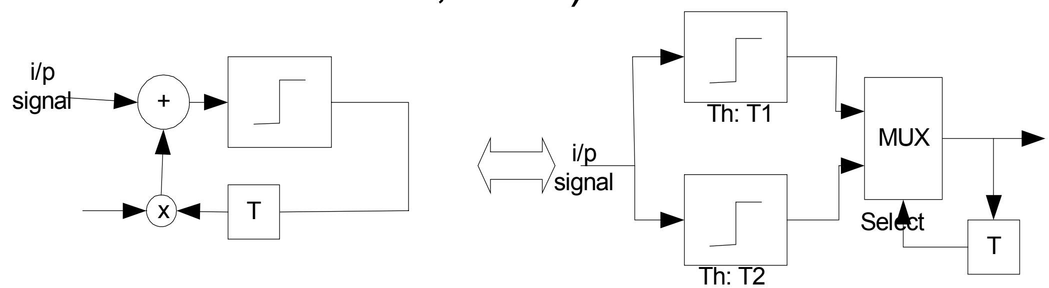
Parameter	10GBASE-L*
Available LR Power Budget	9.4 dB
Channel Insertion Loss	2.3 dB
Allocation for Modal Noise, RIN and other penalties	0.6 dB
Power Budget for Ideal EDC	5.0 dB
EDC Implementation Penalty	1.5 dB
Total budget allocated for EDC	**6.5 dB**

- **DFE and better EDC architectures provide adequate performance for the channels simulated**
- **FFE-based EDC architecture does not close link budget for the channels simulated**

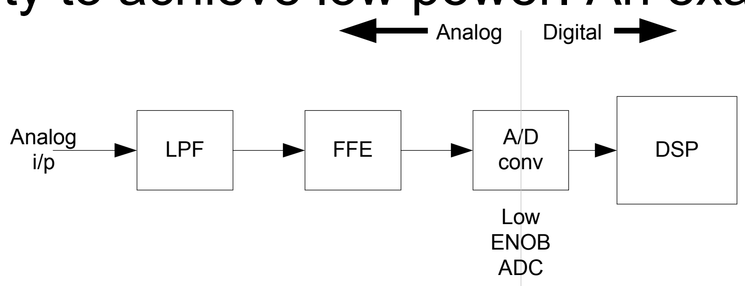
Implementation and Compliance Issues

Implementation Feasibility (1)

- Enhanced filter architectural realizations
  - Exploit parallelizability and pipelineability within signal processing architectures such as FIR filters, feedback loops to meet high-speed requirements.
  - An example – “feedforward” realization of DFE feedback loop (Ref. Kasturia et al: IEEE-JSAC, 1991):



- Optimal partitioning of analog and digital signal processing functionality to achieve low power. An example:



Implementation Feasibility (2)

- Actual equalizer implementations (including reasonable number of taps and finite precision effects) can approach within ~1 dB of the ideal performance shown for these channels.
- Blind (or decision-directed) LMS adaptation can provide sufficient performance; therefore training sequence-assisted adaptation not needed for these channels.
- Speed of adaptation: Experimental observations suggest coherence time of channel is sufficiently high.
  - Fully digital implementations for the adaptation of tap coefficients may be used.
- RX signal power range determined by linearity requirements and by RX sensitivity
  - EDC with sufficient gain can interoperate with commercial TIA’s or ROSA’s
- TX power range
  - Within 10GBASE-LR link budget, so supported by commercial lasers (FP/DFB).
- *Low-power CMOS or SiGe technology is very feasible for EDC*

Compliance Test Set-Up for EDC-Enabled Receivers: Principles

- Easy to use, repeatable, deterministic, provides for reliable operation in installed fiber base.
- Supports scaling for low cost, high volume manufacturing.
- <u>Methodology</u>
  - Specifies relaxed TX eye mask at TP2.
  - Uses a simple parametric channel model that reasonably captures a high fraction of worst-case MMF (such as discussed earlier)
  - Specifies additive white Gaussian noise (corresponding to worst case SNR).

Conclusions

- EDC significantly reduces the ISI penalty caused by fiber dispersion
- EDC reduces the slope of the power penalty vs. fiber length curve, allowing more flexibility in formulating the link budget (i.e. ISI power penalty is “well-behaved”)
- Blind adaptation eliminates need for training sequence. *No protocol change/bit-rate change required*!
- Low power solutions compatible with XFP are feasible with today’s state-of-the-art technology
- EDC relies on proven Signal Processing technology, already in wide commercial use in wireless, 1000Base-T, disk drive read channel, and many other applications.

Thank You!