BACKGROUND OF SONET/SDH LINE JITTER SPECIFICATIONS

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OUTLINE

- Overview of line jitter requirements and specifications
- Definitions
- Jitter transfer
- Jitter tolerance
- Jitter generation
- Network interface jitter (network limit)

OVERVIEW OF LINE JITTER REQUIREMENTS

- Network interface jitter requirement/Network limit
  - limits accumulated jitter at any STM-N/OC-N network interface
- Equipment requirements
  - jitter tolerance (should stress the equipment at least as much as the network limit would)
  - jitter transfer (controls jitter accumulation)
  - jitter generation (controls jitter accumulation)
- Implementation of Consecutive Identical Digit (CID) Immunity Measurement

SONET/SDH LINE JITTER SPECIFICATIONS

Specification	ITU-T Recommendation	ANSI/T1 Specification	Telcordia GR
Network Interface Jitter	G.825	T1.105.03	GR-253/GR-1377
Jitter Tolerance	G.825 (referred to in G.783)	T1.105.03	GR-253/GR-1377
Jitter Transfer	G.783 (formerly in G.958)	T1.105.03	GR-253/GR-1377
Jitter Generation	G.783 (formerly in G.958)	T1.105.03	GR-253/GR-1377
CID Immunity Measurement	G.957 (formerly in G.958)		

INFORMAL DEFINITIONS

- Note: see G.810 and T1.101for formal definitions pertaining to jitter and synchronization
- **Phase** -- the difference between the actual time of a bit and the ideal time of that bit
  - phase is typically expressed in units of unit intervals (UI), degrees, or radians
  - often referred to as *phase-time* when expressed in units of time
  - phase is a random process; can characterize in the frequency domain (via power spectral density or in the time domain using various statistics (e.g., MTIE, TDEV, etc. (see G.810 and T1.101))

INFORMAL DEFINITIONS (Cont.)

- **Jitter** -- the short-term variations of the times of the respective bits from their ideal times
  - here, *short-term* is quantified by defining a measurement filter
  - measurement filter is a bandpass filter; the high-pass and low-pass portions are precisely defined
  - actually define *high-band* and *wide-band* jitter with appropriate measurement filter for each (i.e., each is characterized by its measurement filter)
    - high-band jitter relates to the jitter of the recovered timing signal and the resulting eye-closure; excessive high-band jitter results in mis-decisions of bits (it is of most interest here)
    - wide-band jitter relates to the buffering of data in the regenerator and the possible over/underflow of this buffer (it is of less interest in this presentation)

INTERFACES

- Jitter transfer, tolerance, generation, and network interface jitter are defined with respect to STM-N OC-N optical interfaces
  - there are definitions for STM-N and OC-N electrical interfaces, but these are not relevant for OC-192 and STM-64
- For jitter tolerance, sinusoidal jitter is applied to an STM-N optical signal by sinusoidal modulation
  - this will be described in more detail later

JITTER TRANSFER

- Basic objectives of clock recovery circuit (paraphrased from [1])
- Generate a timing signal that can be used to sample the data
  - track the input data in the presence of jitter (i.e., tolerate the input jitter)
  - stay locked to the data stream during periods of no transitions
- First requirement drives the bandwidth of the clock recovery PLL wider
  - i.e., above the frequency range of the jitter
- Second requirement drives the PLL bandwidth narrower, as recovered clock phase tends to drift during periods of no transitions
- Current CID test sequence in G.957 has 72 consecutive 1s and 72 consecutive 0s
  - driven by expected output of SONET/SDH scrambler

JITTER TRANSFER (Cont.)

- Additional requirement to limit jitter accumulation over reference chain of regenerators
  - this tends to limit the 3 dB bandwidth and gain peaking
  - has been shown (via both simulation and measurement; see, for example, [2] - [4]) that, with gain peaking, can eventually get very rapid jitter accumulation

JITTER TRANSFER (Cont.)

- Above gave rise to jitter transfer requirement
  - concentrate on Type A regenerators here
- (line rate)/(3 dB bandwidth of clock recovery circuit) > 1250
  - for 10 Gbit/s (STM-64), f3dB <= 8 MHz
- Gain peaking <= 0.1 dB
- roll-off = 20 dB/decade
- Above requirement was based on both simulation and measurement
- More recently, may have implementations with initial wide-band PLL (meeting above requirement) to recover clock, followed by narrower band PLL to time output data
  - this implies data is buffered (consistent with processing of regenerator section overhead)
  - reduces jitter accumulation (but this is not an ITU-T, ANSI, or Telcordia GR requirement)

JITTER TOLERANCE

- Input jitter is considered one of possibly many impairments that may impact BER
- Characterize its effect on equipment via a *power penalty*
- Original studies (see, for example, [5] and [6]) looked at particular jitter processes input to equipment, and considered the magnitude of jitter that corresponds to a 1 dB optical power penalty at a specific BER
  - example distributions were Gaussian and truncated Gaussian
  - jitter processes were broadband, with the magnitude characterized by the rms (standard deviation) of the process (area under the PSD)
- Also note that it is *alignment* jitter that gives rise to mis-decisions and bit errors
  - *Alignment jitter* is defined as the difference between the input phase and the output phase; it is in essence the difference between the actual and ideal sampling times of the decision circuit

JITTER TOLERANCE (Cont.)

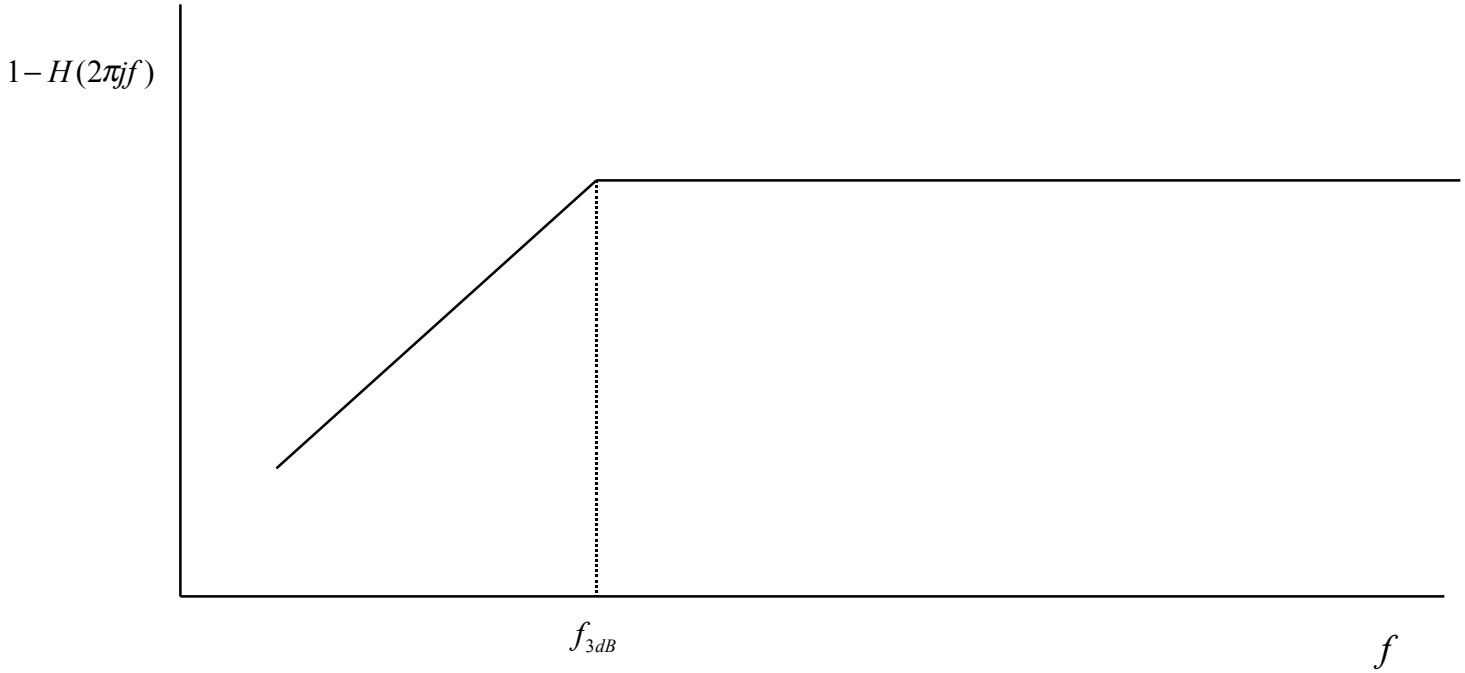
- The alignment jitter process is related to the input jitter by a high-pass transfer function

$$e_a(j\omega) = (1 - H(j\omega))e_{in}(j\omega)$$

where $H(j\omega)$ is the jitter transfer function

- This shows why it is jitter and not phase that gives rise to sampling offset and mis-decisions; low frequency phase variation is tracked by the clock recovery PLL
  - For broadband input phase noise, it is mainly the portion above the PLL cutoff frequency that influences BER and power penalty

JITTER TOLERANCE (Cont.)



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JITTER TOLERANCE (Cont.)

- Now, the power penalties as defined above (or the jitter associated with a specific penalty) are heavily dependent on the distribution and on parameters of the model
- It was found that the use of sinusoidal alignment jitter is conservative
  - sinusoidal alignment jitter of a specific (peak-to-peak) magnitude causes a much larger power penalty than truncated Gaussian alignment jitter of the same peak-to-peak magnitude
- Therefore, a sinusoidal jitter tolerance mask was created for SONET/SDH equipment
  - jitter tolerance is defined relative to the STM-N or OC-N optical interface (as indicated earlier, there are also STM-N and OC-N electrical interfaces, but these are not relevant for the STM-64 and OC-192 rates discussed here)
- Let the input phase variation be sinusoidal, with frequency f_m and peak-to-peak magnitude $2K$

$$e_{in} = K \sin 2\pi f_m t$$

JITTER TOLERANCE (Cont.)

- Then the input phase and alignment jitter are related by

$$e_a(t) = (1 - H(2\pi j f_m)) K \sin 2\pi f_m t$$

- If we wish to tolerate a certain peak-to-peak alignment jitter $e_a^{p\text{-}p}$, then the peak-to-peak input $J_{P\text{-}P}$ jitter that must be tolerated is (all at frequency f_m)

$$J_{P-P} = \frac{e_a^{P-P}}{1 - H(2\pi j f_m)}$$

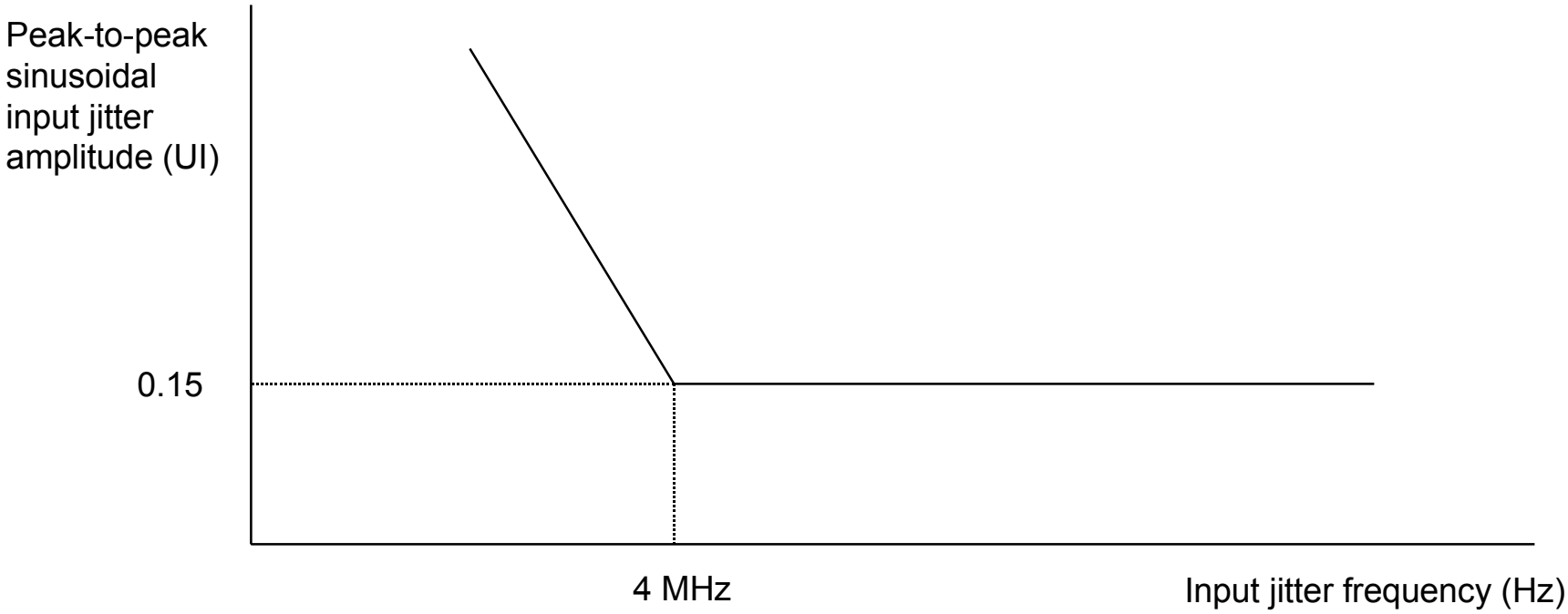
- Since $H(j\omega)$ has a low-pass characteristic, 1 - $H(j\omega)$ has a high-pass pass characteristic
  - then, for fixed $e_a^{P\text{-}P}$, the jitter tolerance mask decreases with a slope of 20 dB/decade until it reaches $e_a^{P\text{-}P}$ at the cutoff frequency of $H(j\omega)$, and is then flat with a value of $e_a^{P\text{-}P}$

JITTER TOLERANCE (Cont.)

- In jitter tolerance mask, neglect the gain peaking
- Also, choose the breakpoint to be one-half the PLL 3 dB bandwidth
  - 4 MHz for STM-64
  - this allows for the fact that the actual clock recovery BW will be somewhat less than the 8 MHz maximum
  - the narrowest allowed BW is one-half the widest allowed BW
- Finally, the sinusoidal alignment jitter that must be tolerated was chosen as 0.15 UIpp
  - for expected pulse shapes (the references used either cosine or raised cosine), this range of sinusoidal alignment jitter corresponds to 1 dB optical power penalty while allowing for some static sampling offset
- Resulting mask is on next slide

JITTER TOLERANCE (Cont.)

Sinusoidal Jitter Tolerance Mask for STM-64 (portion that stresses clock recovery PLL)



Note: there are other breakpoints and corresponding levels at lower frequencies, corresponding to other effects not discussed here

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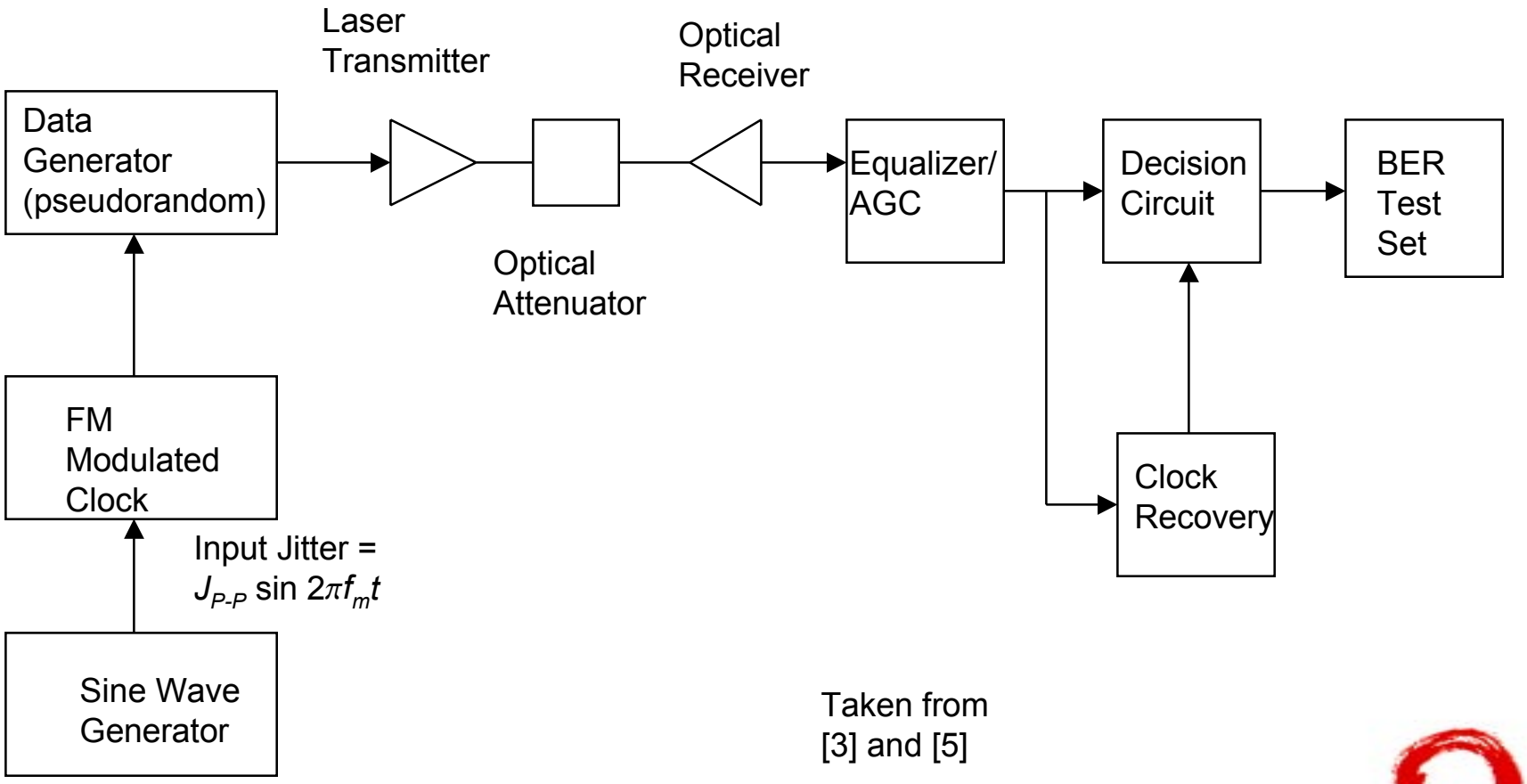
JITTER TOLERANCE TEST METHODOLOGY

- Refer to figure on next VG (taken from [3] and [5]); more details of procedure is outlined in ITU-T Recommendations O.171 and O.172 (Jitter measuring equipment for PDH and SDH, respectively)
  - Pseudorandom data has 2^{23} - 1 word length
- With the setup on the next VG, and with no input jitter, increase the noise or attenuation (or set the power) such that a convenient BER is measured (O.171 suggests 100 errors per second, or 1e-8 for 10 Gbit/s rate)
  - Note that this is a higher BER than the reference BER for defining receiver sensitivity
- Record the SNR
- Increase the Optical power by 1 dB (optical) (the BER will decrease)
- Set the jitter frequency to the desired value (one of the values covered by the mask
- (Continued on VG after next)

JITTER TOLERANCE TEST METHODOLOGY (Cont.)



Taken from
[3] and [5]

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JITTER TOLERANCE TEST METHODOLOGY (Cont.)

- Increase the jitter amplitude until the BER returns to its value before the optical power was increased by 1 dB (1e-8 in the example here)
- Plot this peak-to-peak amplitude versus this frequency; this is one point on the measured jitter tolerance
- Repeat the above for the range of frequencies covered by the mask. The resulting curve should be below the mask for the test to be passed

JITTER GENERATION

- Jitter generation was chosen such that jitter accumulation over a reference chain of regenerators would not exceed 0.15 UIpp
- Verified by simulation studies and measurements
- Measure jitter generation as peak-to-peak output (over a measurement interval) when no input jitter is applied to pseudo-random input data
  - often, 60 s interval is used
  - could also measure rms jitter over the interval, if appropriate

JITTER GENERATION (Cont.)

- At present, there are 2 specs (one for SONET (Option 2 SDH), and one for Option 1 SDH (same as ETSI spec))
  - Option 1
    - high band limit is 0.1 UIpp, measured from 4 MHz to 80 MHz
    - wide-band limit is 0.3 UIpp, measured from 20 kHz to 80 MHz
  - Option 2
    - 0.01 UIrms limit (and also 0.1 UIpp in GR-253)
    - no measurement filter specified in G.783; 12 kHz high-pass in T1.105.03 (and 80 MHz low-pass also in GR-253), but there has been some discussion to align with Option 1 and with the network interface measurement filters in G.825

NETWORK INTERFACE JITTER

- Specify peak-to-peak jitter allowed at a network interface (STM-N or OC-N)
  - measured over a convenient interval
  - both high-band and wide-band limits
- For STM-64
  - limit to 0.15 UIpp when measured from 4 MHz to 80 MHz
  - limit to 1.5 UIpp when measured from 20 kHz to 80 MHz
- As before, high-pass filter is first-order; low pass filter is 3rd order, butterworth
- Note that the high-band limit amplitude and breakpoint are consistent with the jitter tolerance mask

REFERENCES

[1] Tim Armstrong, Richard Kusyk, T1X1.5/97-130, 1997.

[2] E.L. Varma and J. Wu, *Analysis of Jitter Accumulation in a Chain of PLL Timing Recovery Circuits*, Proc. IEEE Globecom, 1982, pp. 653-657.

[3] Patrick R. Trischitta and Eve L. Varma, *Jitter in Digital Transmission Systems*, Artech House, 1989.

[4] Patrick R. Trischitta, Peddapullaiah Sannuti, and Christodoulos, *A Circulating Loop Experimental Technique to Simulate the Jitter Accumulation of a Chain of Fiber-Optic Regenerators,* IEEE Trans. Communications, Vol. 36, No. 2, Feb., 1988.

[5] Patrick R. Trischitta and Peddapullaiah Sannuti, *The Jitter Tolerance of Fiber Optic Regenerators,* IEEE Trans. Communications, Vol. 35, No. 12, Dec., 1987.

[6] K. Schumacher and J.J. O'Reilly, *Distribution Free Bound on the Performance of Optical Communication Systems in the Presence of Jitter,* IEE Proceedings, Vol. 136, Pt. J, No.2, April, 1989.