Cl **45** *SC* **45.2.7.100** *P* **47** *L* **1** # 1
Marris, Arthur Cadence

Comment Type **E** *Comment Status* **A**

Correct editors comment at the top of the page

SuggestedRemedy

remove refernec to 7.83.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.5** *P* **49** *L* **8** # 2
Marris, Arthur Cadence

Comment Type **T** *Comment Status* **R**

Correct PICS by correcting subclause to 45.2.1.6 for *BPE, remove shalls from PMA/PMD management functions and add tables for AN options and AN management functions.

SuggestedRemedy

As above

Response *Response Status* **C**

REJECT.

The reference item was deleted from the document and should have been shown in the compare document with a crossout.

These changes are being done in P802.3an.

Cl **45** *SC* **45.2.1.8** *P* **24** *L* **32** # 3
Marris, Arthur Cadence

Comment Type **T** *Comment Status* **A**

Need to add modifications for the 10G PMD transmit disable register

SuggestedRemedy

modify 802.3an to add the following text:

45.2.1.8 10G PMA/PMD transmit disable register

The transmit disable function for serial PMDs is described in 53.4.7 and 72.6.5. The transmit disable function for 10GBASE-KX4 is described in 71.6.5.

Response *Response Status* **C**

ACCEPT.

add transmit disable register definition as a modification to 802.3aq

Cl **45** *SC* **45.2.1.7.6** *P* **25** *L* **1** # 4
Marris, Arthur Cadence

Comment Type **T** *Comment Status* **A**

Wrong clause number - should be 45.2.1.10

SuggestedRemedy

Correct the clause number for the bit definitions for register 1.11 the extended ability register. They should be 45.2.1.10.6 and 45.2.1.10.7

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
They should be 45.2.1.10.3 and 45.2.1.10.4

Cl **45** *SC* **45.2.1.76.2** *P* **26** *L* **24** # 5
Marris, Arthur Cadence

Comment Type **E** *Comment Status* **A**

Missing word 'to'

SuggestedRemedy

Reword to 'This bit maps to the state variable'

also do this for 45.2.1.77.1, 45.2.1.77.2, 45.2.1.77.3, 45.2.1.77.4

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.78.1** *P* **28** *L* **12** # 6
Marris, Arthur Cadence

Comment Type **E** *Comment Status* **A**

Change 'The update gain defines' to 'The update gain bits define'

SuggestedRemedy

as above

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.78** *P* **28** *L* **27** # 7

Marris, Arthur Cadence

Comment Type **E** *Comment Status* **A**

IN tables 45-56, 45-57, 45-58, 45-59 remove the underlining of bits 1:0, 3:2 5:4 and 15.

SuggestedRemedy

as above

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.1.1.4** *P* *L* # 8

Bradshaw, Peter Intersil Corpn.

Comment Type **ER** *Comment Status* **A**

This refers to the following unsatisfied comment: #21152,

Both the suggested remedy and the response to this comment use the wording "ports types". The correct form is "port types". A search of several sections of the 802.3-2005 confirms that "ports types" does not appear (except as part of "Supports types", but all such possible occurrences are given as "port types", the grammatically correct form. The proposed "Change text to" would introduce the error.

SuggestedRemedy

In the response "ACCEPT IN PRINCIPLE" to comment # 152, under "Change text to", replace "ports types" by "port types".

Response *Response Status* **W**

ACCEPT.

Although the comment database refers to "ports types" when the change was made to the document the correct form "port types" was used. Therefore no further action is required.

Cl **69** *SC* **69B.4** *P* **208** *L* **10** # 9

Powell, Scott Broadcom

Comment Type **TR** *Comment Status* **A**

** Pile onto Ali Ghiasi's unresolved comment number 21127 **

SuggestedRemedy

See comment

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

See response to comment #40.

Cl **72** *SC* **6.10.2.7.1** *P* **112** *L* **6** # 10

Andre, Szczepanek Texas Instruments

Comment Type **E** *Comment Status* **A**

MIN_LIMIT and MAX_LIMIT are not constants. The limits are subject to the restrictions on tap coefficient values stated in 72.7.1.10

SuggestedRemedy

Move MIN_LIMIT and MAX_LIMIT to the variables section.

Change the descriptive text to something on lines of ...

MIN_LIMIT
Integer variable containing the minimum tap coefficient value, subject to the constraints detailed in 72.7.1.10.
MAX_LIMIT
Integer variable containing the maximum tap coefficient value, subject to the constraints detailed in 72.7.1.10.

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **6.10.2.8** *P* **114** *L* **32** # 11

Andre, Szczepanek Texas Instruments

Comment Type **ER** *Comment Status* **A**

COEFF_UPDATE function lacks ""preset"" & ""initialize"" inputs

Currently ...

COEFF_UPDATE(coefficient,inc,dec,gain)
Adds or subtracts the requested gain value to the coefficient value. If inc is TRUE then the function returns (coefficient + gain). If dec is TRUE then the function returns (coefficient û gain).
Otherwise the function returns coefficient.

SuggestedRemedy

Replace with ..

COEFF_UPDATE(coefficient,preset, initialize,inc,dec,gain)
Sets a fixed coefficient value, or Adds or subtracts the requested gain value to the coefficient value.
If initialize is TRUE then the function returns the coefficient vale such that the transmit output meets the conditions defined in 72.6.10.3.2.
If preset is TRUE then the function returns the coefficient value equivalent to no equalization (C(-1) & C(1) coefficients are set to zero, C(0) set to maximum).
If inc is TRUE then the function returns (coefficient + gain).
If dec is TRUE then the function returns (coefficient û gain).
Otherwise the function returns coefficient.

Response *Response Status* **W**

ACCEPT.

Cl **74** *SC* **7.4.4.1** *P* **187** *L* **5** # 12

Andre, Szczepanek Texas Instruments

Comment Type **T** *Comment Status* **A**

The change to the initial PN-2112 state improves the DC balance of the transmitted transcode bit, but does not really scramble it.

A better solution would be to scramble the transcode bit before Parity generation/unscramble before sync re-creation.

A simple way to do this (suggested by Pat Thaler) would be to XOR the transcode bit with one of the associated (scrambled) data bits. This avoids the need to define another scrambler, and is very easy to implement - it requires just one XOR gate.

The adjacent data bit (0) should not be used, I have picked bit 8 in my suggested resolution but I am willing to leave this to the editors discretion.

SuggestedRemedy

I think the change can be accomplished with these two changes

Change section 74.7.4.2 to:

The FEC encoder connects to the PCS Gearbox function using the 16-bit tx_data-group. The FEC encoder takes 32 x 64b/66b blocks from PCS and encodes it into a single FEC block of 2112 bits. The FEC Encoder compresses the two sync bits to one transcode bits as explained in 74.7.3.

The transcode bit is then XOR'ed with data bit 8.

The resulting 32 x 65b = 2080 bits with the frame format as shown in Table 74û2 are fed to the (2112,2080) encoder, which produces 32 parity-check bits. The parity check bits are appended to the end of the FEC frame. The FEC frame is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1. and sent to the PMA interface.

Change section 74.7.4.5 paragraph 2 (page 187 line 34) to:

The FEC decoder recovers and extracts the information bits using the parity-check data. In case of successful decoding the decoder restores the sync bits in each of the 64b/66b blocks sent to the PCS function,

by first XOR'ing the received transcode bit with the associated data bit 8 and then generating the two sync bits.

When the decoder is configured to indicate decoding error, the decoder indicates error to the PCS by means of setting both sync bits in each of the 64B/66B block to the same value (11), thus forcing the PCS sublayer to consider this block as invalid.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In addition to the proposed response, ensure that it is clear which bit is bit 8.

Revert PN-2112 initialization back to the text in draft 2.1. (binary sequence 101010..)

Cl **69B** *SC* **69B.4.1** *P* **209** *L* **5** *#* 13

Moore, Charles Avago Technologies

Comment Type **TR** *Comment Status* **A**

Channel attenuation is too large. For KR port type, signal for worst case channel with worst case attenuation and ripple will not not have enough margin to work in the presence of worst case PSXT.

SuggestedRemedy

reduce channel attenuation by 3dB at 5.15625GHz. Suggested values for b1-b4 will be provided in a separate presentation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt values on P. 8 in goergen_01_0206.pdf, based on EIT results presented to date.

Cl **69B** *SC* **69B.4.5.4** *P* **214** *L* **42** *#* 14

Moore, Charles Avago Technologies

Comment Type **TR** *Comment Status* **A**

Crosstalk levels are too high. They represent an interference tolerance which reasonable receivers will not be able to handle even with reduced channel loss.

SuggestedRemedy

either increase ICR by 12dB or change method of specifying crosstalk. Alternate method will be described in a separate presentation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Either change equation 69B-21 from

ICRfit (f) > = ICRmin (f) =12.5- 20 log(f/5GHz)

to:

ICRfit (f) > = ICRmin (f) =14.8 - 18.7log(f/5GHz)

Cl **72** *SC* **72.7.2.1** *P* **129** *L* **6** *#* 15

Moore, Charles Avago Technologies

Comment Type **TR** *Comment Status* **R**

Worst case combination of effects of crosstalk, self interference, and DCD add up to an equivalent of an EITbaseline of 21mV, 15.

SuggestedRemedy

Change EITbaseline value in specification to 21mV. Justification for this number was sent to the reflector and will be repeated in a separate presentation.

Response *Response Status* **U**

REJECT.

In light of changes to Amax and ICRmin (See Comments #13 and #14), the study of the proper EIT value needs to be revisited.

Cl **72** *SC* **72.7.1** *P* **120** *L* **26** *#* 16

Mellitz, Richard Intel

Comment Type **TR** *Comment Status* **R**

Table 72-9
0.05 UI DCD is too high
Refer to krooswyk_c1_0106.pdf

SuggestedRemedy

Suggest changing DCD to 0.03 UI

Response *Response Status* **U**

REJECT.

The task force can not reach consensus to make the change.

Straw Poll #3
a. Reduce DCD to 0.03UI
b. Keep DCD at 0.05UI

A - 6
B - 9
abstain - 3

Cl **69A** *SC* **69a.2.2** *P* **203** *L* **23** # 17
Mellitz, Richard Intel

Comment Type **TR** *Comment Status* **A**

The test channel need to have a return loss spec so that it is not double counting in EIT voltage.

SuggestedRemedy

The test channel have a return loss greater than 20 dB for a range spanning f1 and f2.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See comment 136.

Cl **71** *SC* **71.7.1** *P* **85** *L* **36** # 18
Dudek, Mike Picolight

Comment Type **TR** *Comment Status* **R**

Sub clause 71.6.6 says that transmit disable shall drive a constant level that does not exceed the maximum differential peak-to-peak output voltage in Table 71-4. The only maximum differential peak-to-peak output voltage in that table is the normal value (not disabled).

SuggestedRemedy

Insert an extra row in table 71.4 with Maximum differential peak-to-peak output voltage when disabled.

Response *Response Status* **W**

REJECT.

Text in 71.6.6 is saying that the differential voltage during disable is constrained by the same specification as the maximum differential peak-to-peak output voltage during normal operation, as defined in Table 71-4.

Motion #3
Technical (>=75%)
Move to accept response.
Move - John D'Ambrosia
Second - Tom Palkert

All
Y- 13
N- 0
A- 2

Motion passes

Cl **71** *SC* **71.10.4.1** *P* **95** *L* **43** # 19
Dudek, Mike Picolight

Comment Type **TR** *Comment Status* **A**

There is technical detail in the PICS that contradicts the main document in FS10, FS11, FS12, and TC5

SuggestedRemedy

Fix it.

Response *Response Status* **W**

ACCEPT.
Make FS10, FS11, FS12, and TC5 consistent with the text.

Cl **72** *SC* **72.6.1** *P* **102** *L* **53** # 20
Dudek, Mike Picolight

Comment Type **E** *Comment Status* **A**

The reference to figure 72-2 doesn't make sense.

SuggestedRemedy

Change Figure 72-2 to Figure 72-1

Response *Response Status* **C**

ACCEPT.

Cl **71** *SC* **71.7.1.9** *P* **90** *L* **19** # 21
Dudek, Mike Picolight

Comment Type **E** *Comment Status* **R**

The references to the figures appear to be wrong. (Fig 71-5 is differential return loss which doesn't make sense.

SuggestedRemedy

Change fig 71-5 to fig 71-6 (or maybe it should be fig 71-1)

Response *Response Status* **C**

REJECT.

Text in Clean version was correct
Fig.ref is to fig71-2 and fig71-5

This is a Frame diferential Issue

Cl **72** *SC* **72.7.1** *P* **120** *L* **16** *#* 22

Dudek, Mike Picolight

Comment Type **TR** *Comment Status* **R**

Subclause 72.6.5 states that the transmit disable shall drive a constant level not to exceed the maximum differential voltage peak-to-peak voltage in Table 72-6. The only value of maximum differential voltage in that table is the normal value which doesn't make sense.

SuggestedRemedy

Add row to Table 72-6 with maximum differential voltage with Tx disable.

Response *Response Status* **W**

REJECT.

Text in 72.6.5 is saying that the differential voltage during disable is constrained by the same specification as the maximum differential peak-to-peak output voltage during normal operation, as defined in Table 72-6.

See also comment #18.

Cl **69** *SC* **B.4** *P* **208** *L* **1** *#* 23

Agarwal, Puneet Broadcom

Comment Type **TR** *Comment Status* **A**

Comment #127 on draft 2.1 (from Ali Ghiasi) was rejected saying that ""no servicable return loss mask had been proposed"", implying that the suggested remedy was not technically complete. I think the draft itself is not technically complete unless it provides specification for the channel. Specifically, the draft needs to at least specify crosstalk, return loss, insertion loss and insertion loss to crosstalk ratio.

SuggestedRemedy

Define channel specifications in the spec as stated above.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

See response to comment #40

Cl **71** *SC* **7.2.1** *P* **91** *L* **32** *#* 24

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A** *e*

I believe that the intent of Note 1 to Table 71-8 should be to define the total RMS jitter, TJ, as a function the sinusoidal jitter, SJ, and the random jitter RJ and not as a function of DJ and RJ.

SuggestedRemedy

Change note 1 to read:

RMS jitter is defined to be:

TJrms = Sqrt[((SJrms)^2)/8 +((RJpp/14.06)^2)]

where SJrms is the sinusoidal jitter referenced to in 69A.2.1 and RJpp is the peak-to-peak random jitter defined in Table 71-4

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The note is intended to define the origin of the rms jitter value in Table 71-8. The quantity SJrms in the note should be renamed RMS jitter to be consistent with the table.

See comment 32, 35.

Cl **72** *SC* **6.10.2.3.3** *P* **109** *L* **7** *#* 25

Spagna, Fulvio INTEL

Comment Type **ER** *Comment Status* **A**

Make the Initialize update protocol consistent with the Coefficient update protocol.

SuggestedRemedy

Insert following sentence at then of line 7 :

""At that point the outgoing request shall be set to zero""

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Insert the following sentence at then of line 7:

At that poin the outgoing initialize field shall be set to zero.

Cl **45** *SC* **2.1.78.2** *P* **28** *L* **25** # 26

Spagna, Fulvio INTEL

Comment Type **ER** *Comment Status* **A**

In Table 45-57, bits 12 and 13 are not correctly defined.

SuggestedRemedy

Update table to match bits definition in Table 72-7 on page 108

Response *Response Status* **W**

ACCEPT.

Cl **45** *SC* **2.1.80.2** *P* **30** *L* **6** # 27

Spagna, Fulvio INTEL

Comment Type **ER** *Comment Status* **A**

In Table 45-59, bits 12 and 13 are not correctly defined.

SuggestedRemedy

Update table to match bits definition in Table 72-7 on page 108

Response *Response Status* **W**

ACCEPT.

Cl **70** *SC* **7.1** *P* **68** *L* **45** # 28

Spagna, Fulvio INTEL

Comment Type **ER** *Comment Status* **A** *e*

For notational consistency with clause 71 and 72 change the jitter units from UIpp to UI. The parameter listed in the table is already defined as peak-to-peak.

SuggestedRemedy

Change units from UIpp to UI.

Response *Response Status* **W**

ACCEPT.

Cl **73** *SC* **5.3** *P* **141** *L* **13** # 29

Spagna, Fulvio INTEL

Comment Type **ER** *Comment Status* **A**

DME page timing summary Table number is duplicated.

SuggestedRemedy

Change table heading to Table 73-2.

On line 13, page 141 change reference to Table 73-1 inot Table 73-2

Response *Response Status* **W**

ACCEPT.

Cl **45** *SC* **2.1.80.2** *P* **30** *L* **6** # 30

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

The bits in this register are defined as R/W. I interpret this to mean that the register's content can be written by the device, to report the value of the vairables associated to these bits, and by the user through MDIO management. This being the case, there is nothing that prevents a conflict from happening, that is an instance in which both the device and the user try to access the register.

More in general, if the intent is to provide management a way to override the LD coefficient update, there does not seem a mechanism to insure that a value written to the register by management can be acted upon before being overwritten by the device.

SuggestedRemedy

Make the register read only (RO).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make the LD status report register read only.

Cl **45** *SC* **2.1.80.2** *P* *L* *#* 31

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

The bits in this register are defined as R/W. I interpret this to mean that the register's content can be written by the device, to report the value of the vairables associated to these bits, and by the user through MDIO management. This being the case, there is nothing that prevents a conflict from happening, that is an instance in which both the device and the user try to access the register.

More in general, if the intent is to provide management a way to override the LD coefficient update, there does not seem a mechanism to insure that a value written to the register by management can be acted upon before being overwritten by the device.

SuggestedRemedy

Make the register read only (RO).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The register will be made read only (RO).

As a corollary to this discussion, register 152 will be made RW with the write function accessible only when training_enable is deasserted.

Cl **70** *SC* **7.2.1** *P* **73** *L* **32** *#* 32

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A** *e*

I believe that the intent of Note 1 to Table 70-8 should be to define the total RMS jitter, TJ, as a function the sinusoidal jitter, SJ, and the random jitter RJ and not as a function of DJ and RJ.

SuggestedRemedy

Change note 1 to read:

RMS jitter is defined to be:

TJrms = Sqrt[((SJrms)^2)/8 +((RJpp/14.06)^2)]

where SJrms is the sinusoidal jitter referenced to in 69A.2.1 and RJpp is the peak-to-peak random jitter defined in Table 70-4

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The note is intended to define the origin of the rms jitter value in Table 70-8. The quantity SJrms in the note should be renamed RMS jitter to be consistent with the table.

Editorial - correct spelling of "jitter" in test pattern row.

See comment #35, 24.

Cl **72** *SC* **6.10.2.3.2** *P* **108** *L* **46** *#* 33

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

Make the Preset update protocol consistent with the Coefficient update protocol.

SuggestedRemedy

Insert following sentence in line 46 :

""At that point the outgoing request shall be set to zero""

prior to

""Maximum status ... ""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Insert the following sentence at then of line 7:

At that point the outgoing initialize field shall be set to zero.

Cl **72** *SC* **7.1** *P* **120** *L* **3** # 34

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

Add definition for Duty Cycle Distortion

SuggestedRemedy

Replace line 31 with the following text:

""The Duty Cycle Distortion is defined as the ratio of the difference in the mean pulse width of a æ1Æ pulse compared to the mean pulse width of a æ0Æ pulse
(as measured in a clock-like repeating 0,1,0,1,à bit sequence) and the nominal pulse width. Duty Cycle Distortion is considered part of the deterministic jitter distribution.""

Response *Response Status* **C**

ACCEPT.

""The Duty Cycle Distortion is defined as the unsigned ratio of the difference in the mean pulse width of a "1" pulse compared to the mean pulse width of a "0" pulse (as measured at the AC coupled "0" crossing in a clock-like repeating 0,1,0,1 bit sequence) and the nominal pulse width. Duty Cycle Distortion is considered part of the deterministic jitter distribution.""

See comment #44

Motion#4
Moiton to reconsider.

Moved by Fulvio Spagna
Second - Howard Baumer

Passed without objection

Reconsidered resolution -
""The peak-to-peak duty cycle distortion (DCD) is the unsigned ratio of the difference in the mean pulse width of a "1" pulse compared to the mean pulse width of a "0" pulse (as measured at the AC coupled "0" crossing in a clock-like repeating 0,1,0,1 bit sequence) and the nominal pulse width. DCD is considered part of the deterministic jitter distribution.""

Cl **72** *SC* **7.2.1** *P* **128** *L* **14** # 35

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

I believe that the intent of Note 1 to Table 72-14 should be to define the total RMS jitter, TJ, as a function the sinusoidal jitter, SJ, and the random jitter RJ and not as a function of DJ and RJ.

SuggestedRemedy

Change note 1 to read:

RMS jitter is defined to be:

TJrms = Sqrt[((SJrms)^2)/8 +((RJpp/14.06)^2)]

where SJrms is the sinusoidal jitter referenced to in 69A.2.1 and RJpp is the peak-to-peak random jitter defined in Table 72.9

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The note is intended to define the origin of the rms jitter value in Table 72-14. The quantity SJrms in the note should be renamed RMS jitter to be consistent with the table.

See comment 24, 32.

Cl **69B** *SC* **4.3** *P* **210** *L* **13** # 36

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

Equations 69B-7 and 69B-8 are missing. Also, the ""clean"" version of D2p2, which shows the two equations, but references A(f) instead of Amax(f)

SuggestedRemedy

Equations 69B-7 and 69B-8 in D2p2 should reference Amax(f) and not A(f)

Response *Response Status* **C**

ACCEPT.

Cl **69B** *SC* **69B.4** *P* **208** *L* **17** # 37

Telang, Vivek Broadcom

Comment Type **TR** *Comment Status* **A**

This is a pile-on to Ali Ghiasi's UNSATISFIED comment #21127
For interoperability to be guaranteed, the standard should have a normative specification for the channel return loss.

SuggestedRemedy

See equation in Howard Baumer's comment

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

See response to comment #40

Cl **72** *SC* **72.7.1** *P* **120** *L* **22** # 38

Baumer, Howard Broadcom

Comment Type **T** *Comment Status* **A**

Transition times in Table 72-9 do not match the text in 72.7.1.7. Table has 24-40ps and text has 24-47ps.

SuggestedRemedy

Pick one range and make text and table match.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Fix table 72.6 to indicate max transition time of 47ps

Cl **72** *SC* **72.7.2.1** *P* **129** *L* **5** # 39

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **R**

Pile onto commet #56 D2.1
With backplane systems having upwards of 100+ links a target BER specified to 1e-15 should at least be specified along with the standard 802.3 BER of 1e-12. There sould at least be a set of ""shalls"" that go with a BER of 1e-15 even if it makes the inclusion of FEC mandatory.

SuggestedRemedy

Add a new table entry of: BERe with FEC on, 1e-15
or add a second set of test with BER at 1e-15

Response *Response Status* **U**

REJECT.
The following response was accepted by the Task Force without objection.

Comment #57 from D2.1 was a pile-on to #613 from D2.0. A pile-on to a pile-on is not considered a valid new comment. Recirculation requirements have been met.

The response to comment #57 is repeated below.

The Task Force objective is to support a BER of 1E-12 or better, and therefore the performance targets are within the objectives.

However, the Task Force recognizes that some systems may require backplane links that perform better than the stated 1E-12 target. It is suggested that the Forward Error Correction sublayer defined in Clause 74 be utilized to supply this additional performance. It has been shown in:

http://ieee802.org/3/ap/public/nov05/ganga_02_1105.pdf
http://ieee802.org/3/ap/public/nov05/valliappan_01_1105.pdf

that links exhibiting 1E-9 peformance improve to better than 1E-12. Therefore, links operating at 1E-12 can be expected to improve to 1E-15 or better via use of the Clause 74 FEC.

With regards to testability, the interference tolerance test procedure verifies receiver performance, without FEC, to a BER target of 1E-12 or better. Mathematic techniques may then be applied to derive the receiver performance with the benefit of FEC.

Cl **69B** *SC* **69B.4** *P* **242** *L* **20** # 40

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **A**

This is a pile on to D2.1 comment #21127

There are three impairmets to the system:
1) loss in the channel
2) reflections in the channel
3) noise injected into the channel from external sources

All three of these impairments need to be completely specified as conditions of the test. The loss of the ""test channel"" (condition #1) is only partially specified, the slope of the loss is specified (mTC) whereas the D.C. component is not (bTC). The return loss of the ""test channel"" and of the test signal is not specified at all resulting in partially specifying the test condtions for the reflections in the channel (the receiver's return loss is specified as it is what is under test).

Without the complete specification for #1 & #2, the signal going into the receiver under test will be unknown therefore invalidating any test results. Even using the EIT test to emulate the affects of return loss (self interference) is invalidated for without knowing what the true signal into the reciever under test is you cannot know what level of EIT is appropriate. It cannot be assumed that all test setups will be built with the best possible conditions (i.e. no return loss).

SuggestedRemedy

Specify that the return loss of the channel must be
Return Loss >= -13 + 9.65*log10(f/350MHz) for 500MHz <= f <= 3GHz
Return Loss > -4 for 3GHz < f <= 8GHz

Note: return loss is specified as negative dB here and the limits are such that the compiance (test) channel should have a return loss that is at these levels or worse. The reason for making the test channel worse is that these are compliance conditions on the receiver and therefore the receiver under test needs to be able to tollerate these conditions or worse.

Note #2: The test compliance channel can be built by creating a very clean PCB with a passive circuit network that creates the appropriate insertion loss and return loss.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Howard has indicated that this is really 2 comments, requesting a interconnect return loss limit to go into annex 69B and an identical spec but with the opposite sign for the interference tolerance test channel return loss in annex 69A.

A different EIT Channel Return Loss model was adopted (see comment #136) for the following reasons :

1.Circuits for producing a return loss worse than some line over a broad range of frequencies without greatly distorting the transfer characteristics have not been shown.
2.Having return loss above -10 to -4dB but not otherwise specified will result in very unrepeatable test results.

Recommend change 69B

Add sub clause 69B4.5 and change number of existing 69B4.5 to 69B4.5 etc.

69B4.5 Return loss

The recommended return loss of the interconnect, measured at either end, be such that:

Return Loss >= 13 - 9.65*log10(f/350MHz) for 500MHz <= f <= 3GHz
Return Loss > 4 for 3GHz < f <= 8GHz

Cl **73A** *SC* **73A.2** *P* **187** *L* **36** *#* 41

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **A**

Subclause, page and line number are for file p802.3ap-D2.2.pdf
Message code #5 is improperly encoded. The whole point of the extended next pages was to have to exchange less next pages. The current encoding of MP5 requires 1 message next page and 4 unformatted next pages, however, if it took full advantage of the exteded next pages it would only need 1 message next page and 1 unformatted next page.

SuggestedRemedy

Change the entire 73A.2 to read:

The OUI Tagged Message shall consist of a single message code of 0000 0000 0101 followed by one user code defined as follows. The unformatted code field of Message Next Page 5 shall contain the most significant 11 bits of the OUI (bits 23:13) with the most significant OUI bit in bit 26 (bit U11) of the unformatted code field, the next 11 most significant bits of the OUI (bits 12:2) in bits 42:32 (bit U26 to U16) of the unformatted code field and the remaing unformatted code field bits, bits 31:27 (bits U15 to U10) and bits 47:43 (bits U31 to U27) as a user-defied user code value that is specific to the OUI transmitted. The unformatted next page user code field shall contain the remaining least significant 2 bits of the OUI (bits 1:0) with OUI bit 1 in bit 1 (bit U1) with the remaining bits 10:2, 47:16 (bits U10 to U2, U47 to U16) as a user-defined user code value that is specific to the OUI transmitted.

For example, assume that a manufacturer's IEEE-assigned OUI value is AC-DE-48 and the manufacturer-selected user-defined user code associated with the OUI is 3-CE-1F-CA-35-D9-B2. The message code values generated from these two numbers is encoded into the message next page and unformatted next page codes, as specified in Figure 73Aû7. For clarity, the position of the global broadcast g is illustrated.

Change Figure 73A-7 to match above paragraph.

Response *Response Status* **C**

ACCEPT. Match to the way the extended next pages are used to send these messages in 28C.

Editor"s note: in adding this edit, I found that the figure showing the bit placement didn't match the text. That also applies to the source text in Clause 28C. Since the figure is newer than the text (it was added in Rev AM ballot), the Clause 73 figure has been modified to match the text.

Cl **73A** *SC* **73A.3** *P* **187** *L* **51** *#* 42

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **A**

Subclause, page and line number are for file p802.3ap-D2.2.pdf
Message code #6 is improperly encoded. The whole point of the extended next pages was to have to exchange less next pages. The current encoding of MP6 requires 1 message next page and 4 unformatted next pages, however, if it took full advantage of the exteded next pages it would only need 1 message next page and 1 unformatted next page.

SuggestedRemedy

The PHY ID tag code message shall consist of a single message code of 0000 0000 0110 followed by one user codes defined as follows. The unformatted code field of Message Next Page 6 shall contain the most significant 11 bits of the PHY ID (2.15:5) with the most significant PHY ID bit in bit 26 (bit U11) of the unformatted code field, the next 11 most significant bits of the PHY ID (bits 2.4:0 to 3.15:10) in bits 42:32 (bit U26 to U16) of the unformatted code field and the remaing unformatted code field bits, bits 31:27 (bits U15 to U10) and bits 47:43 (bits U31 to U27) as a user-defied user code value that is specific to the PHY ID transmitted. The unformatted next page user code field shall contain the remaining least significant 10 bits of the PHY ID (bits 3.9:0) in bits 9:0 (bit U9 to U10) with the remaining bits 10, 47:16 (bits U10, U47 to U16) as a user-defined user code value that is specific to the OUI transmitted.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. Match to the way the extended next pages are used to send these messages in 28C.

Cl **72** *SC* **72.7.1.10** *P* **125** *L* **5** *#* 43

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **R**

There is nothing constraiing the negative edge of the transmitter output waveform.

SuggestedRemedy

Add text that constrains the nengative edge the same way the positive edge is constrained.

Response *Response Status* **U**

REJECT.

See comment #45.

Cl **72** *SC* **72.7.1** *P* **102** *L* **47** *#* 44

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **A**

Duty Cycle Distortion is not defined

SuggestedRemedy

Define Duty Cycle Distortion

Response *Response Status* **C**

ACCEPT.

See comment #34

Cl **72** *SC* **72.7.1.10** *P* **106** *L* **49** *#* 45

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **R**

Transmitter output waveform is not constrained tightly enough allowing many different output waveform shapes. See attched example, Vout_KR.pdf, showing two different transmitter output waveforms that would result in different pre-equalization. This creates an unknown for the receiver design.

SuggestedRemedy

Although I do not have a more precise transmitter output waveform constraints the task force needs to more precisely specify the transmitter.

Response *Response Status* **U**

REJECT.

Reference baumer_01_0206.

Suggested remedy is incomplete and presented material does not have consensus. Comments on this issue in D2.3 recirculation will not be ruled out of scope.

Motion #8
Technical (>=75%)
Move to accept response.
Move John D'Ambrosia
Second Schelto van Doorn

Motion passes by acclamation.

Cl **99** *SC* **99** *P* **1** *L* **1** *#* 46

Healey, Adam Agere Systems

Comment Type **ER** *Comment Status* **A** *e*

Draft cover page should contain a description of the status of this document as it relates to the standards process as well as an expiration date. In addition, the header of each page should note the publication date of the draft.

SuggestedRemedy

Update cover page and document template accordingly.

Response *Response Status* **W**

ACCEPT.

Cl **72** *SC* **Table 72-9** *P* **120** *L* **22** *#* 47

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

Table is not consistent with referenced text (72.7.1.7).

SuggestedRemedy

Change transition time range to 24 - 47 ps

Response *Response Status* **C**

ACCEPT.

See 38

Cl **72** *SC* **72.7.1.7** *P* **124** *L* **41** *#* 48

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The draft now contains a precise description of ""no equalization,"" and it should be utilized.

SuggestedRemedy

Add statement to the effect that: ""Transmitter equalization may be disabled via the preset control defined in 72.6.10.2.3.2.""

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.7.1.9** *P* **125** *L* **3** # 49

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The draft now contains a precise description of ""equalization off,"" and it should be utilized.

SuggestedRemedy

Add statement to the effect that: ""Transmitter equalization may be disabled via the preset control defined in 72.6.10.2.3.2.""

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **Table 72-11** *P* **126** *L* **40** # 50

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The draft now contains a precise description of ""equalization off,"" and it should be utilized.

SuggestedRemedy

To simply the table, change references from ""equalization off"" to ""disabled"". Add a footnote to Table 72-11 stating that: ""A coefficient may be disabled by first asserting the preset control defined in 72.6.10.2.3.2, and then manipulating the other coefficients as required by the test.""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Use proposed text and update the cross reference to point to Register 152 in clause 45.

Cl **72** *SC* **72.7.1.10** *P* **127** *L* **6** # 51

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The conditions cited in c) are only valid when the transition times are in the lower end of the permitted range. At the higher end of the range, this formula will tend to underestimate the peak voltage. It is more precise to verify the peak voltage using a 101010... pattern.

SuggestedRemedy

Define a second test pattern (101010...) to be used for peak output voltage measurement. Note that when equalization is off, it is possible that the steady-state voltage measured per 72.7.1.11 will exceed the peak voltage of this new test pattern. Therefore, the requirement must be re-phrased such that thelarger of the two values, Vpk and Vss, must be less than the 600 mV limit.

Appropriate text will be supplied to editor on request.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Delete Bullet C in 72.7.1.10

Add to 72.7.1.4 the requirement that for a 1010 pattern, the peak to peak differential output voltage shall be less than 1200mV, regardless of equalization setting.

Cl **74** *SC* **74.7.4.5** *P* **187** *L* **38** # 52

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The text states that, when the decoder is set to indicate at decoding error, the sync header for the block is set to 11. It is not clear whether this is intended to every block in the FEC frame, or a specific block within the frame. If it is intended to be every block in the frame, this would translate to 32 consecutive sync header errors, which would force the clause 49 lock state machine out of block lock. Is this what was intended?

SuggestedRemedy

Clarify whether all of the blocks in the FEC frame are populated with the invalid sync header, or specifically which blocks is to be corrupted.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Provide which blocks are to be corrupted with Sending '11' . Need to mark "11" in atleast one in every 8th block to guarantee a minimum size Ethernet frame is dropped. This is below the threshold that cause the state machine to go out of sync. Mark the 1st, 9th, 17th, 25th, 32nd, 66 bit block of the decoded FEC blocks.

Cl **45** *SC* **45.2.1.78** *P* **28** *L* **5** *#* 53

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

Preset and Initialize controls added in Clause 72 need to be reflected in the Clause 45 registers.

SuggestedRemedy

Add Preset and Initialize controls and cross-reference to clause 72 (see also 45.2.1.80).

Response *Response Status* **C**

ACCEPT.

Cl **70** *SC* **70.6.4** *P* **67** *L* **30** *#* 54

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A** *e*

The text really doesn't reflect the optional nature of the signal detect function.

SuggestedRemedy

Replace text of 70.6.4 with: ""PMD signal detect is optional for 1000BASE-KX and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.""

Response *Response Status* **C**

ACCEPT.

Cl **71** *SC* **71.6.4** *P* **83** *L* **44** *#* 55

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A** *e*

The text really doesn't reflect the optional nature of the signal detect function. It could also be re-organized to add clarity.

SuggestedRemedy

Replace the text of 71.6.4 with: ""Globabl PMD signal detect is optional for 10GBASE-KX4 and its definition is beyond the scope of this specification. When Global PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

When the MDIO is implemented, each PMD_signal_detect_n value, where n represents the lane number in the range 0:3, shall report the value of signal_detect for the corresponding lane when signal detect is implemented, or OK otherwise.""

Response *Response Status* **C**

ACCEPT.

Cl **70** *SC* **70.7.1.2** *P* **69** *L* **51** *#* 56

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A** *e*

The text in this subclause was based on similar text in Clause 54, which has been clarified via Maintenance Request 1151. This is useful clarification that should be included in P802.3ap.

SuggestedRemedy

Change:
""The nominal differential impedance of the transmit test fixture depicted in...""

to:

""The differential load impedance applied to the transmitter output by the test fixture depicted in ...""

Response *Response Status* **C**

ACCEPT.

Cl **71** *SC* **71.7.1.2** *P* **86** *L* **51** *#* 57

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A** *e*

The text in this subclause was based on similar text in Clause 54, which has been clarified via Maintenance Request 1151. This is useful clarification that should be included in P802.3ap.

SuggestedRemedy

Change:
""The nominal differential impedance of the transmit test fixture depicted in...""

to:

""The differential load impedance applied to the transmitter output by the test fixture depicted in ...""

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.7.1.2** *P* **121** *L* **30** # 58

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The text in this subclause was based on similar text in Clause 54, which has been clarified via Maintenance Request 1151. This is useful clarification that should be included in P802.3ap.

SuggestedRemedy

Change:
""The nominal differential impedance of the transmit test fixture depicted in...""

to:

""The differential load impedance applied to the transmitter output by the test fixture depicted in ...""

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.7.1.4** *P* **121** *L* **49** # 59

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **R**

Insertion loss to crosstalk ratio limits assume that the transmitter and aggressors are of the same PHY type, have similar output amplitude, and similar equalization settings.

However, if it this is not the case, hypothetical scenarios exist where the transmitter is configured for a low peak output voltage and high transmit equalizer gain (Vpk = 400 mV, Vss = 40 mV) while the aggressors have high output voltage and low equalization gain (Vpk = Vss = 600 mV).

This creates an unfavorable signal-to-noise ratio.

SuggestedRemedy

If it cannot be assumed that the transmitter and aggressors are identical, there are multiple approaches to mitigating this issue.

1. Since the peak output amplitude is programmable, increase the minimum output amplitude requirement to accomodate longer channels and higher noise (lower values can be configured for lower loss/noise channels)
2. Limit the maximum output voltage to only be available for transmitter configurations with a certain level of equalization gain
3. Or, some combination thereof.

A supporting presentation will be supplied with additional detail.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **72** *SC* **72.6.10.2.7.2** *P* **114** *L* **6** # 60

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

Changebar version,
update_status variable refers to the Coefficient Status field ""as defined in Table 72-7"", but this table is Table 72-8 Status report field.

non-changebar version
update_status page 98 line 43, refers to Table 72-4, should be Table 72-5 Status Report Field

SuggestedRemedy

Fix reference to Status report field table in definition of update_status

Response *Response Status* **C**

ACCEPT.

Cl **69A** *SC* **69A.1.1** *P* **201** *L* **32** # 61

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

replace 'are' with 'and': ""Other terms are abbreviations are"" to ""Other terms and abbreviations are""

SuggestedRemedy

replace 'are' with 'and': ""Other terms are abbreviations are"" to ""Other terms and abbreviations are""

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **Figure 74-9** *P* **188** *L* **25** # 62

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

figure 74-9 and 74-8 (both ""FEC (2112,2080) decoding"") would seem to be duplicated, strike one and renumber appropriately.

SuggestedRemedy

Delete duplicate figure

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Strike 74-8 and renumber as appropriate

Cl **73** *SC* **Figure 73-2** *P* **140** *L* **24** # 63

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

Figure 73-2 is called ""PCS idle randomizer"" but has nothing to do with a PCS or idle

SuggestedRemedy

Rename Figure 73-2 to ""DME page bit 49 randomizer""

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.10.1** *P* **153** *L* **13** # 64

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

editorial: 73.10.1 in definition of ack_nonce_match ""acknowledg_match"" should be ""acknowledge_match""

SuggestedRemedy

""acknowledg_match"" should be ""acknowledge_match""

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.10.1** *P* **152** *L* **49** # 65

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

ability_match_word[48:1] and definition are improperly indented.

SuggestedRemedy

Correct indentation of ability_match_word variable and definition

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.6.10.3.3** *P* **115** *L* **21** # 66

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

changebar version, refers to ""Coefficient Update state diagram as depicted in Figure 72-7"" but is Figure 72-9.

non-changebar version
72.6.10.3.3 - line 53 page 99, refers to Figure 72-5, should be 72-6

SuggestedRemedy

Fix referenced figure to refer to actual Coefficient Update state diagram.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Cl **74** *SC* **Figure 74-11** *P* **190** *L* **25** # 67

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

The behavior when FEC Error Indication is not set is not clear to the reader.

(page 36) 45.2.1.84.2.2 defines bit 1.171.1 ""Enable FEC Error Indication"" indicates that if zero ""the error indication function is disabled""(line 30)

74.7.4.5.1 does not clearly state what occurs if 1.171.1=0.

1.171.1 allows forced error indication to the PCS to be enabled or disabled by management. As each FEC block received with forced errors would cause the Clause 49 PCS to loose block_lock, it may be desireable to set 1.171.1=0 for some implementations, however the process followed in this condition is not clearly defined.

Further confusion arises from 74.7.4.5 line 37 page 187, which indicates sh=11 is used to indicate errors.

SuggestedRemedy

1. Either:
A) Update the flow diagram of Figure 74-11 to show behavior when 1.171.1=0 by adding a decision block ""1.171.1=0 ?"" between FEC Decoder and Decoding successful to show configuration check. Add 'yes' transition to the left-hand side ""x1=0 ?"" decision block, and add 'no' transition to continue to the ""Decoding successful ?"" block.

Or
B) Add clarifing language to 74.7.4.5.1 to define behavior when 1.171.1=0.

2)
Correct text in 74.7.4.5 line 37 page 187 from ""to the same value (11),"" to the corrected text ""to the same value (11 or 00),""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add clarifing language to 74.7.4.5.1 to define behavior when 1.171.1=0.

Cl **74** *SC* **74.7.4.6** *P* **191** *L* **50** # 68

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

74.7.4.6 line 50 page 191 indicates ""The default value for variables m=8 and n=4.""

The term 'default value' implies management control, but there is no defined management method for altering the value of m or n, or reading their current values.

SuggestedRemedy

Delete the word 'default' from the final sentance, and rewrite as follows:
""The value for variables ""m"" and ""n"" are as follows, m=8 and n=4.""

Alternatively, define a management method for reading the current values of these variables and writing new values.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Modify text as follow:

Delete the word 'default' from the final sentence, and rewrite as follows:
""The values for ""m"" and ""n"" are as follows, m=8 and n=4.""

Cl **74** *SC* **74.7.4.6** *P* **191** *L* **40** # 69

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

74.7.4.4.1 line 5 page 187 indicates that ""Before each FEC block processing (encoding or decoding) the PN-2112 generator is initialized"" While for proper operation this requirement should be clear, figures 74-9(74-8) indicate that the PN-2112 Generator is xor'd prior to FEC Block Sync.

""74.7.4.6 FEC block synchronization"" and ""Figure 74-12 FEC(2112,2080) block sync and decoding"" make no mention of the requirements of 74.7.4.4.1.

SuggestedRemedy

At a minimum, modify the procedure of 74.7.4.6 as follows, inserting a new item #1 below:
""a) Test a candidate block start position
1) Descramble block using PN-2112 Generator per 74.7.4.4.1
2) Evaluate parity for the potential block
i) If it fails shift candidate by one bit position and try again""

Also, optionally strike the PN-2112 Generator block and XOR junction from Figure 74-9(74-8).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add text to 74.7.4 as proposed.

Do not remove the XOR junction and PN-2112 generator as suggested, instead refer response to comments #109,148 regarding modifications to Figure 74-6, 74-9 that illustrate the initialization at each FEC block start

Cl **73** *SC* **73.7.4.1** *P* **146** *L* **13** # 70

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

How does parallel detection work in the presence of 10GBASE-R FEC?

As FEC resides below the XSBI of a 10GBASE-KR interface, then nothing in clause 73 explicitly forbids parallel detection of a 10GBASE-KR interface with FEC, as a system capable of parallel detecting an FEC encoded KR link would ultimately report sync_status_KR=READY. However, it is not clear that the detected link would be indicated to management as FEC enabled.

SuggestedRemedy

Modify the last sentance of the second to last paragraph in 73.7.4.1 which currently ends:
""the parallel detection function shall set the bit in the link partner ability registers (See 45.2.7.7) corresponding to the technology detected by the parallel detection function.""
This statement refers to a single bit, if FEC parallel detection is to be supported, modify the statement to read:
""the parallel detection function shall set the bit in the link partner ability registers (See 45.2.7.7) corresponding to the technology detected by the parallel detection function, including the presence of FEC via the F0 bit""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add note to indicate that if you parallel detect for 10GBASE-KR, then it is up to the implementation to determine whether to turn on FEC.

Cl **69B** *SC* **69B.2** *P* **207** *L* **25** # 71
Abler, Joe IBM

Comment Type **T** *Comment Status* **R**

reader should be advised that the recommendations for channel attributes have been individually defined and that concurrently taking all attributes to their absolute limits may be beyond the bounds of the standard.

SuggestedRemedy

recommended text will be provided at Feb meeting.

Response *Response Status* **C**

REJECT.

The group was unable to reach consensus on making the change.

Straw Poll # 4
Option #1 - Make the change
Option #2 - Don't make the change

Option 1 - 4
Option 2 - 8

Cl **72** *SC* **72.6.10.2.4.2** *P* **110** *L* **49** # 72
Abler, Joe IBM

Comment Type **E** *Comment Status* **A**

main tap is no longer referred to as gain tap.

SuggestedRemedy

delete "",or gain,""

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.78** *P* **28** *L* **25** # 73
Abler, Joe IBM

Comment Type **T** *Comment Status* **A**

Need to add new bit fields, preset and initialize, to Table 45-57

SuggestedRemedy

update table to include bits 13 & 12. add corresponding subclause defining preset and initialize bits. carry through to clause 45.2.1.80

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.7.1** *P* **120** *L* **22** # 74
Abler, Joe IBM

Comment Type **T** *Comment Status* **A**

transition time in Table 72-9 needs to be updated

SuggestedRemedy

change to 24 - 47ps

Response *Response Status* **C**

ACCEPT.

See 38

Cl **72** *SC* **72.7.1.8** *P* **124** *L* **46** # 75
Abler, Joe IBM

Comment Type **T** *Comment Status* **A**

need to update tx jitter description to include a DCD component.

SuggestedRemedy

update text to specify a max DCD of 0.05UIpp, which is a component of total DJ.

Response *Response Status* **C**

ACCEPT.

Cl **44** *SC* **44.1.1** *P* **19** *L* **49** # 76
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A** *e*

In this draft the optional FEC sublayer is not tied to Backplane Ethernet any more: it's an independent option.

SuggestedRemedy

Add another paragraph: 'An optional FEC sublayer is defined in Clause 74.'

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.1.3** *P* **22** *L* **54** # 77

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

If adding this sentence, the lack of an equivalent for 10G becomes apparent.

SuggestedRemedy

Insert another sentence: 'When set to 0000, bits 5:2 select the use of a 10G PMA/PMD. More specific selection is performed using the 10G PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6) and the Clause 74 FEC control register (Register 1.171) (see 45.2.1.86.2).

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.7.4** *P* **23** *L* **46** # 78

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Because 10GBASE-KR is a serial PMD, the new sentence 'The description of the transmit fault function for the 10GBASE-KR PMD is given in 72.6.8.' contradicts 802.3's 'The description of the transmit fault function for serial PMDs is given in 52.4.8.'. But note the latter is being modified by P802.3aq. Another remedy would be to keep the new sentence for 10GBASE-KR and change 'other serial' to 'other optical serial'.

SuggestedRemedy

Change:
The description of the transmit fault function for 10GBASE-LRM serial PMDs is given in 68.4.8, and for other serial PMDs in 52.4.8.'
to:
The description of the transmit fault function for the 10GBASE-KR PMD is given in 72.6.8, for 10GBASE-LRM serial PMDs in 68.4.8, and for other serial PMDs in 52.4.8.
and delete the sentence:
The description of the transmit fault function for the 10GBASE-KR PMD is given in 72.6.8.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Adopt the proposed remedy and add editors note to say it is an 802.3aq change

Cl **45** *SC* **45.2.1.7.5** *P* **24** *L* **27** # 79

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Because 10GBASE-KR is a serial PMD, the new sentence 'The description of the receive fault function for the 10GBASE-KR PMD is given in 72.6.9.' contradicts 802.3's 'The description of the receive fault function for serial PMDs is given in 52.4.9.'. But note the latter is being modified by P802.3aq. Another remedy would be to keep the new sentence for 10GBASE-KR and change 'other serial' to 'other optical serial'.

SuggestedRemedy

Change:
The description of the receive fault function for 10GBASE-LRM serial PMDs is given in 68.4.9, and for other serial PMDs in 52.4.9.'
to:
The description of the receive fault function for the 10GBASE-KR PMD is given in 72.6.9, for 10GBASE-LRM serial PMDs in 68.4.9, and for other serial PMDs in 52.4.9.
and delete the sentence:
The description of the receive fault function for the 10GBASE-KR PMD is given in 72.6.9.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Adopt the proposed remedy and add editors note to say it is an 802.3aq change.

Cl **45** *SC* **45.2.1.86.4** *P* **37** *L* **5** # 80

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

As for Clause 74 FEC corrected blocks counter, these are non-rollover registers.

SuggestedRemedy

Add sentence as in 45.2.1.86.3: 'These bits shall be held at all ones in the case of overflow.' Add appropriate PICS.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.2.2** *P* **40** *L* **34** # 81

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Name of bit not consistent. Sometimes 'able', sometimes 'ability'. Also, sometimes 'LP' comes before 'Auto-Negotiation', sometimes after. Using 'ability' brings it in line with the majority of Clause 45, line 36 and 7.1.3 'Auto-Negotiation ability'.

SuggestedRemedy

Change 'LP AN able' to 'AN LP ability' here, change 'LP Auto-Negotiation able' to 'AN LP ability' in Table 45-119.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.7** *P* **43** *L* **39** # 82

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

nest

SuggestedRemedy

next

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.100.1** *P* **47** *L* **35** # 83

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

one of three...

SuggestedRemedy

is set (not are set)

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.100.2** *P* **47** *L* **39** # 84

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

'the PHY type': which PHY type?

SuggestedRemedy

Change to 'If at least one Backplane Ethernet PHY type (1000BASE-KX, 10GBASE-KX4 or 10GBASE-KR)' is implemented...'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment 105

Cl **74** *SC* **74.1** *P* **174** *L* **13** # 85

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Each subclause usually has a layer diagram.

SuggestedRemedy

Insert diagram 'Figure 74-1 -10GBASE-R FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model' Copy and modify fig. 50-1. Copy and modify sentence to introduce figure from one of clause 46 upwards (wording varies slightly).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Insert diagram as proposed and provide the following introductory text:

74.3 Relationship to other sublayers
Figure 74-1 depicts the relationships among the 10GBASE-R FEC (shown shaded), the 10 Gb/s MAC and Reconciliation Sublayers, the 10GBASE-R PCS and PMA, the ISO/IEC 8802-2 LLC, and the ISO/IEC Open System Interconnection (OSI) reference model.

Cl **74** *SC* **74.3.1** *P* **177** *L* **27** # 86
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Name of one functional block does not match 74.7.4.

SuggestedRemedy

Change DECODE to DECODER or decoder.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

To be consistent also change FEC ENCODE to FEC ENCODER

Also refer to comment #107

Cl **74** *SC* **74.3.1** *P* **177** *L* **8** # 87
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Do not see why some labels are all-capitals.

SuggestedRemedy

Change to upper/lower case as in body text or table.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

To be consistent, make similar changes to Figure 74-8 which has labels with all-capital letters.

Cl **74** *SC* **74.3.1** *P* **177** *L* **32** # 88
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Something white on top of PMA_SIGNAL.indication?

SuggestedRemedy

Set background of rx_data-group<15:0> to transparent?

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Move the white on top of PMA_Signal.indication

Cl **74** *SC* **74** *P* **174** *L* **1** # 89
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Tweaking the clause title to be more like others e.g. 51, 52, and to get the sublayer have 'FEC' in its name. Removing stray capitals. Do not know exactly what 'Physical Layer signaling systems' is meant to mean. Shortening.

SuggestedRemedy

Preferably, change to:
74. Forward Error Correction (FEC) sublayer for 10GBASE-R
or, to:
74. Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs
or, to:
74. Forward Error Correction (FEC) sublayer for 10GBASE-R Physical Layers
or, to:
74. Forward Error Correction (FEC) sublayer for 10GBASE-R Physical Layer signaling systems

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change Clause 74 title to:

Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs

Cl **74** *SC* **74.7.4.4.1** *P* **187** *L* **5** # 90
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

We've gone 180 pages without using this unnecessary notation; it's a pity to give up now.

SuggestedRemedy

Please change '0x2AAAAAAAAAAA2F8' to 'hexadecimal 2AAAAAAAAAAA2F8' (as in 72.6.10.2.1).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Over taken by events. Refer response to comment #127.

Cl **74** *SC* **74** *P* **179** *L* **49** # 91
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Terminology: sometimes it's 'FEC frame', sometimes 'FEC block'.

SuggestedRemedy

Pick one. I think 'FEC block' is more common.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change all instances of "FEC frame" to "FEC block"

Cl **45** *SC* **45.2.1** *P* *L* # 92
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Clause numbers are arbitrary: can have more descriptive register names.

SuggestedRemedy

Change 'Clause 74 FEC ...'to '10GBASE-R FEC ...' (several times in 45 and 74).

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.7.4** *P* **181** *L* **37** # 93
Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

This sentence is out of place.

SuggestedRemedy

Delete it?

Response *Response Status* **C**

ACCEPT.

Delete the sentence. (line 37,38 page 181)

Cl **74** *SC* **74.3.1** *P* **177** *L* **3** # 94
Dawe, Piers Avago Technologies

Comment Type **ER** *Comment Status* **A**

Fonts smaller than style guide recommends, not in scale with body text.

SuggestedRemedy

There's space to make it all at least 8 point. Suggest you make the major items (sublayer and service interface names) 10 point. Also figs 74-6, 74-9, 74-12. Check other figures e.g. 74-4 'tx_data-group<0> (PMA) tx_data-group<15> (PMA)'

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Change the font size as appropriate in all figures in Clause 74

Cl **30** *SC* **30.5.1.1.14** *P* **16** *L* **51** # 95
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A** *e*

Wrong way. Editorial: should be underlined to show a change to base document.

SuggestedRemedy

Change 'to' to 'of' (underlined). Same in 30.5.1.1.15.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* **74.13.2** *P* **193** *L* **35** # 96

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A** *e*

A FEC receiver sorts blocks into three categories: good ones it thinks don't need correcting, moderate ones that it thinks it can correct, and bad ones that it cannot reliably correct. 'Uncorrected' blocks could be the first, the last, or, literally, their sum. In the base document, 10PASS-TS has 'uncorrectable errors', 30.5.1.1 has 'uncorrectable FEC blocks', but 65.2.3 has (1000BASE-PX FEC) 'uncorrected FEC blocks'. Counting the uncorrectable blocks seems the most sensible choice.

SuggestedRemedy

Change 'uncorrected' to 'uncorrectable' throughout 802.3ap.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Blocks that are uncorrectable are uncorrected by the FEC sublayer. Therefore, when they leave the FEC sublayer they are uncorrected, and either term could apply. Given the lack of a clear precendent, the Task Force has chosen to use "uncorrected."

Appropriate text will be added to explain that the uncorrected blocks are error blocks that are uncorrected.

Cl **45** *SC* **45.2** *P* **21** *L* **17** # 97

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

Now that FEC is a separate sublayer, it could be in the same chip as the PCS, or PMA, or its own chip: it has to be added to the MMD tables, I think.

SuggestedRemedy

In Table 45-1, change '8 through 28 Reserved' to '9 through 28 Reserved' and insert new row '8 Clause 74 FEC for 10GBASE-R'. In Table 45-2, change 'm.5.15:8 Reserved Ignore on read RO' to 'm.5.15:9 Reserved Ignore on read RO', insert new row 'm.5.8 10GBASE-R FEC present 1 = 10GBASE-R FEC present in package 0 = 10GBASE-R FEC not present in package RO'.

Response *Response Status* **C**

REJECT.
While the commenter is correct, the consensus of the committee is that, based on current technologies, the FEC would probably be implemented in the same PCS / PMA / PMD device.

It is possible to split a MMD across two chips, such as independent tx and rx devices.

There is concern regarding allocating an MMD given the dwindling supply to support only a handful of registers.

Strawpoll#1 - reject comment
Y - 5
N - 0
A - majority of room

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **50** # 98

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

FEC bit has wrong address.

SuggestedRemedy

Change 7.21.15 to 7.18.15, 7.18.15:0 to 7.18.14:0? But see another comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change 7.21.15 to 7.18.15, 7.18.15:0 to 7.18.14:0

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **41** # 99
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

This table seems very untidy. There are two rows with the same name, 'Technology Ability Field' and two more that have dual names including this one. The order of bits is not the same as in 73.6. Similarly for the AN LP base page ability registers.

SuggestedRemedy

Would re-ordering the contents of these registers help?

Response *Response Status* **C**

REJECT.
This table needs to be compatible with 802.3an and so cannot be re-ordered.

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **41** # 100
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Confusing bit name. Wrong subclause.

SuggestedRemedy

Change 'Technology Ability Field/Pause' to 'Pause ability'. Change '73.6.5' to '73.6.6'. On p144, change '73.6.6 Pause' to '73.6.6 Pause ability'.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **43** # 101
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Confusing double-name. Clause 28 doesn't have a nonce.

SuggestedRemedy

Change 'Technology Ability Field/Echoed Nonce Field' to 'Echoed nonce field'? Explain what to do with this field in a clause 28 situation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add explanation that this is'Technology Ability Field' when used by Clause 28 and 'Echoed nonce field' when used by Clause 73.

Cl **45** *SC* **45.2.7.7** *P* **43** *L* **41** # 102
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Confusing (and duplicate) bit name. Description is wrong (P802.3anD3.0#82). Wrong subclause.

SuggestedRemedy

Change 'Pause' to 'LP pause ability'. Change description to 'LP is/is not extended next page capable'. Change '73.6.5' to '73.6.6'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Bit names by themselves are not unique within Clause 45. Register name plus bit name is unique.

Correct reference "73.6.5" to "73.6.6" and make sure it is a hot link.

Cl **45** *SC* **45.2.7.7** *P* **43** *L* **34** # 103
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Duplicate bit names.

SuggestedRemedy

Make each name in table 45-121 and Table 45-125 begin with 'LP '.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Added LP prefix to Table 45-121 and Table 45-123

Cl **45** *SC* **45.2.7.100** *P* **47** *L* **17** # 104
Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Status registers are always RO.

SuggestedRemedy

Change all 'R/W' to 'RO' in this table.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.100.2** *P* **47** *L* **39** # 105

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Don't use 'will be' like this.

SuggestedRemedy

Change to 'shall be' and add PICS - or change to 'is'.

Response *Response Status* **C**

ACCEPT.

Change to 'is' in the table and 'shall be' in the text. Also list out the Backplane ethernet PHYs.

So change:
"If the PHY type is implemented, this bit will be set to 1."
to:
"If a 1000BASE-KX, 10GBASE-KX4 or 10GBASE-KR PHY type is implemented, this bit shall be set to 1."

Also see comment 84.

Cl **45** *SC* **45.5.2.3** *P* **49** *L* **1** # 106

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

If 10GBASE-R FEC is its own sublayer and MMD, make it a major option too. Notice there is another major option called 'FEC already: might wish to rename that e.g. PFEC.

SuggestedRemedy

Reinstate subclause title and table row, but change it to:
*RFEC Implementation of 10GBASE-R FEC MMD 45.2.1.86 Yes [ ] No [ ]
Move items MM112 to MM115 to FM1 to FM4 in their own table: I think we need a new subclause '10GBASE-R FEC management functions' (I didn't notice any 10GBASE-R FEC options), suggest it goes just before or after the WIS subclauses. Status becomes RFEC:M. Editorial: subclause references need updating to 45.2.1.86.n.

Response *Response Status* **C**

REJECT.
It is not its own MMD.
PICS naming is local to a (Clause) PICS

Cl **74** *SC* **74.3.1** *P* **177** *L* **26** # 107

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

74.7.4 says there are four functional blocks in FEC yet this figure omits one of them.

SuggestedRemedy

Within FEC sublayer, insert a box above FEC ENCODE, called REVERSE GEARBOX or Reverse gearbox.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In Figure 74-2 modify the title of the block "FEC ENCODE" to read as "REVERSE GEARBOX & FEC ENCODER"

Also refer to comment #86

Cl **74** *SC* **74.6.1** *P* **179** *L* **15** # 108

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

We need to be more accurate than this: 'A value of FAIL denotes that errors have been detected by the Receive process that prevent valid data from being presented to the PCS...' Just 'errors' is not enough. As I understand it, we do not want the signal detect line to toggle for every uncorrected FEC block, still less for every corrected one. Signal detect is supposed to come on at some point definitely below rated sensitivity, indicating a gross problem (no light in an optical PMD, CDR sync loss, or FEC out of block lock), as indicated by 74.6.2.

SuggestedRemedy

Change to:
A value of FAIL denotes that the Receive process has determined that the received signal is so bad that it cannot present any received data to the PCS...'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Provide reference to state machine variable fec_signal_ok

Refer to comment #159 for state machine variable definition

Cl **74** *SC* **74.7.4.4** *P* **186** *L* **36** # 109

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

The PN-2112 generator is not independent as shown: per this clause it has to be synced to the FEC block boundaries.

SuggestedRemedy

Add an arrow from 'Compress Sync bits' or 'Message or Parity Selector' to 'PN-2112 Generator'. Or use a self-synchronous scrambler.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In Figure 74-6 Add an arrow from 'Message or Parity Selector' to 'PN-2112 Generator.

Also refer to comment #148 that proposes similar change to FEC decoder block diagram 74-9

Cl **74** *SC* **74.7.4.1** *P* **187** *L* **25** # 110

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

I'm not sure what this sentence is trying to say: 'Scrambling with the PN-2112 sequence at the FEC codeword boundary is necessary for establishing FEC block synchronization (to ensure that any shifted input bit sequence is not equal to another FEC codeword) and to ensure DC balance.' If it means that the scrambler has to be synchronised to the FEC blocks, I disagree. A self-synchronous scrambler would have worked too.

SuggestedRemedy

Not sure what to suggest as do not understand what was intended.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There is no specific remedy.

A self synchronous scrambler will not work in this case because the error propogation will defeat the error correction property of FEC.

The FEC code is a cyclic code. The cyclic code has a property that a shifted code can be another valid cyclic code. The block lock state machine uses repeated shifting to establishing synchronization. The FEC block is XOR'd with PN-2112 sequence to ensure that a shifted cyclic code is not another valid code word.

A reference will be added to the bibliography in Annex A.

Cl **74** *SC* **74.7.3** *P* **181** *L* **18** # 111

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

This sentence 'The transcode bits are further scrambled (as explained in 74.7.4.2) to ensure DC balance.' contradicts 74.7.4.4 'The resulting payload block including the T bits is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.' and figures 74-6 and 74-9 which show everything being (further) scrambled and de-scrambled. Depending what 'payload' means, 74.7.4.4 and the figures also disagree.

SuggestedRemedy

Move this sentence to line 21 and modify: 'The FEC block is further scrambled (as explained in 74.7.4.2) to ensure DC balance.'. Move the sentence in 74.7.4.4 to follow 'extracted directly.' and modify: 'The whole FEC block is scrambled using the PN-2112 pseudo-noise sequence specified in 74.7.4.4.1.'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer to revised comment #140 for remedy

Cl **74** *SC* **74.7.5.1** *P* **188** *L* **14** # 112

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

The PN-2112 generator is not independent as shown: per this clause it has to be synced to the candidate FEC block boundaries.

SuggestedRemedy

Add an branch of the arrow from Decoder to 'FEC Block Sync', to 'PN-2112 Generator'. Or use a self-synchronous scrambler.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add an branch of the arrow from Decoder to 'FEC Block Sync', to 'PN-2112 Generator' in Figure 74-9.

Also refer response to comments #109,148

Cl **74** *SC* **74.7.5.1** *P* **188** *L* **20** # 113

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

FEC error monitor is an input to 'Reconstruct 64b/66b Blocks', in order to implement bullet b) below. Also per 74.7.4.6 it controls the FEC Block Sync?

SuggestedRemedy

Add arrow from FEC error monitor to 'Reconstruct 64b/66b Blocks'. Consider changing the arrow from Decoder to 'FEC Block Sync', to start from FEC error monitor instead

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add arrow from FEC error monitor to 'Reconstruct 64b/66b Blocks'.
change the arrow from Decoder to 'FEC Block Sync', to start from FEC error monitor instead.

Add arrow from Decoder to FEC error Monitor

Cl **74** *SC* **74.13** *P* **193** *L* **31** # 114

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

To avoid nuisance counting, it may be worth stipulating that if FEC_SIGNAL.indication is FAIL (no signal detect or FEC block sync), then neither counter should count. (But the FEC machine or some of it may still be running: it needs to, or it will never recover.)

SuggestedRemedy

In 74.13.1, change 'corrected FEC blocks processed.' to 'corrected FEC blocks processed when FEC_SIGNAL.indication is OK.' In 74.13.2, change 'uncorrected FEC blocks processed.' to 'uncorrectable FEC blocks processed when FEC_SIGNAL.indication is OK.'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Also refer to comment #159

Make the the corresponding change to State machine and variable definitions (of counters). Provide text to indicate that the counters get updated only when fec_block_lock variable is true.

Cl **74** *SC* **74.10** *P* **192** *L* **32** # 115

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Better than 'Enable FEC'

SuggestedRemedy

FEC enable. Similarly FEC error indication enable, FEC_enable and so on.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Modify text in Table 74-3 and corresponding subclauses in 74 and tables/text 45.2.1.84. Make corresponding changes to Cl.73

Cl **74** *SC* **74.10** *P* **192** *L* **32** # 116

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

This FEC sublayer would be even more useful if transmit and receive could be switched on and off independently. At least two reasons: 1, so useful for diagnostics, debug and conformance testing that every implementation will do it, so might as well have a consistent mechanism to control it; 2, while the transmit and receive paths to the link partner are likely to be similar lengths, there is no reason to expect them to have the same crosstalk or SNR. If the FEC can be switched off on the good side only, it improves latency and thermals. Conveniently, there is no dependency between FEC transmit and receive sides.

SuggestedRemedy

In 45.2.1.86.2 table 45-67, use two more bits to provide Tx, Rx enable masks, respectively. For preference, make them 1.171.2, 1.171.1 respectively (and move FEC error indication enable to 1.171.3). Type R/W, default 1 meaning that side comes on with 1.171.0 FEC enable, 0 meaning it doesn't. Add description here.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Provide 1 FEC capability bit and 1 Request to Turn on bit in the Auto-Neg advertisement page. This will allow the link partners to asymytrically request to turn on FEC.

However the FEC will be turned on both directions only if both sides are capable and any one side requests turn on.

There will be only one FEC Enable bit. It is important for one side of the link partner to request FEC to be turned on, if it finds a problem, but it does not have the burden of managing asymmetric operation.

Make appropriate changes to Clauses 73 and 45

Cl **74** *SC* **74.15** *P* **194** *L* **2** # 117

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

PICS does not match main clause title. FEC does not contain a medium.

SuggestedRemedy

Keep in step with main clause title: at line 2, 8 and 37.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make appropriate changes to lines at 2,8,37 on page 195 to match the Clause 74 title:

Protocol Implementation Conformance Statement (PICS) proforma for Clause 74, Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs.

Also refer to comment #89 for new title for Cl.74

Cl **74** *SC* **74.7.4.5.1** *P* **188** *L* **36** # 118

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

New term 'configuration option' doesn't appear in 802.3 parts 1 or 4. It would need explanation.

SuggestedRemedy

Delete 'configuration' about 4 times, and '(from configuration)' once, change 'Configuration' to 'Option' once in PICS.

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.9** *P* **192** *L* **34** # 119

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

Do not see why the FEC error indication is so necessary that it must be mandatory, and then can be turned off (or default off).

SuggestedRemedy

Change 'The FEC sublayer shall have the' to 'It is recommended that the FEC sublayer shall have the'. Add a FEC error indication ability bit 1.170.1 and description to 45.2.1.86.1. Change status of PICS item M3 to FEC:O.

Response *Response Status* **C**

REJECT.

If FEC is implemented, the FEC sublayer should be able to indicate known errors to the upper layer. This allows the upper layers to discard the frame which is known to have an uncorrectable error. This is consistent with other clauses that propogate known errors to the upper layers. (Example Clauses 49, 50)

Also refer response to comment #52

Cl **00** *SC* **00** *P* **1** *L* # 120

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A** *e*

Editorials

SuggestedRemedy

In context of FEC, some more 'KR's to be changed to 'R's. Some stray capitals. Some subclause titles missing especially in Clause 30. Code Word -> Codeword

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There are some proper occurences of "KR" in the context of FEC, such as the capability bits in the context of autonegotiation. The editor will review the document for any improper occurences.

"Code Word" will be changed to "codeword."

Reminder to editor - review inclusion of all subclause titles.

Cl **74** *SC* **74.5.2** *P* **178** *L* **46** # 121

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Not 16 payload bits (ex FEC parity), not necessarily valid, not 'when delineated' but probably later after correction and some latency.

SuggestedRemedy

Change 'The FEC sends one rx_data-group<15:0> to the 10GBASE-KR R PCS whenever it has delineated exactly 16 bits of valid payload information from the incoming FEC data stream received from the PMA sublayer.' to 'The FEC sends one rx_data-group<15:0> to the 10GBASE-KR R PCS for each 16 bits received from the PMA sublayer.'

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.7.4.1** *P* **181** *L* **49** # 122

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

No test mode any more.

SuggestedRemedy

Delete 'When the transmit channel is operating in normal mode,' here, and 'When the receive channel is in normal mode of operation' in 74.7.4.5.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **1** # 123

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

I don't believe there is enough information here, for such complicated multi-use registers.

SuggestedRemedy

Add sentences of explanation, field by field in separate subclauses, as is Clause 45 style.

Response *Response Status* **W**

REJECT.
It is not clear what needs to be addressed from the supplied comment and suggested remedy.

This is an amendment to 802.3an, and 802.3an content will not be duplicated in 802.3ap.

Motion #2
Technical (>=75%)
Move to accept this response.
M - Schelto van Doorn
S - John D'Ambrosia

All
y - 12
n - 0
a - 2

Motion Passes

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **1** # 124

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **A**

Which AN do these registers apply to? Clauses 28 and 73 are mentioned: what about 37?

SuggestedRemedy

Add sentence of explanation: 'The AN advertisement register is related to Clause 28, Physical Layer link signaling for Auto-Negotiation on twisted pair, or Clause 37, Auto-Negotiation function, type 1000BASE-X, or Clause 73, Auto-Negotiation for Backplane Ethernet, according to ...' [what? PHY type?] Or if Clause 37 doesn't apply, say so explicitly. Add a correlation table between different ANs and PHY types (if that is what matters), or refer to one elsewhere.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

These registers do not apply to Clause 37.

Add a sentence:

"Note: Clause 37 1000BASE-X autonegotiation is controlled through Clause 22 registers."

Cl **74** *SC* **74.6.3** *P* **179** *L* **25** # 125

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

This sentence 'The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.' might be true (and very obvious) but it is offensively unhelpful. Especially as the effect of receipt is not well specified, at present, it needs to be, and you have said that there is only one possible FEC client.

SuggestedRemedy

Change to:
This primitive is received and acted on by the 10GBASE-R PCS in the same way as PMA_SIGNAL.indication or WIS_SIGNAL.indication. See 49.2.

Response *Response Status* **W**

REJECT.

The current definition is consistent with the definition in Clause 51.2.2.3 (PMA sublayer).

The mapping of primitives 74.3 and 74.4 means the same thing as the requested by the commenter.

Motion #6
Move to accept the response
move - Brad Booth
Second - John D'Ambrosia
Tech (>=75%)

Motion passes by acclamation.

Cl **74** *SC* **74.6.1** *P* **179** *L* **45** # 126

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **A**

'guaranteed to correct an error burst of up to 11 bits per block.' Need to say more. Is this 11 bits on the line, 11 after the x3 error multiplication of the PN-2112 descrambler, or what? Also, what is the number of errored bits per block that are guaranteed to be DETECTED?

SuggestedRemedy

Please add the missing information.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

The PN-2112 is a sidestream scrambler and does not propogate errors. So 11 errors on the wire will be same as descramble data.

If there is one error burst which spans more than 11 bits or if there are multiple error burst then there is no guarantee of detection or correction.

A reference will be added to the bibliography in Annex A for reference on this type of FEC code.

Cl **74** *SC* **74.7.4.4.1** *P* **187** *L* **5** # 127

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **A**

This draft does not specify how the hex number is mapped to the shift register.

SuggestedRemedy

Add the missing information: '0x2AAAAAAAAAA2F8, where the least significant bit maps to S0|S57 and the most significant non-zero bit to maps to S57|S0.'

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Overtaken by events. Refer to comment #12 that proposes a different mechanism to maintain DC balance.

Cl **74** *SC* **74.7.4.4** *P* **185** *L* **38** # 128

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

Having a second scrambler in the FEC as well as the Clause 49 one, still running, costs heat in the silicon (if PCS and FEC are in the same place) and degrades performance.

SuggestedRemedy

On the transmit side, use a reverse scrambler as well as a reverse gearbox to get back to the unscrambled 64b/66b. Transcode and add FEC parity bits as currently. Now use the clause 49 self-synchronous scrambler polynomial on the whole stream of FEC blocks. On the receive side, use the Clause 49 self-synchronous scrambler polynomial to descramble, do FEC decoding, rescramble per Clause 49. (Alternatively, convince me that this is a bad idea!)

Response *Response Status* **W**

REJECT.

Refer response to comment #141.

Cl **69A** *SC* **3** *P* **176** *L* **45** # 129

Valliappan, Magesh Broadcom

Comment Type **TR** *Comment Status* **A**

The last line of the paragraph - ""and no more than two adjacent BERm values shall exceed BERs."" does not make sense.

I believe this line is present only to allow random test failures. It should be upto the user to run the test for sufficient time to get a high confidence BER measurement. This kind of verbiage is usually not present in similar tests like jitter tolerance.

SuggestedRemedy

Remove ""and no more than two adjacent BERm values shall exceed BERs""

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **6.10.2.5** *P* **96** *L* **20** # 130

Valliappan, Magesh Broadcom

Comment Type **TR** *Comment Status* **A**

Fixed pattern training sequence can lead to sub optimal performance.

During training, if the aggressor transmitters are synchronous (running of the same RefClk), and the delays between them are aligned, FEXT and NEXT can not be separated from equalizable ISI. This is because all the transmitters are sending the same PN random bits.

The DFE, TXFIR and CDR can mistrain during startup, potentially leading to sub optimal performance at showtime, when independent scrambled data is being transmitted. Sub-optimal DFE taps, may be fixed by continuing to train
the taps after the end of training, but a glitch in performance is likely. Sub-optimal TXFIR can not be recovered from without a restart.

The same problem can happen (in a smaller scale) during training, if the frequency offset between RefClks is small like 2 ppm. The clock phase moves by 1 bit time every 125 training blocks. So there could be times when the transmitted bits and the FEXT/NEXT source bits are the same for several blocks.

SuggestedRemedy

Possible solution is to use a continuously running PRBS training sequence, interrupted by the manchester encoded transmitter config data. Transmitters must be set up with independent randomly generated seeds, to make sure they do not sync up.

Sampling the PRBS sequence at intervals of powers of 2 still produces a valid PRBS sequence and can be used for a sampling based adaptive algorithm that needs to know the transmitted bits.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Straw Poll #2
Option #a - Seeded short scrambler (status quo)
Option #b - free running polynomial (proposed change)

a - 0
b - 8
abstain - 9

Implement the following changes-

72.6.10.1 Training Frame Structure

From line 27, remove -
"The frame marker pattern does not appear in either the control channel or training pattern."

72.6.10.2.1 Frame marker

From Line 50, modify -

"This pattern does not appear in the control channel or training pattern and therefore serves as a unique indicator of the start of a training frame."

to

"This pattern does not appear in the control channel and is not expected to appear in the training pattern in consecutive training frames and therefore serves as an indicator of the start of a training frame."

72.6.10.2.6 Training pattern

Replaced by -

"The training pattern shall be a 512 octet pattern consisting of 4096 bits from the output of a Pseudo-Random Bit Sequence of order 58 generator.The PRBS pattern generator shall produce the same result as the implementation shown in Figure 72-3. This implements the bit stream produced by the polynomial:
G(x) = 1 + x^39+x^58

(Insert figure from Clause 49, Figure 49-8 and remove input bit stream arc)

Each bit of the training pattern is transmitted as a single 10.3125 Gbaud symbol. At the end of each training pattern, the state of the PRBS pattern generator shall be preserved to seed the start of the next training pattern, such that consecutive training patterns form a continuous PRBS sequence. Before the first training frame, it is recommended that the initial seed of the pseudo-random generator be generated by a random process to reduce the probability of adjacent transmitters generating correlated bits. "

Cl **72** *SC* **7.1.9** *P* **106** *L* **44** # 131

Valliappan, Magesh Broadcom

Comment Type **TR** *Comment Status* **A**

Transmitter jitter should be specified with a lower frequency for the high pass filter.

6MHz is proportionately scaled up from 1.875MHz for CX4. CX4 used 8B/10B code and a cleaner receive eye. Both of these enabled a high bandwidth CDR to operate with small self jitter. In 10GBase-KR, with 64B/66B, there are potentially long runs with few transitions and the phase information can be corrupted by increased xtalk and reflections. These effects increase the CDR jitter in the receiver.

Also, the serial 10G transceivers specified in Clause 52 use a filter with 3dB at 4MHz.

SuggestedRemedy

Change the high pass filter 3dB frequency to 4MHz.

Response *Response Status* **C**

ACCEPT.

Straw Poll#
High pass corner frequency at
a. 6 MHz
b. 4 MHz

a - 2
b - 9
abstain -

Cl **69A** *SC* **3** *P* **176** *L* **3** # 132

Valliappan, Magesh Broadcom

Comment Type **TR** *Comment Status* **A**

The PHY vendor should be allowed to choose the frequency at which the extrapolated offset is computed. Forcing it to f1 artifically favors certain receive filter configurations.

SuggestedRemedy

Allow the frequency at which extrapolated offset is computed to be anywhere between f1 and 0.6*fs

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

On page 204 line 35, change:

"Set the interference generator frequency to f1 and amplitude to a non-zero value such that the measured BER, BERM, is less than BERS."

to:

"Set the interference generator frequency to a value between f1 and 0.6*fs which is not an integer sub multiple of fs, where fs is the signaling speed of the port type under test. Set the interference genertator amplitude to a non-zero value such that the measured BER, BERM, is less than BERS."

Cl **71** *SC* **7.1** *P* **85** *L* **43** # 133

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

figure reference of note 1 is incorrect

SuggestedRemedy

change to Figure 71-4

Response *Response Status* **C**

REJECT.

This is a Frame compare issue. The ref to fig 71-3 is correct.

Cl **00** *SC* *P* *L* *#* 134

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

Page # total at bottom wrong

SuggestedRemedy

Response *Response Status* **C**

REJECT.

This is an artifact of the compare document. The clean version is OK

Cl **72** *SC* **7** *P* **120** *L* **29** *#* 135

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **A**

Figure reference for note 1 is incorrect.

SuggestedRemedy

should be fig 72-11

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

New figure is Fig 72-8

Cl **69A** *SC* **2.2** *P* **203** *L* **54** *#* 136

D'Ambrosia, John Tyco Electronics

Comment Type **TR** *Comment Status* **A**

No channel loss (SDD11 / SDD22) is specified for the Test channel

SuggestedRemedy

SDD11 /22 = -20 dB from fmin to f2
See dambrosia_01_0206

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In 69A.2.2Test channel:

change:
"The test channel is specified with respect to transmission magnitude response, ILTC."

to

"The test channel is specified with respect to transmission magnitude response, ILTC, SDD11 and SDD22."

Change:

"The test channel shall have mTC greater than 1.0."

to:

"The test channel shall have mTC greater than 1.0, and both SDD11 and SDD22 less than -20dB from fmin to f2."

Cl **69A** *SC* **2.1** *P* **203** *L* **15** # 137

D'Ambrosia, John Tyco Electronics

Comment Type **TR** *Comment Status* **A**

For 10GBASE-KR, equalization equivalent to a three-tap.... meeting the requirements of 72.7.1.10 shall be included.

This statement seems constrained by the condition of 69a.2.1, which states that the amplitude may be no greater than the minimum transmitter amplitude. Post cursor equalization via the transmitter is limited by this constraint.

SuggestedRemedy

Change 1st paragraph
Add at beginning of 1st sentecne ""for 1000BASE-KX and 10GBASE-KX4

Add text of 69a.2.1

For 10GBASE-KR the signal delivered by the pattern generator will be constrained by the protocol and associated limited defined by 72.6.10.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add to Annex69A.2.1, a statement that for 10GBASE-KR the peak-to-peak output differential voltage shall be no more than 800mv, regardless of equalization setting, as adjusted by the gain, btc, defined in 69A.2.2.

Editor will also make clear that the existing statement applies to 1000BASE-KX and 10GBASE-KX4.

Cl **74** *SC* **74.7.4.2** *P* **182** *L* **11** # 138

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

As noted in another comment, the draft contradicts itself when describing the relationship between the FEC parity process and the scrambler. Also it puts the scrambler between the FEC and the line, which makes the FEC less effective. On reception, the FEC error correcting should act directly on the received bit stream: any descrambler can follow that. There is no point scrambling the 32 parity bits: they are well randomized already. This proposed remedy can help avoid the difficulty of saying what is the encoder, the transcoder, and the scrambler, or is one part of another: they become separate things

SuggestedRemedy

At 74.7.3, change 'The transcode bits are further scrambled (as explained in 74.7.4.2) to ensure DC balance. The 32 sequential 64b/66b blocks are transcoded in this fashion, and then 32 bits of FEC parity are computed for them. The 32 transcoded words and the 32 FEC parity bits constitute an FEC block.' to 'The 32 sequential 64b/66b blocks are transcoded in this fashion to create a 2080-bit FEC payload. This block is scrambled (as explained in 74.7.4.2) to remove the DC unbalance of the T bits. Then, 32 bits of FEC parity are computed for this scrambled payload and appended to form a 2112-bit FEC block.'. At 74.7.4.2, change 'The FEC Encoder compresses the two sync bits to one transcode bits as explained in 74.7.3. The resulting 32 x 65b = 2080 bits with the frame format as shown in Table 74û2 are fed to the (2112, 2080) encoder, which produces 32 parity-check bits. The parity check bits are appended to the end of the FEC frame. The FEC frame is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1. and sent to the PMA interface.' to 'The transcoder compresses the two sync bits to one transcode bits as explained in 74.7.3. The resulting 32 x 65b = 2080 bits with the frame format as shown in Table 74û2 are scrambled by a block-synchronous scrambler using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1. The resulting 2080-bit FEC payload are fed to the (2112, 2080) encoder, which produces 32 parity-check bits. The parity check bits are appended to the end of the FEC payload to form the 2112-bit FEC frame. which is sent to the PMA interface.'. At 74.7.4.4, change 'The block diagram of the FEC Encoder is illustrated in Table 74û2. The 32 x 65 bit payload blocks are encoded by the (2112,2080) code. This code is a shortened cyclic code that can be encoded by generator polynomial g(x). The resulting payload block including the T bits is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.' to 'The 2080-bit FEC payload blocks are encoded by the (2112, 2080) code. This code is a shortened cyclic code that can be encoded by generator polynomial g(x).'. Modify figures 74-6 and 74-9 to have the scrambler act on the' 65b blocks' not the PMA signal.

Response *Response Status* **W**

REJECT.

Refer to comment #12 that proposes a mechanism to XOR T bit with data bit 8 to ensure DC balance. The FEC encoder encodes the 32x65b payload which has DC balance. So XORing with PN-2112 sequence now has only one purpose i.e, to aid in establishing block sync

Having a PN-2112 side stream scrambler does not reduce the error correction properties of

the FEC because it does not propagate errors.

Refer to comment #110

Motion #5
Move to accept response
move - Pat Thaler
Second - Schelto van Doorn
Technical (>=75%)

Motion passes by acclamation.

Cl **73** *SC* **73.8** *P* **149** *L* **12** # 139

Dawe, Piers — Avago Technologies

Comment Type **TR** *Comment Status* **R**

This comment picks up D2.0 comment 539 which was never completed. The draft says 'The management interface is used to communicate Auto-Negotiation information to the management entity. The clause 45 Management Data Input/Output (MDIO) interface shall be used for logical interface to access the device registers for Auto-Negotiation and other management purposes. The clause 45 MDIO electrical interface is optional....'
There's a contradiction here: 'shall be used' and 'optional'. The latter is right per 45.1: 'The MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.'
Also, station management is optional per 30.1,
'In CSMA/CD no peer management facilities are necessary for initiating or terminating normal protocol operations or for handling abnormal protocol conditions. Since these activities are subsumed by the normal operation of the protocol, they are not considered to be a function of Layer Management and are, therefore, not discussed in this clause. Implementation of part or all of Layer Management is not a requirement for conformance to any other clause of this standard.'
So the 'shall' has to go. Is Auto-Negotiation a 'management purpose'? Isn't it automatic (PHY doesn't need management's help to use it)? Editorials: 'state variable' not 'state diagram variable', capital Clause 45, paragraph ends with two full stops.

SuggestedRemedy

Rewrite paragraph: 'A management interface may be used to communicate Auto-Negotiation information to a management entity. The optional Clause 45 Management Data Input/Output (MDIO) interface is recommended for access to the device registers for Auto-Neg

Response *Response Status* **W**

REJECT.
Accept editorial comments.

For backplane Ethernet devices, provision of the management registers is mandatory though provision of the electrical interface is optional. Autonegotiation does require management intereaction with the PHY to complete because link code words must be read from and written to advance negotiation process.

It is valid for a portion of the standard such as a PHY to require implementation of a feature that is optional for other parts of the standard. For instance, next page support is optional for clause 28 AN and is mandatory for 1000BASE-T. There is no conflict in support for the logical interface being optional in Clause 45 and mandatory for Clause 73.

Motion #1
Technical (>=75%)
Move to accept response.
Moved - Pat Thaler
Second- Schelto van Doorn

All
Y- 15
N- 0
A- 2

motion passes

Cl **74** *SC* **74.7.3** *P* **181** *L* **18** # 140

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

(Revised comment) How much should be scrambled? This sentence 'The transcode bits are further scrambled (as explained in 74.7.4.2) to ensure DC balance.' contradicts 74.7.4.4 'The resulting payload block including the T bits is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.' and figures 74-6 and 74-9 which show everything being (further) scrambled and de-scrambled. Depending what 'payload' means, 74.7.4.4 and the figures also disagree.

SuggestedRemedy

If you go with scrambling everything (not optimum): Move this sentence to line 21 and modify: 'The FEC block is further scrambled (as explained in 74.7.4.2) to ensure DC balance.'. Move the sentence in 74.7.4.4 to follow 'extracted directly.' and modify: 'The whole FEC block is scrambled using the PN-2112 pseudo-noise sequence specified in 74.7.4.4.1.'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The first part of remedy is overtaken as proposed in comment #12.
Modify line 21 as appropriate.

Modify text in 74.7.4.4 (line 38, page 185) as follows:
"The FEC block is scrambled using the PN-2112 pseudo-noise sequence specified in 74.7.4.4.1"

Cl **74** *SC* **74.7.4.4** *P* **185** *L* **38** # 141

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

(Revised comment) Having a second scrambler in the FEC sublayer, as well as the Clause 49 one, still running, costs heat in the silicon (if PCS and FEC are in the same place) and (depending how it's done) degrades performance.

SuggestedRemedy

On the transmit side, use a reverse scrambler as well as a reverse gearbox to get back to the unscrambled 64b/66b. Transcode and use the Clause 49 self-synchronous scrambler polynomial to scramble the stream of 2080-bit payloads. On the receive side, use the Clause 49 self-synchronous scrambler polynomial to descramble, do 65/66 transcoding, rescramble per Clause 49. Delete the PN-2112 scrambler. (Alternatively, convince me that this is a bad idea!)

Response *Response Status* **W**

REJECT.

Refer to comment #12

The PN-2112 is required to establishing block sync. Refer to response to comment #138, 110

Motion #7
Technical (>=75%)
Move - John D'Ambrosia
Second - Pat Thaler
Move to accept response.

Motion passes by acclamation.

Cl **69B** *SC* **69B.4** *P* *L* # 142

Ghiasi, Ali Broadcom

Comment Type **TR** *Comment Status* **A**

Unresolved comment 127 from D2.1

SuggestedRemedy

Apply resolution based on D2.1

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

See response to comment #40

Cl **72** *SC* **7.2** *P* **128** *L* **24** # 143

Ghiasi, Ali Broadcom

Comment Type **TR** *Comment Status* **R**

10GBaseKR require to have maximum non-DDJ jitter and a comprehensive jitter tolerance

SuggestedRemedy

Propose that receiver must be able to operate with 0.45 UI of non-DDJ jitter. Currently the transmitter is specified to be tested with certain jitter high pass filter, but the receiver are not tested against this low frequency jitter
which can be several UI. Propose to use sinusoidal jitter mask similar to IEEE 802.3ae clause 52 with corner frequency matching transmitter high pass (to simplify the 802.3ae mask jitter from high frequency corner 4-40 MHz can be set to fix 0.05 UI).

Response *Response Status* **W**

REJECT.

The same comment has been received and addressed by the Task Force for D2.0 and D2.1. It is not addressing changed text, and is beyond the scope of the recirculation.

Cl **69B** *SC* **69B.4** *P* **208** *L* # 144

Thaler, Pat Broadcom

Comment Type **TR** *Comment Status* **A**

This comment is in support of unresolved disapprove comment 127. The channel is not fully specified enough to ensure vendors will be able to produce interoperable components.

SuggestedRemedy

Return loss should be specified.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment #40

Cl **72** *SC* **72.7.2.1** *P* *L* # 145

Thaler, Pat Broadcom

Comment Type **TR** *Comment Status* **R**

This comment is in support of unresolved disapprove comment 31 by Charles Moore. It is the responsibility of the task force to produce a draft with the specifications necessary for interoperability.

The comment response doesn't say that the current specifications are enough to do that. If there is a flaw, it should be fixed before we create a standard even if the commenter doesn't have a solution.

SuggestedRemedy

Response *Response Status* **U**

REJECT.

See Comment #15.

Cl **73** *SC* **73.4** *P* **164** *L* **28** # 146

Thaler, Pat Broadcom

Comment Type **TR** *Comment Status* **A**

Executing the comment resolution last time that deleted the next page ability flags broke the state diagram. Now if one side sets the NP flag in the base page and the other doesn't one device will proceed to next page exchange and the other will go to bring up the link.

SuggestedRemedy

Delete desire_np variable.
This will result in a state diagram where next pages are exchanged after base page if either side sets the NP flag. This is the same behavior that is used for additional next page exchanges.

Response *Response Status* **C**

ACCEPT.

Cl **73A** *SC* **General** *P* **215** *L* *#* 147

Thaler, Pat Broadcom

Comment Type **TR** *Comment Status* **A**

Clause 73A was ommitted from the change marked version - normally I thought the change marked version is a full draft and includes clauses with no changes.

When we added clause 73A we forgot to make the modifications to these pages for extended next page format.

SuggestedRemedy

Change these to send the OUI and Phy identifiers packed into the 48 bit next page in the same fashion as for extended next pages in Clause 28 (i.e. using only the bits that are not in the flag bit positions) for best compatibility with managers that handle both backplane and Clause 28 PHYs.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. See #41 and #42

Cl **74** *SC* **74.7.4.5.1** *P* **188** *L* **10** *#* 148

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

In the FEC decoder Block diagram in figure 74-9, draw a line from FEC block sync to PN-2112 generater to illustrate the initialization of seed value at the start of every FEC frame

SuggestedRemedy

In Figure 74-9, draw a line from FEC block sync to PN-2112 generator with arrow pointing towards PN-2112 generator.

Response *Response Status* **C**

ACCEPT.

Also refer to comment #109 that proposes similar change to FEC encoder block diagram 74-6

Cl **73** *SC* **73.2** *P* **138** *L* **18** *#* 149

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

In figure 73-1 below the ""Medium"" There is a reference to 100Mb/s. Change this to ""1Gb/s or 10Gb/s""

SuggestedRemedy

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.7.1** *P* **179** *L* **44** *#* 150

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Rephrase line 44 to read as follows:

""This shortened cyclic code (2112,2080) is guaranteed to correct an error burst of up to 11 bits per block"".

SuggestedRemedy

as per comment

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Rephrase line 44 to read as follows:

The shortened cyclic code (2112,2080) is guaranteed to correct an error burst of up to 11 bits per block

---

Cl **74** *SC* **74.11** *P* **193** *L* **1** *#* 151

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

The title of this subclause 74.11 ""Test pattern mode"" is ambiguous because FEC sublayer does not provide test pattern functionality only 10GBASE-R PCS provides this function. This is just an informative text to mention that 10GBASE-R PCS provides this function.

Fix the title as suggested.

SuggestedRemedy

Change the title to read as follows:

74.11 10GBASE-R PCS Test pattern mode

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the title 74.11 to read as follows:

74.11 10GBASE-R PHY Test pattern mode

Cl **74** *SC* **74.7.4.3** *P* **185** *L* **1** # 152

Ganga, Ilango Intel

Comment Type **ER** *Comment Status* **A**

Redraw Transmit bit ordering Figure 74-4 to include 16 bit data groups from PCS function. Also show the bit ordering for 64b/66b sync bits in the diagram

SuggestedRemedy

Redraw FEC transmit bit ordering figure as attached.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.86.3** *P* **36** *L* **38** # 153

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

The Clause 74 FEC corrected blocks counter (Register 1.172, 1.173) is a 32-bit counter and two 16 bit registers are used to read the value through MDIO interface.

So provide text to indicate the reading sequence and that the Second register is latched when the first register is read.

SuggestedRemedy

Add the following text to the end of subclause 45.2.1.86.3:

Registers 1.172, 1.173 are used to read the value of 32-bit counter. When registers 1.172 and 1.173 are used to read the 32-bit counter value, the register 1.172 is read first, the value of the registers 1.173 is latched when (and only when) register 1.172 is read and reads of registers 1.173 returns the latched value rather than the current value of the counter.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.86.4** *P* **37** *L* **6** # 154

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

The Clause 74 FEC uncorrected blocks counter (Register 1.174, 1.175) is a 32-bit counter and two 16 bit registers are used to read the value through MDIO interface.

So provide text to indicate the reading sequence and that the Second register is latched when the first register is read.

SuggestedRemedy

Add the following text to the end of subclause 45.2.1.86.3:

Registers 1.174, 1.175 are used to read the value of 32-bit counter. When registers 1.174 and 1.175 are used to read the 32-bit counter value, the register 1.174 is read first, the value of the registers 1.175 is latched when (and only when) register 1.174 is read and reads of registers 1.175 returns the latched value rather than the current value of the counter.

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* *P* **193** *L* **54** # 155

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Provide a sample FEC frame(s) to ensure different implementations encode properly as in Clause 74.

Provide an informative annex or informative text at the end of clause 74 with a sample FEC frame(s).

SuggestedRemedy

Provide an informative annex or informative text at the end of clause 74 with a sample FEC frame(s).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Provide an informative annex 74A with one sample FEC block with 2112 bits in hexadecimal format. Make sure to label the bit ordering

Cl **74** *SC* **74.7.4.5** *P* **187** *L* **48** *#* 156

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Provide Receive bit ordering figure to illustrate proper bit ordering in the FEC decoder function.

SuggestedRemedy

Add FEC Receive bit ordering Figure to subclause 74.7.4.5 as shown in the attached document.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer to comment #12 Make appropriate changes if any to indicate the scrambling of transcode bit

Cl **74** *SC* **74.7.4.5.1** *P* **190** *L* **1** *#* 157

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

There is no need to have a state machine to define the value of x1 bit. Also the state machine does not completely define the sync bits during uncorrectable error condition for entire FEC block. Remove Figure 74-11 and provide this information to the text on page 188 line 39.

SuggestedRemedy

Modify the text (subclause 74.7.4.5.1, page 188 line 39) to define the reconstruction of sync bits as follows:

a) If decoding is successful and the received transcode bit (x1) is 1 then the sync bits take a value of {x1,x0} = 10 or if the received transcode bit (x1) is 0 then the sync bits take a value of {x1,x0} = 01.
b) If configuration is set to indicate error to PCS layer and the received FEC block has uncorrectable errors then the sync bits for the entire FEC block take a value of {x1, x0} = 11.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer response to comment #52

Cl **74** *SC* **74.7.4.5.1** *P* **188** *L* **40** *#* 158

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Only Sync bits value of ""11"" is used to indicate error to PCS layer. Remove ""00"" from line 40: b) reconstruct sync bits to additional codes ô00ö and ô11ö, if decoding error occurred.

SuggestedRemedy

Rephrase line 40 to read as follows:
b) reconstruct sync bits with code ô11ö, if decoding error occurred.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

This is complimentary to comment #52.

Cl **74** *SC* **74.7.4.6** *P* **191** *L* **3** # 159

Ganga, Ilango Intel

Comment Type **TR** *Comment Status* **A**

Redraw FEC sync state machine as per state diagram conventions in Clause 1.2

Also refer to comment #21181

SuggestedRemedy

Redraw FEC sync state machine (figure 74-12) as per state diagram conventions defined in 1.2

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See ganga_01_0206.pdf

Delete flow diagram 74-12 and replace with diagram from ganga_01_0206.pdf with the following changes -

1. Delete the correctable parity state
2. Replace parity_uncorrectable with parity_bad
3. Delete parity_correctable
4. Correct FEC_PARITY_CHECK function.
5. Sort variables definitions alphabetically.
6. Move correctable_error and uncorrectable_error counters out of state machine and indicate they only count when fec_block_lock is "true".

Make appropriate changes to text in subclause 74.7.4.6 FEC block synchronization to be consistent with state machine.

Make appropriate changes to other text that uses these variables. For example "corrected blocks counter" etc.

Cl **74** *SC* **74.7.4.5.1** *P* **188** *L* **44** # 160

Ganga, Ilango Intel

Comment Type **TR** *Comment Status* **A**

This FEC code (2112,2080) is guaranteed to correct an error burst of up to 11 bits per block.

So the FEC decoder implementaitons shall be able to correct up to a minimum of 11 bit burst errors in order to achieve the target performance.

Provide a normative text in subclause 74.7.4.5.1 to indicate this.

SuggestedRemedy

Provide the following normative text to the end of subclause 74.7.4.5.1 and add corresponding PICS

""The FEC code (2112, 2080) is guaranteed to correct up to 11 bit burst errors per block as specified in 74.7.1. The FEC (2112, 2080) decoder implementations shall be able to correct up to a minimum of 11 bit burst errors per FEC block.""

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.6.2** *P* **133** *L* **38** # 161

Geoff, Thompson Nortel

Comment Type **TR** *Comment Status* **R**

Page/Line ref is to 2.1
Pile on Barass #56
I agree with Hugh that 10E-12 is insufficient for a backplane system.

SuggestedRemedy

Response *Response Status* **W**

REJECT.

Refer to comment #39.

Cl **00** *SC* *P* *L* *#* 162

Geoff, Thompson Nortel

Comment Type **ER** *Comment Status* **A** *e*

The draft does not conform to (What I hoped) was the firmly established 802.3 practice of:
1) Dating all drafts (to the day) on each page <==========<<<<<
2) Dating the cover sheet <==========<<<<<
3) Including an explanation on the cover sheet of where this draft fits into the process
4) Including an expiration date for the draft

As well as the Style Guide directives:
""Remember to include the standards designation, the draft number, and the date at the top right of every page.""

SuggestedRemedy

Add the date of the draft to the cover sheet.
Use the standard page template for drafts which (a) conforms to the page information if the Style Guide and (b) puts a date on each page.

Response *Response Status* **W**

ACCEPT.

Cl **99** *SC* *P* **1** *L* **34** *#* 163

Geoff, Thompson Nortel

Comment Type **ER** *Comment Status* **A** *e*

The draft does not conform to (What I hoped) was the firmly established 802.3 practice of:
1) Dating all drafts (to the day) on each page
2) Dating the cover sheet
3) Including an explanation on the cover sheet of where this draft fits into the process <==========<<<<<
4) Including an expiration date for the draft

SuggestedRemedy

Revise the text and amend the format of the cover page to include information regarding where the draft fits into the sequence of events of the balloting process. I suggest that you refer to any one of a number of 802.3 drafts from the pst or present for appropriate examples of this information

Response *Response Status* **W**

ACCEPT.

Cl **99** *SC* *P* **1** *L* **35** *#* 164

Geoff, Thompson Nortel

Comment Type **ER** *Comment Status* **A** *e*

The draft does not conform to (What I hoped) was the firmly established 802.3 practice of:
1) Dating all drafts (to the day) on each page
2) Dating the cover sheet
3) Including an explanation on the cover sheet of where this draft fits into the process
4) Including an expiration date for the draft <==========<<<<<

SuggestedRemedy

Add an expiration date for the draft to the end of the explanation referred to in item 3. (This was an IEEE requirement at one time. I still think it is a very good idea.)

Response *Response Status* **W**

ACCEPT.

Cl **99** *SC* *P* **2** *L* **1** *#* 165

Geoff, Thompson Nortel

Comment Type **ER** *Comment Status* **A** *e*

Abstract is out of date:
For example it says that ""This draft is an amendment to IEEE Std 802.3-20XX.""
It is, in fact, an amendment to IEEE Std 802.3-2005.

SuggestedRemedy

Update the abstract to an appropriate current level.

Response *Response Status* **W**

ACCEPT.

related 169 166

Cl **99** *SC* *P* **2** *L* **4** *#* 166

Geoff, Thompson Nortel

Comment Type **ER** *Comment Status* **A** *e*

Entire draft is out of date per the abstract:
It says that this draft is based on to P802.3REVam/D2.2
At 06:27 AM 6/9/2005 , Grow, Bob wrote:
Colleagues:

P802.3REVam was considered by RevCom and the Standards Board at its June meeting. RevCom recommended approval by the Standards Board on 8 June and P802.3REVam/D2.2 was approved on 9 June for publication without opposition. Upon publication, the new revision of the standard will become the base for all current amendment projects.

SuggestedRemedy

Update the draft to reflect changes to IEEE Std 802.3-2005 as published in December.

Response *Response Status* **W**

ACCEPT.

Related 165 169

Cl **30** *SC* *P* *L* *#* 167

Geoff, Thompson Nortel

Comment Type **ER** *Comment Status* **A** *e*

Changes are shown only as the textual changes but not shown in the context of the formatting of clause 30. This presentation does not provide sufficient contextual information for the publications editor to fold the new text into the existing clause 30

SuggestedRemedy

Provide the change information within full editorial context.

Response *Response Status* **W**

ACCEPT.

Cl **45** *SC* **45.2.1.1.3** *P* **22** *L* **51** *#* 168

Grow, Robert Intel

Comment Type **ER** *Comment Status* **A**

The text should be added to the end of the paragraph, not inserted as a new paragraph.

SuggestedRemedy

Modify editing instruction to be a change and include the full paragraph with new text marked with underscore.

Change last paragraph as follows:

[You don't need to identify 802.3-2005, only when the base text is the result of an amendment to 802.3-2005 like IEEE Std 802.3an-2006 (for now P802.3an/D3.0).]

Response *Response Status* **W**

ACCEPT.

Cl **99** *SC* *P* **2** *L* **2** *#* 169

Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

Update the abstract. IEEE Std 802.3-2005 is now published.

SuggestedRemedy

Replace 20xx with 2005. Delete second and third sentences. Fourth sentence: ""This document also ..."" becomes ""This document ..""

Response *Response Status* **C**

ACCEPT.

Related 165 166

Cl **28A** *SC* **Table 28A-1** *P* **55** *L* **28** *#* 170

Grow, Robert Intel

Comment Type **E** *Comment Status* **A**

Correct base text.

SuggestedRemedy

Footnote mark should be a letter, not number

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The Editor was not sucsessful in making the change and need to consult a specialist.

Cl **99** *SC* *P* **3** *L* **16** # 171
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

Make editorial changes to Introduction based on publication of IEEE Std 802.3-2005.

SuggestedRemedy

Line 16, Media Access Control -> media access control
Line 37, Section one -> Section One, also correct other Section numbers.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* **6** *L* **20** # 172
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

The ballot will be by individual.

SuggestedRemedy

Change ""[individual/entity]"" to ""individual""

Response *Response Status* **C**

ACCEPT.

Cl **01** *SC* **1.5** *P* **15** *L* **50** # 173
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

The addition is not required.

SuggestedRemedy

Delete FEC from the list, it is included in 1.5 of IEEE Std 802.3-2005.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* *L* # 174
Grow, Robert Intel

Comment Type **E** *Comment Status* **A**

Though out of scope, the capitalization is inconsistent with the 802.3-2005.

SuggestedRemedy

Only capatilize defined terms. Do not capitalize in the expansion: backplane, Differential Manchester encoded. local device, link partner, next page and extended next page. FYI, the following are inconsistent in 802.3-2005 (fraction that are lower case): local device (64/106), link partner (237/385), next page (101/342)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Searched the document and the editor made changes where appropriate.

Cl **30** *SC* **30** *P* **16** *L* **4** # 175
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

The Editor's note appears to be misanchored.

SuggestedRemedy

Properly anchor the note so it appears at line 19.

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.5.1.1.2** *P* **16** *L* **21** # 176
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

Incorrect marking

SuggestedRemedy

Inserts are not marked with underscore (only new text within a Change instruction). Make line 24 and line 27 consistent with line 21.

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.6.1.1.10** *P* **17** *L* **42** # 177
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

Correct order of subclauses.

SuggestedRemedy

Move 30.6.1.1.10 instruction and changes to its proper sequence.

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.6.1.1.8** *P* **19** *L* **1** # 178
Grow, Robert Intel

Comment Type **E** *Comment Status* **A** *e*

This isn't a change editing instruction.

SuggestedRemedy

As presented it is an insert, and if changed to insert, the inserted text should not be underscored.

Response *Response Status* **C**

ACCEPT.

Cl **00** *SC* *P* *L* # 179
Grow, Robert Intel

Comment Type **E** *Comment Status* **R**

It appears in the changes to base text that two means of indicating new changed text are used (because of different line thickness. For example see the plain version page 17 line 13.

SuggestedRemedy

If appearance is right pick either use an underscore font or underline of the text but not a mix of both.

Response *Response Status* **C**

REJECT.

This is a PDF artifect. If text is enlarged it is the same.

Cl **45** *SC* **45.2.1** *P* **21** *L* **20** # 180
Grow, Robert Intel

Comment Type **E** *Comment Status* **A**

Confusing editing instruction. I'm not sure if this is a change to 802.3an or a change included in 802.3an without significant research. Though not really the intent of replace, that is probably the best editing instruction to use for clarity.

SuggestedRemedy

Assuming that the base text is 802.3an, change to read:

Replace the ""1.147 through 1.32 767"" row of Table 45-3 with following rows (P802.3an/D3.0):

The change marking on the first row would also be removed, if a replace editing instruction is used.

Response *Response Status* **C**

ACCEPT.

yes this is a change to the base text of 802.3an.

Cl **99** *SC* *P* **1** *L* **11** # 181
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

This isn't a revision

SuggestedRemedy

Change ""Draft Revision of:"" to ""Draft Amendment of:"".

Response *Response Status* **W**

ACCEPT.

Cl **99** *SC* *P* **1** *L* **35** # 182
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

It is now 2006.

SuggestedRemedy

Change copyright year to 2006. Also change in all page footers.

Response *Response Status* **W**

ACCEPT.

Cl **99** SC P **1** L **45** # 183
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

This isn't the current mandated copyright statement, there have been minor textual changes.

SuggestedRemedy

Update per Style Manual (4.2.2 in the 2005 manual which was the current one on the web as of 1/31).

Response *Response Status* **W**

ACCEPT.

Cl **00** SC P L # 184
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

Make sure all base text is consistent with IEEE Std 802.3-2005.

SuggestedRemedy

I'll submit comments against any differences I find, but please do an independent comparison.

Response *Response Status* **W**

ACCEPT.

Text has been checked

Cl **00** SC P L # 185
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A**

Some of my D2.0 comments are marked as accept but were not implemented in the draft

SuggestedRemedy

Implement all comments that were accepted in previous ballots. I'll attempt to submit separate comments for those of mine that were not implemented.

Response *Response Status* **W**

ACCEPT.

Checked

Cl **99** SC P **13** L **8** # 186
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

My D2.0 comment #196 was not implemented. This note both incorrect format and is now obsolete.

SuggestedRemedy

Document should be based on IEEE Std 802.3-2005, there is no justification for not having updated any base text changed from P802.3REVam/D2.2 to that published in 802.3-2005.

This is should not be an Editors Note, it should be a ""NOTE --"" per 2005 Style Manual 21.1.

Update the text to the correct text (""four instructions"").

Response *Response Status* **W**

ACCEPT.

Cl **30** SC **30.5.1.1.2** P **16** L **31** # 187
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

The Change instruction could be misinterpreted.

SuggestedRemedy

Change last two sentences of first paragraph of aMAUType, BEHAVIOUR DEFINED AS as follows:

Response *Response Status* **W**

ACCEPT.

Cl **30** SC **30.5.1.1.13** P **16** L **38** # 188
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

The Change instruction could be misinterpreted. Make marking consistent with base text.

SuggestedRemedy

Change first paragraph of aFECAbility, BEHAVIOUR DEFINED AS follows:

802.3-2005 has a gramatical error corrected in the text but not shown as strike through (""the if the"" was corrected to ""if the"", so the first ""the"" needs to be included as strikethrough.)

""for 1000BASE-PX PHY"" also needs to be underlined.

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.5.1.1.14** *P* **16** *L* **44** # 189
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

This would be best as a single change to the subclause

SuggestedRemedy

Change 30.5.1.1.16 as follows:

Add ""ATTRIBUTE"" and ""APPROPRIATE SYNTAX""lines

The previous ""and"" in the SYNTAX paragraph should be replaced with a comma (strikethrough the ""and"" and underscore a new "","").

Replace the second change instruction with the text ""BEHAVIOUR DEFINED AS:""

In third paragraph, ""or PMA/PMD"" should be underscored, as should all of the addition at the end (""for 1000BASE-PX or Enable FEC bit in 10GBASE-KR PMD control register (see 45.2.1.76.4)"").

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.6.1.1.4** *P* **18** *L* **16** # 190
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

Correct change marking.

SuggestedRemedy

The text "" or 73.7.4.1"" should be underscore.

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.5.1.1.15** *P* **17** *L* **5** # 191
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

Cut and paste error?

SuggestedRemedy

Delete lines 5 through 17.

Response *Response Status* **W**

ACCEPT.

Check with Ilango

Cl **30** *SC* *P* **17** *L* **42** # 192
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

Rewrite this and other editing instructions for consistency with previous comments.

SuggestedRemedy

Assure editing instruction restricts the Change to the actual text displayed. If only one paragraph is included in changes and there are more than one paragraph, the paragraph must be identified. If a complete paragraph is not included, then the instruction must identify the sentences. Inserts must clearly identify where the insert is to occur.

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.6.1.1.6** *P* **18** *L* **34** # 193
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

The Change instruction could be misinterpreted. Make marking consistent with base text.

SuggestedRemedy

Change first paragraph of aAutoNegAdvertisedTechnologyAbility, BEHAVIOUR DEFINED AS as follows:

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.6.1.1.9** *P* **19** *L* **17** # 194
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A** *e*

TThe Change instruction could be misinterpreted. The change is only to the first paragraph of the BEHAVIOUR. Make marking consistent with base text.

SuggestedRemedy

Correct editing instruction similar to previous comments. Mark the second sentence with underscore, the last sentence is not new and should not be underscore.

Response *Response Status* **W**

ACCEPT.

Cl **45** *SC* **Table 45-4** *P* **22** *L* **33** # 195
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A**

Confusing editing instruction, changes not properly marked. I also can't find any changes in P802.3an to this table.

SuggestedRemedy

Change ""1.0.5:2"" row of Table 45-4 as follows:

The ""x x 1 x = Reserved"" text should be included as strikethrough.

Response *Response Status* **W**

ACCEPT.

Cl **45** *SC* *P* **23** *L* **1** # 196
Grow, Robert Intel

Comment Type **ER** *Comment Status* **A**

End of time and energy to continue detailed comments on this.

SuggestedRemedy

Verify base text is correctly marked. Make sure editing instructions can be understood by readers and the publication editor. Identify the source when the base text is the result of an amendment to IEEE Std 802.3-2005.

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.6.1.1.5** *P* **18** *L* **18** # 197
Grow, Robert Intel

Comment Type **TR** *Comment Status* **A** *e*

If I can't figure out the editing instruction, then I doubt the publication editor will either.

SuggestedRemedy

If this is to be a change, include all the text. If it is to be a series of inserts, then clearly indicate where each item is to be inserted with individual instructions, unless all items are to be inserted adjacent in sequence, but the insertion point needs to be clear for each item.

Response *Response Status* **W**

ACCEPT.

This is an artifact of the pdf and the copare document. In the clean version this looks much clearer.

The editing instructions will be clarified.

Cl **73** *SC* **73.10.1** *P* **154** *L* **22** # 198
Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Incorrect reference to ""Register 4"" in definition of desire_np variable.

SuggestedRemedy

Fix the reference to point to correct register in MMD7 (Auto-Neg advertisement registers are {7.16, 7.17, 7.18} or refer to 45.2.7.6

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. However desire_np variable may be removed.

Cl **45** *SC* **45.2.7.6** *P* **41** *L* **33** # 199
Ganga, Ilango Intel

Comment Type **ER** *Comment Status* **A**

The cross reference in table 45-120 that refers to subclauses in 73 Auto-Neg are incorrect. For example Next Page is defined in 73.6.9 whereas the table row 1 refers this incorrectly as 73.6.8.

Similary fix all cross references in Table 45-121 in page 43.

SuggestedRemedy

Fix all cross references in Table 45-120 and 45-121

Response *Response Status* **W**

ACCEPT.

Cl **73** *SC* **73.10.4** *P* **164** *L* **34** # 200

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **R**

The state machine transitions instantaneously from AN_GOOD_CHECK to AN_GOOD state reporting the link is ok. Typically the transmission of the packet will start immediately whereas the Link partner will not be ready to receive this packet.

This may not be an issue for KX4 because the LP will still be in Remote Fault mode so the LD will not transmit packets. However this will not be the case in KX mode where the transmitter will start transmission immediately before alignment in LP receiver.

SuggestedRemedy

Possible remedy is to have a delay in AN_GOOD_CHECK to AN_GOOD state

Response *Response Status* **C**

REJECT.
The proposed solution doesn't work because the link that comes up more slowly will still be delayed going to AN_good by the timer and there will be a window when a packet can be dropped. Therefore, it's better to leave to software to delay sending its packets or to retransmit on a new link as needed.

Cl **73** *SC* **73.6.9** *P* **144** *L* **47** # 201

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Still the text and the state machine (Fig 73-10, page 164) implies that both sides should be capable of NP for next exchange to occur.

For Next page exchange, still there is inconsistency in the text 73.6.9 and 73.7.7.1.1 (implies that NP is optional to receive and transmit, whereas it is mandatory to implement NP and optional to transmit)

Howerver the intent was to have an ""or"" condition not an ""and"" condition.

SuggestedRemedy

Fix the text and the state machines to be consistent.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
For 73.6.9 Correct the text to reflect that the NP support is mandatory. The text will reflect OR logic on NP bits.

For 73.7.7.1.1 Correct text to reflect that the NP bit in base page is based on the desire to exchange next pages rather than the ability. The text will reflect OR logic on NP bits.

Cl **73** *SC* **73.10.4** *P* **164** *L* **15** # 202

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Refer to Arbitration state diagram Figure 73-10, consistency

The intent of the consistency_match variable is to make sure the same LCW received in ABILITY_DETECT state is recieved in ACK_DET state as well. (i.e the same LCW that caused ability_match = true).

However as per the State machine and variable definition, it is possible that the LCW received in ABILITY_DETECT is different from the LCW received in the ACK state. (This condition will not happen during normal operatio, however may occur say during error in received DME pages)

SuggestedRemedy

One possible fix is that the consistency match definition can state (similar to clause 37) that the acknowledge_match word is the same as the ability_match_word that caused the transition to ACKNOWLEDGE_DETECT state.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The definition of ability_match_word will be changed to lock the link code word that caused the transition to acknowledge_detect state. The definition of consistency match will be changed to match the acknowledge_match_word to the ability_match_word.

Fix the echo nonce.

Cl **30B** *SC* **30B.2** *P* **55** *L* **40** # 203

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A** *e*

Enumerations to ""AutoNegSelector::= ENUMERATED"" (refer to page 715/6 of 802.3-2005) does not comprehend selector field for Clause 73.

Also enumerations for ""AutoNegTechnology::= ENUMERATED"" (refer to page 716 of 802.3-2005) does not comprehend Technology Ability fields for Clause 73.

SuggestedRemedy

Provide enumerations for Clause 73 selector field and Technology Ability fields

Response *Response Status* **C**

ACCEPT.

Cl **28A** *SC* **28A** *P* **45** *L* **26** # 204
Kim, Yong Broadcom

Comment Type **TR** *Comment Status* **R**

Re: My comment on Draft 2.1 requested to delte selector field or provide justification. Now that I am given ""deemed to be valueable"", I am certain that selector field use for backplane is wrong. Selector field objective was to make sure that common RJ45 connecter is used properly and help to avoid equipment damange.

SuggestedRemedy

Unless there is an objective or use cases for RJ45, please delete this selector field.

Response *Response Status* **W**

REJECT.

Because the same registers are used to pass link code words for both clause 28 and 73, and devices may contain a mix of Clause 28 and 73 ports, it is useful to management agents to have the selector fields so they know what the format of the link code words they will be seeing is.

Response accepted by the Task Force without objection.

Cl **69** *SC* **69.1.2** *P* **47** *L* **27** # 205
Kim, Yong Broadcom

Comment Type **TR** *Comment Status* **R**

Revised wording of c) Not preclude compliance to CISPR/FCC Class A for RF emission and noise immunity is a fine objective. I still assert it does not belong. The TF may use this objective to evaluation different proposals, but it is appropriate to use "meet regional applicable regulatory requirements", such as used in "8.7.3.2 Emission levels The physical MAU and trunk cable system shall comply with applicable local and national codes such as♂FCC Docket 20780-1980 [B23] in the USA. Equipment shall comply with local and national requirements for limitation of electromagnetic interference. Where no local or national requirements exist, equipment shall comply with CISPR 22: 1993." to 10G "52.11.1 Electromagnetic emission A system integrating a 10GBASE-R or 10GBASE-W PMD shall comply with applicable local and national♂codes for the limitation of electromagnetic interference." BTW, 72.9.3~4 seems to be consistent w/ my comment.

SuggestedRemedy

Delete the line

Response *Response Status* **W**

REJECT.

Cited text is not within the scope of the recirculation and does not represent a technical flaw in the draft.

If the commenter is sufficiently concerned, he should join the sponsor group and resubmit at that time.

Cl **69** *SC* **7.2.2** *P* **110** *L* **53** # 206
Kim, Yong Broadcom

Comment Type **TR** *Comment Status* **R**

It did not occur to me that channel model is not in. Draft is technically incomplete. PHY needs TX, channel, and RX specs, (or electrical/signaling specification at the conformance test point) to ensure interoperability. Also, without channel model, I don't see how anyone could comply to any performance materics including BER.

SuggestedRemedy

Please provide a channel model or electrical/signaling spec that properly bounds the backplane signals at the receiver (could be done via TX + channel model).

Response *Response Status* **W**

REJECT.

Some of the issues raised by the commenter were addressed in the response to Comment #57 against D2.1. Also, note that the channel model in Annex 69.B has been augmented per the D2.2 comment resolution process.

The response to Comment #57 against D2.1 is included below -

It should be noted that the Task Force voted in favor of specifying normative transmitter/receiver and informative channel Y: 28, N: 1, A: 7 at the May 2005 interim meeting. In addition that Task Force voted Y: 20, N: 1, A: 1 to reject comment #318 (20318)

To the commenter's points:

1. The transmitter and receiver are explicitly defined in Clauses 70, 71, and 72. The required performance of the latter is indicated by the requirements of interference tolerance test procedure, as described in Annex 69A. Thus, there is no ambiguity for the designer regarding the performance targets for compliant devices.

2. The informative recommendations for channel performance in Annex 69B supply guidance for users of the standard regarding what backplane channels are interoperable with compliant devices. This implies a linkage between these recommendations and the performance targets enforced via the interference tolerance test.

3. The danger of specifying the connector as "out of the box" is the implication that the mechanical design and electrical performance of the connector must also be specified (as well as the pin-out of the connector, which will impact crosstalk performance). This will limit the broad market potential of the standard since it would constrain the solution to a single implementation. Abstracting the channel to include the connectors avoids this issue and gives Backplane Ethernet a larger addressable market

4. The specification for open-backplane systems will originate from other organizations such as PICMG. Just as enterprises build generic cable plants to ISO or TIA specifications (not necessarily IEEE specifications), organizations that define open backplane

specifications will define the connectors, pin-outs, and performance requirements for systems bearing those respective labels. It is expected that such organizations will base such requirements on the IEEE P802.3ap informative recommendations to ensure compatibility with compliant Backplane Ethernet devices.

5. The editor would humbly submit that the stated premise that XAUI interconnects are limited to the closed circuit card environment ignores that fact that XAUI channel is defined to include two connectors. Clearly board-board connections were envisioned. In addition, the fact that XAUI does not specify the connector itself has made it adaptable to multiple environments (a variety of pluggable optical module form factors and modular platform backplanes).

Motion #2 (from January 2006 Interim)
Technical (>=75%)
Move to reject comment #57 with response above.
Moved by John D'Ambrosia
Seconded Charles Moore

All
Yes - 22
No - 0
Abstain - 0

Motion Passes