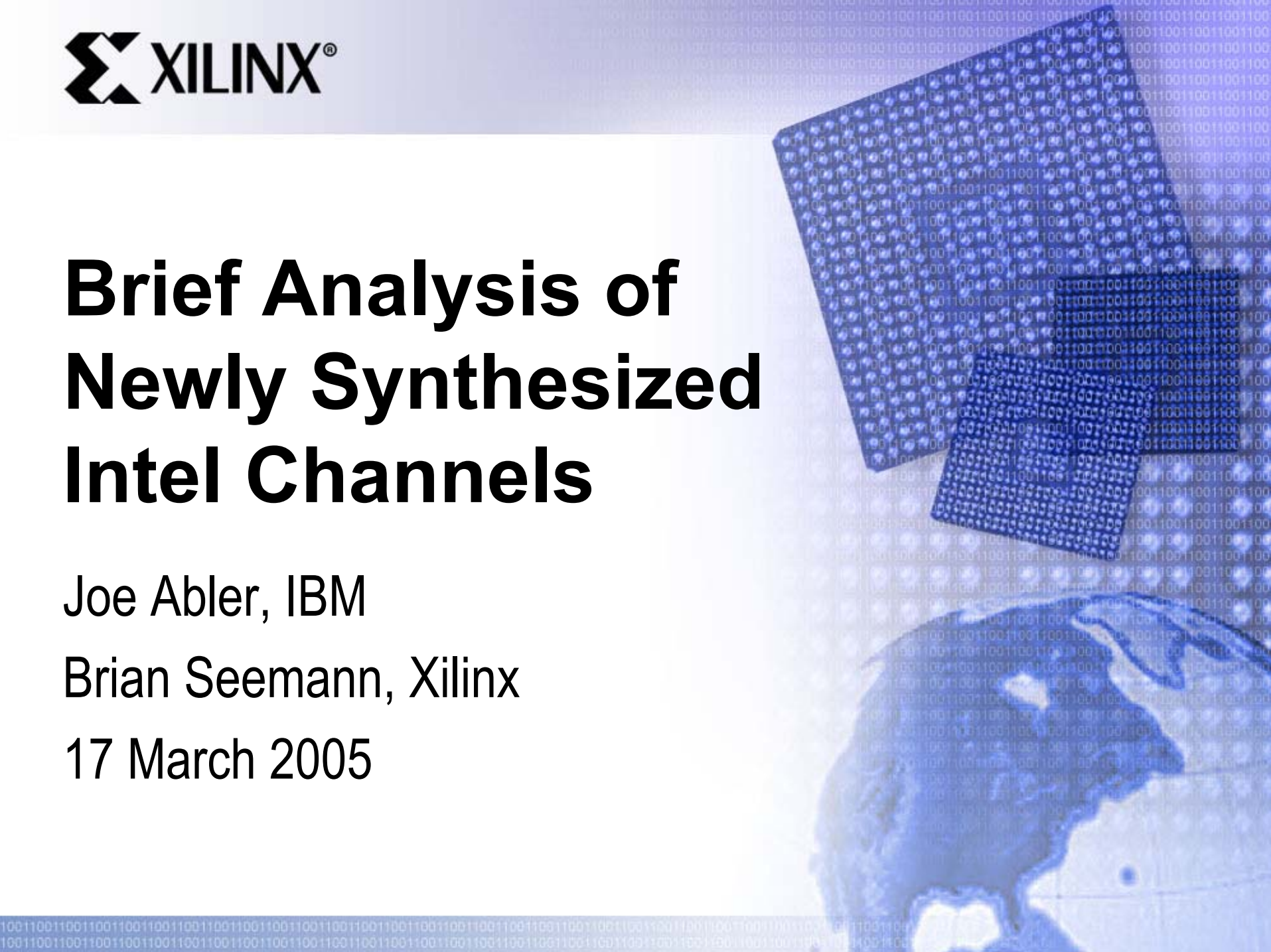

Brief Analysis of Newly Synthesized Intel Channels

Joe Abler, IBM

Brian Seemann, Xilinx

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Objectives

- Communicate progress on solving Intel synthesized channels
- Provide perspective on remaining impediments and opportunities for complete success

Re-Sim of Synthesized

	BER=10^{-12} FFE3 / DFE5			
Channel	**Parameter**	**Units**	**Original**	**Synthesized**
Peters B1	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0.03	0.053
	Timing Margin	$ps_{p\text{-}p}$	9.3	19.6
Peters B12	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0.018	0.051
	Timing Margin	$ps_{p\text{-}p}$	5.8	20.4
Peters B20	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0.003	0.025
	Timing Margin	$ps_{p\text{-}p}$	0.9	10.2
Peters M1	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0.021	0.06
	Timing Margin	$ps_{p\text{-}p}$	7.3	18.9
Peters M20	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0.002	0.021
	Timing Margin	$ps_{p\text{-}p}$	0.2	10.1
Peters T1	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0	0
	Timing Margin	$ps_{p\text{-}p}$	E-05	E-07
Peters T12	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0	0
	Timing Margin	$ps_{p\text{-}p}$	E-05	E-06
Peters T20	Voltage Margin	$V_{p\text{-}p(diff'l)}$	0	0
	Timing Margin	$ps_{p\text{-}p}$	E-04	E-05

Top Channel Study

–Elimination of Crosstalks

- This is not proposed as realistic
- Useful as a outer boundary test

–Change to FFE4 / DFE10

- This is not proposed as realistic
- Useful as a outer boundary test

	Top - original			Top - synthesized		
timing margin (ps_{p-p} @ BER 10^{-12})	t1	t12	t20	t1	t12	t20
Signal ad-hoc setup	E-05	E-05	E-04	E-07	E-06	E-05
no NEXT	E-05	E-09	0.1	E-011	6	10.9
no FEXT	E-05	E-05	E-04	E-011	E-07	E-05
no Xtlk	E-07	E-08	3.2	4.1	9.7	13.9
no Xtlk or DCD	E-06	E-09	5.6	9.5	16.7	18.1

	Top - original			Top - synthesized		
voltage margin ($mV_{p-p\ diff}$ @ BER 10^{-12})	t1	t12	t20	t1	t12	t20
Signal ad-hoc setup	0	0	0	0	0	0
no NEXT	0	0	2	0	19	32
no FEXT	0	0	0	0	0	0
no Xtlk	0	0	10	14	30	43
no Xtlk or DCD	0	0	17	30	53	64

	Top - original			Top - synthesized		
timing margin (ps_{p-p} @ BER 10^{-12})	t1	t12	t20	t1	t12	t20
ffe4/dfe10 ad-hoc setup	E-08	E-06	E-05	1.7	E-07	E-06
no NEXT	E-11	0.7	0	13.4	13.4	15.5
no FEXT	E-07	E-05	E-05	9.3	E-10	E-07
no Xtlk	E-011	0.1	5.7	13.3	13.6	12.3
no Xtlk or DCD	4.7	0.1	11.3	15.8	15.5	17.6

	Top - original			Top - synthesized		
voltage margin ($mV_{p-p\ diff}$ @ BER 10^{-12})	t1	t12	t20	t1	t12	t20
ffe4/dfe10 ad-hoc setup	0	0	0	4	0	0
no NEXT	0	4	1	39	40	48
no FEXT	0	0	0	27	0	0
no Xtlk	0	1	13	47	43	43
no Xtlk or DCD	13	2	34	52	47	60

FFE3 / DFE5

timing margin (ps_{p-p} @ BER 10^{-12})	Top - synthesized t1	t12	t20
Signal ad-hoc setup	E-07	E-06	E-05
no NEXT	E-011	6	10.9
no FEXT	E-011	E-07	E-05
no Xtlk	4.1	9.7	13.9
no Xtlk or DCD	9.5	16.7	18.1

voltage margin ($mV_{p-p\ diff}$ @ BER 10^{-12})	Top - synthesized t1	t12	t20
Signal ad-hoc setup	0	0	0
no NEXT	0	19	32
no FEXT	0	0	0
no Xtlk	14	30	43
no Xtlk or DCD	30	53	64

Removing just NEXT is enough for T12 & T20

Removing just NEXT *OR* FEXT is not enough for T1

Removing all Crosstalk makes them all work

FFE4 / DFE10

timing margin (ps_{p-p} @ BER 10^{-12})	Top - synthesized		
	t1	t12	t20
ffe4/dfe10 ad-hoc setup	1.7	E-07	E-06
no NEXT	13.4	13.4	15.5
no FEXT	9.3	E-10	E-07
no Xtlk	13.3	13.6	12.3
no Xtlk or DCD	15.8	15.5	17.6

voltage margin ($mV_{p-p\ diff}$ @ BER 10^{-12})	Top - synthesized		
	t1	t12	t20
ffe4/dfe10 ad-hoc setup	4	0	0
no NEXT	39	40	48
no FEXT	27	0	0
no Xtlk	47	43	43
no Xtlk or DCD	52	47	60

Adding taps doesn't solve any of them

Verticals Only

FFE3 / DFE5

voltage margin ($mV_{p-p\ diff}$ @ BER 10^{-12})	Top - synthesized t1	t12	t20
Signal ad-hoc setup	0	0	0
no NEXT	0	19	32
no FEXT	0	0	0
no Xtlk	14	30	43
no Xtlk or DCD	30	53	64

FFE4 / DFE10

voltage margin ($mV_{p-p\ diff}$ @ BER 10^{-12})	Top - synthesized t1	t12	t20
ffe4/dfe10 ad-hoc setup	4	0	0
no NEXT	39	40	48
no FEXT	27	0	0
no Xtlk	47	43	43
no Xtlk or DCD	52	47	60

With no X-talk + more taps, removing NEXT *OR* FEXT has a similar effect

With more taps, removing just FEXT on T1 makes it work

Conclusions

- Adding a (un)reasonable number of taps will not solve the present synthesized Intel Top-layer channels
- Reducing the crosstalk is likely the single largest positive effect the channel can offer
- Solving these channels would likely require incremental improvement in both signaling and channel crosstalk