Cl **00** *SC* *P* **11** *L* **7** # 18

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

Page # for Contents Page is incorrect.

SuggestedRemedy

check link.

Response *Response Status* **C**

REJECT.
The contents pages have the same issues as the cross references.

Use the "clean" version to check the page numbers.

Cl **00** *SC* *P* **4** *L* **24** # 17

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

List of proposed amendments to 802.3-2005 incomplete

SuggestedRemedy

add 802.3at and 802.3au

Response *Response Status* **C**

REJECT.

802.3an has no text either
The commenter does not supply a proposed text

Cl **01** *SC* **1.4** *P* **16** *L* **4** # 101

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A** *e*

Per D2.2#174, you have changed Differential Manchester Encoding to differential Manchester encoding in 72 and 73; need to make the change in 1.4 and similar in 1.5.
Note that phrases in the abbreviations list often have the very first letter in lower case.

SuggestedRemedy

Change to differential Manchester encoding, differential Manchester encoded (or -ing).
Change to 'local device', link partner'

Response *Response Status* **C**

ACCEPT.

Cl **28A** *SC* **28A** *P* **47** *L* **47** # 30

Law, David 3Com

Comment Type **TR** *Comment Status* **A** *Check wit Pat*

I don't understand, although I'm probability missing it, why an additional Clause 28 selector is required for Clause 73, it wasn't required for Clause 37. Since I can't see any case where Clause 73 could be communicating to Clause 28 or Clause 37 device there isn't an issue there. Since there are only 32 Selector Filed values we need to do everything to preserve them.

SuggestedRemedy

Until I am convinced otherwise please reuse the existing Clause 28 Selector Field values for Clause 73 or alternatively define your own Clause 73 Selector Field values in a separate Annex that are only used for Clause 73.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Straw Poll #1 -
a) Status quo
b) Use Clause 28 selector field value

a) 0
b) 6

Remove the change to annex 28a and anywhere where selector field value is referenced change to use the existing IEEE802.3 value, including in Clause 73.

Cl **30** *SC* **30.5.1.1** *P* **17** *L* **48** # 122

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A** *e*

Do we need management variables to report FEC status e.g. on or off, as well as aFECAbility?

SuggestedRemedy

Change this into '10GBASE-R FEC capability register', add status bit(s).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add following subclause:

45.2.7.100.1 FEC Enabled (7.48.x)

When AN process has been completed as indicated by the AN complete bit, the FEC Enabled bit indicates that FEC function has been enabled in the 10GBASE-KR PHY as a result of the priority resolution function.

Add FEC enabled bit to the register 7.48 (register bit x) Backplane Ethernet Status Register

Modify the text to 30.5.1.1.14 aFECmode as follows:

A read-write value that indicates the mode of operation of the 1000BASE-PX PHY or 10GBASE-R PHY optional FEC Sublayer for Forward error correction (see 65.2 for 1000BASE-PX PHY or see clause 74 for 10GBASE-R PHY).

When Clause 73 Auto-Negotiation is enabled a GET operation maps to the variable FEC enabled in Clause 45 register 7.48

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value.

Request that Task Force gives editor editorial license to modify verbiage as appropriate when implementing above response. The editor can choose appropriate bit in Register 7.48.

Cl **30** *SC* **30.5.1.1.14** *P* **18** *L* **11** # 103

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A** *Check Cl 74*

Per 1.5, forward error correction doesn't necessarily have capitals (entry now in base document). But the name of the sublayer gets capitals.

SuggestedRemedy

Make changes at 30.5.1.1.14, 45.2.1.84.1.1, 74.2, 74.16.3, Keywords

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Changed 30.5.1.1.14, 45.2.1.84.1.1, 74.2, 74.16.3, Keywords

There might be some more corrections required in the base text.

Cl **30** *SC* **30.5.1.1.15** *P* **18** *L* **33** # 55

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

I suspect the increment rates at 10 Mb/s, 1000 Mb/s have been reversed. Bug in base document?

SuggestedRemedy

Consider doing a service to humanity and swapping them back, here and next subclause. Editorial: space between 10 and Mb/s.

Response *Response Status* **C**

REJECT.

The comment is out of scope for this project. Commenter is encouraged to take this up as a maintenance item.

Cl **30** *SC* **30.5.1.1.15** *P* **18** *L* **40** # 100

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **R**

Why does this counter have a maximum increment rate (wrong?) for 10 Mb/s implementations, when text says 'This counter will not increment for other PHY types.'? Does 10PASS-TS use both aFECCorrectedBlocks and aPMEFECCorrectedBlocks?

SuggestedRemedy

If we can find the answers, consider cleaning up the base text. Consider referring to maintenance.

Response *Response Status* **C**

REJECT.

Beyond the scope of this project. Refer to maintenance.

Cl **45** *SC* *P* *L* # 19

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

Links in document are broken, so it is not possible to verify links are to correct positions.

SuggestedRemedy

Correct broken link problem and then verify all links are correct.

Response *Response Status* **C**

REJECT.

The links in the compare document do not always work.

The links in the "clean" version should be used to check the cross references.

Cl **45** *SC* **45** *P* **47** *L* **4** # 74

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

To be in sync with 802.3an-D3.1, Change Title of table 45-123 to read as follows:

""Table 45-123-AN LP XNP ability register bit definitions""

SuggestedRemedy

As per comment

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.10.3** *P* **27** *L* **41** # 46

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

The descriptions of ability bits are not consistent in 45. In the text, we have 'PMA/PMD is able to operate as 10GBASE-LRM' but 'PMA/PMD is able to support a 10GBASE-KX4 PMA/PMD type'. ''Support' is not precise (that's why we sometimes use it in objectives!). Nor accurate: 'The floor supports the table, the computer supports Linux, the modem supports PPP, PCS is able to support PRBS31 pattern testing...' This should be harmonized across .3an, .3aq (I have made a comment), and in the next revision.

SuggestedRemedy

Change to 'operate as 10GBASE-KX4' and as 10GBASE-KR in next subclause.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.7.4** *P* **26** *L* **7** # 4

Dallesasse, John Emcore Corporation

Comment Type **E** *Comment Status* **A**

During the IEEE 802.3ae meetings, after a (very) lengthy debate on whether to refer to the type of WDM used in 10GBASE-LX4 as ""WWDM"" or ""CWDM"", it was the concensus of the group to refer to it as ""LX4-WDM"". After this debate, it was discovered that all references to ""WWDM"" or ""CWDM"" had been previously removed from the document, so the concensus was not captured.

SuggestedRemedy

Change all instances of ""WWDW"" to ""LX4-WDM"" (multiple instances).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

change "WWDM" to "LX4-WDM" in 45.2.1.7.4 and 45.2.1.7.5

change "wide wavelength division multiplexing (WWDM)" to "LX4-WDM" in 45.2.1.8

Cl **45** *SC* **45.2.1.83** *P* **37** *L* **11** # 50

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

Transmit and receive mixed up

SuggestedRemedy

In Table 45-63 Description, for bits 1.161.13 and 1.161.12, change transmit fault to receive fault and vice versa.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.84.1** *P* **39** *L* **23** # 121

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

We may need an MDIO register that lets station managment (if it exists) know if FEC is in use or not.

SuggestedRemedy

Change this into '10GBASE-R FEC capability register', add status bit(s).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement a 10GBASE-KR FEC negotiated bit 7.48.4 in the Backplane Ethernet status register with appropriate text. This bit is only set if FEC and 10GASE-KR has been negotiated.

In 73.6.5 for FEC indicate it only gets turned on 10GBASE-KR has been selected.

Cl **45** *SC* **45.2.1.84.1** *P* **39** *L* **23** # 106

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

The language of the subclause and table titles should follow the bit name

SuggestedRemedy

Change 'capability' to 'ability', twice and in Table 45-64, twice more in 45.2.1.84.1, maybe in Table 45-120 p44 line 27 and Table 45-121.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

change 'capability' to 'ability' in registers 1.170, 7.18 and 7.21

Cl **45** *SC* **45.2.1.84.1** *P* **39** *L* **38** # 91

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Delete ""SC-Self Clearing"" from foot note under the tables 45-65 and 45-66 because it is not used in these tables.

Delete R/W from foot note under 45-65 because it is not used in this table

SuggestedRemedy

As per comment.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.84.1.1** *P* **39** *L* **43** # 89

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Rephrase the line to indicate 10GBASE-R PHY, ""When read as a one, this bit indicates if the PHY supports 10GBASE-R Forward Error Correction (FEC)""

SuggestedRemedy

Rephrase the line as follows:
""When read as a one, this bit indicates if the 10GBASE-R PHY supports Forward Error Correction (FEC)""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

change to:
"When read as a one, this bit indicates that the 10GBASE-R PHY supports forward error correction (FEC)"

Cl **45** *SC* **45.2.1.84.2** *P* **40** *L* **11** # 120

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

Do we still need unidirecttional FEC Clause 45 registers for debug purposes?

SuggestedRemedy

Add Clause 45 bits for transmit and receive side FEC. See D2.2 comment 116.

Response *Response Status* **C**

REJECT.

This change was requested previously and was recirculated. There has been no pile-on to this comment to support it. The Task Force feels that the usefulness of the feature would not justify the additional complexity.

The response to D2.2 comment 116 rejects having separate bits for transmit and receive.

Cl **45** *SC* **45.2.1.84.2** *P* **40** *L* **14** # 90

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

In the description of ""FEC Enable Error Indication"" bit change ""upper layer"" to ""PCS layer""

SuggestedRemedy

Rephrase the description of ""FEC Enable Error Indication"" bit as follows:

A write of 1 to this bit configures FEC decoder to
indicate Error to the PCS layer

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
change to:
'A write of 1 to this bit configures the FEC decoder to indicate errors to the PCS layer'

Cl **45** *SC* **45.2.1.84.2.1** *P* **40** *L* **22** # 105

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

After the rearrangement of the resister names, there are many leftover capitals to be cleaned up (bit names in Clause 45 don't use capitals much)

SuggestedRemedy

FEC enable (also in 74.9), Pause ability (D2.2 # 100 refers), LP acknowledge and so on.
Also FEC error indication

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7** *P* **42** *L* # 77

Ganga, Ilango Intel

Comment Type **ER** *Comment Status* **A**

Sync up All registers in MMD7 with the latest 802.3an-D3.1. Also modify change instructions accordingly throughout the AN register definitions.

SuggestedRemedy

As per comment

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.
Review against 802.3an draft 3.2 rather than 3.1

Change instructions to make it clear at the start of Clause 45 that all Clause 45 changes are against 802.3an unless otherwise stated.

Implement suggested remedy and delete 45.2.1.1, 45.2.1.1.3, 45.2.1.4, 45.2.1.4.1, PMA / PMD Extended Ability Register 1.11, 45.2.1.10.3, and 45.2.1.10.4.

This functionality is already defined in 802.3an Draft 3.1.

In light of comment response to 802.3an D3.1:

Motion #1 - Move to reconsider response to comment #77
Procedural (>=50%)
Moved by Arthur Marris
Second by Schelto van Doorn

Motion passes by voice vote without objection

New Response -

Implement suggested remedy and delete 45.2.1.1, 45.2.1.1.3, 45.2.1.4, and 45.2.1.4.1.

Add to PMA / PMD Control 2 Register (1.7) 1000BASE-KX PMA / PMD Type.

Add to PMA / PMD Extended Ability Register (1.11) 1000BASE-KX Ability bit.

Cl **45** *SC* **45.2.7.1** *P* **42** *L* **22** # 3

Marris, Arthur Cadence

Comment Type **T** *Comment Status* **A**

The text ""A device that supports multiple port types may implement both Clause 22 control register operation and Clause 45 control register operation. Some control functions have been duplicated in both definitions. The register bits to control these functions are simply echoed in both locations, any reads or writes to these bits behave identically whether made through the Clause 22 location or the Clause 45 location.""

belongs in 802.3an not 802.3ap.

A comment has been submitted against 802.3an 3.1 to request the insertion of this text in 802.3an.

SuggestedRemedy

Delete this text from 802.3ap.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.2** *P* **42** *L* **47** # 76

Ganga, Ilango Intel

Comment Type **ER** *Comment Status* **A**

In table 45-119, as per 802.3an-D3.1 bit 7.1.2 is link status and is not reserved. Hence sync up the changes with respect to 802.3an-D3.1

SuggestedRemedy

Delete 7.1.2 reserved from table 45-119.

Response *Response Status* **W**

ACCEPT.

Cl **45** *SC* **45.2.7.2** *P* **43** *L* **21** # 80

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Definition for 45.2.7.2.2 Page reveived bit: As per 802.3an-3.1 the definition of page received bit is defined as follows:

The Page Received bit (7.1.6) shall be set to one to indicate that a new Link Code Word has been received and stored in the AN LP XNP ability registers 7.25-7.27. The contents of register 7.16 will be valid when bit 7.1.6 is set the first time during the Auto-Negotiation.

The above definition does not comprehend the Clause 73 Auto-Neg base page received. Hence rephrase the above definition to include Clause 74 base page received. In clause 73 there is a possibility that only base pages are exchanged and not next page exchange takes place.

SuggestedRemedy

Modify the definition of 45.2.7.2.2 Page received bit to include Clause 73 base page received.

The Page Received bit (7.1.6) shall be set to one to indicate that a new Link Code Word has been received and stored in the AN LP base page ability registers 7.19-7.21 or AN LP XNP ability registers 7.25-7.27. The contents of AN advertisement register(s) 7.16-7.18 will be valid when bit 7.1.6 is set the first time during the Auto-Negotiation.

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.6** *P* **44** *L* **10** # 71

McClellan, Brett Solarflare

Comment Type **E** *Comment Status* **A**

typo "28.2.12" should be "28.2.1.2"

SuggestedRemedy

change as indicated

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.6** *P* **44** *L* **10** # 92

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Fix typo on description to bit 7.16.15 as follows:

7.16.15: See 28.2.1.2 and 73.6.9

Also add reference to clause 28 on description to bit 7.16.14 as follows:

7.16.14: See 28.2.1.2 and 73.6.8

Underline the changes to 7.16.9:5 in second column ""Echoed Nonce Field"" and in the third column, do not underline Technology ability field.

SuggestedRemedy

As per comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

7.16.15: See 28.2.1.2 and 73.6.9

Make the description of 7.16.14 exactly the same as in 802.3an.That is 'value always 0, writes ignored'.

Cl **45** *SC* **45.2.7.6** *P* **44** *L* **50** # 93

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Delete reference to register 1.7 from the following sentence because the Ability is indicated only in registers 1.4 and 1.11.

""......is set according to the appropriate Backplane Ethernet port type values set in the PMA/PMD registers 1.4, 1.7 and 1.11"".

SuggestedRemedy

As per comment

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.7** *P* **45** *L* **25** # 1

Marris, Arthur Cadence

Comment Type **E** *Comment Status* **A**

reference to Clause 28 is wrong

SuggestedRemedy

Change 'See 28.2.12' to 'See 28.2.1.2'

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.7** *P* **45** *L* **25** # 94

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Table 45-121 column 3. Change all occurences of ""28.2.12"" to ""28.2.1.2"" (total of 5 occurences.

Register bits 7.19.9:5: Underline ""Echoed Nonce Field"" in column 2

SuggestedRemedy

As per comment

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.7** *P* **45** *L* **25** # 72

McClellan, Brett Solarflare

Comment Type **E** *Comment Status* **A**

typo on lines 25,26,28,32 and 33 "28.2.12" should be "28.2.1.2"

SuggestedRemedy

change as indicated

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.8** *P* **46** *L* **14** # 2

Marris, Arthur Cadence

Comment Type **T** *Comment Status* **A**

Bit 7.22.14 in Table 45-122 AN Next Page register should be reserved.

SuggestedRemedy

Change bit 7.22.14 to be Reserved Value always 0, writes ignored RO

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.7.8** *P* **46** *L* **23** # 95

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **R**

Change description of Unformatted Field bits as follows:

U[15:0] see 28.2.3.4 or U[26:11] see 73.7.7.1

U[31:16] see 28.2.3.4 or U[42:27] see 73.7.7.1

SuggestedRemedy

As per comment.

Also make same changes to Unformatted Field bit descriptions in AN XNP LP ability registers in Table 45-123 in page 47.

Response *Response Status* **C**

REJECT.

With 802.3an D3.2 these bits have been removed from the table so there is no need to call them out separately in the description.

Cl **45** *SC* **45.5.3.2** *P* **50** *L* **21** # 53

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

There is already an option *FEC in Clause 45: it's in 45.5.3.16.

SuggestedRemedy

Rename one of them.

Response *Response Status* **C**

ACCEPT.

Rename *FEC to *FEC-R

Cl **45** *SC* **45.5.3.9** *P* **54** *L* **14** # 78

Ganga, Ilango Intel

Comment Type **ER** *Comment Status* **A**

In Clasue 45 PICS, Incorrect reference to subclauses for AN39, AN40 and AN41. Fix the reference as appropriate. Also add the register bit name to make it clear (similar to AM37).

SuggestedRemedy

As per comment

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

remove AM39 and AM40 because this functionality is now in 802.3an.

Renumber AM37, 38 and 41 to AM55, 56, 57.

Change AM41 to:
AM57 BP AN ability (7.48.0) 45.2.7.100.3 Set to 1 if KX, KX4, or KR PHY is implemented

Cl **69** *SC* **69.2.3** *P* **59** *L* **30** # 75

Ganga, Ilango Intel

Comment Type **E** *Comment Status* **A**

Rephrase line 30 to include ""10GBASE-R Forward Error Correction"" as follows:

SuggestedRemedy

Rephrase line as follows:

The 10GBASE-KR PHY may optionally include 10GBASE-R Forward Error Correction (FEC), as defined in Clause 74.

Also in Table 69-1 last column, change ""FEC"" to ""10GBASE-R FEC""

Response *Response Status* **C**

ACCEPT.

Cl **69** *SC* **69.3** *P* **60** *L* **18** # 49

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

The maximum delay through each layer is specified in Table 69-3, so that users know what to expect. But the FEC sublayer isn't mentioned, and it will need a reasonable delay allocation. Note for Clause 45 purposes, FEC is in PMA/PMD MMD.

SuggestedRemedy

Unless FEC round-trip latency is <<512BT: insert another row for 10GBASE-R FEC, just above 10GBASE-KR PMA/PMD. Choose a comfortable maximum round-trip delay limit. Copy and modify 72.4 Delay constraints (without the last sentence) into Clause 74.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See Comment #33.

Cl **69** *SC* **69.3** *P* **61** *L* **17** # 81

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

In table 69-3, delay constraints for 10GBASE-KR should include delay constraints for 10GBASE-R FEC.

SuggestedRemedy

Add a row to Table 69-3 to include delay constraints for 10GBASE-R FEC and provide a reference to corresponding subclause in Clause 74.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add a row to Table 69-3 to include delay constraints for 10GBASE-R FEC and provide a reference to corresponding subclause in Clause 74.

See Comment #33

Cl **69A** *SC* **69A** *P* **209** *L* **11** # 20

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

The sentence ""a major problem in communicating across crowded backplanes is interference"" can be generalized

SuggestedRemedy

Change to
""Interference is a significant problem to the successful transmission of an electrical signal.""

Response *Response Status* **C**

REJECT.

It is not necessary to generalize this statement, as these requirements specifically address the problem of Ethernet operation over electrical backplanes.

Cl **69A** *SC* **69A.2.1** *P* **210** *L* **28** # 73

Valliappan, Magesh Broadcom

Comment Type **TR** *Comment Status* **A**

rise time to use in the pattern generator. The EIT result depends on this parameter. Faster rise times, will imply larger signal at the receiver, less equalization, and more interference tolerance. To get a useful result, this must be contrained.

SuggestedRemedy

Specify that the pattern generator must have a rise time > 40ps, measured according to Clause 72.7.1.7

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

It appears to be appropriate to also adopt comparable specifications for 1000BASE-KX and 10GBASE-KX4. Specify that the pattern generator rise time is greater than the minimum value specified for the port type under test. Add a minimum rise time specification to tables 70-7, 71-7, and 72-10 with the value set to the maximum recommended/required transmitter rise time for the PHY under test (note that this 320 ps for 1000BASE-KX, 130 ps for 10GBASE-KX4, and 47 ps for 10GBASE-KR).

Cl **69A** *SC* **69A.3** *P* **212** *L* **51** # 63

Noseworthy, Bob UNH-IOL

Comment Type **E** *Comment Status* **A**

Equation reference is incorrect

SuggestedRemedy

Change:
""The frequency dependent EITbaseline is defined in Equations (69A-1) and (69A-2)""
To:
""The frequency dependent EITbaseline is defined in Equations (69A-7) and (69A-8)""

Response *Response Status* **C**

ACCEPT.

Cl **69A** *SC* **69A.3** *P* **212** *L* **6** # 31

Telang, Vivek Broadcom Corp

Comment Type **TR** *Comment Status* **R**

A sinusoid interferer does not accurately capture the intent of this test, which is to evaluate the tolerance of a receiver to a crosstalk interferer, for the following reasons:
1. As pointed out by Fulvio in a recent channel ad-hoc conference call, the pdf (histogram) of a sinuoid is significantly different from that of a crosstalk interferer
2. A receiver could be ""built-to-the-test"" with a 2-tap predictive noise canceller that could effectively cancel any sinusoid in the signal passband. Clearly, this would have no correlation to the receiver's ability to tolerate real crosstalk (False Positive)
3. A well-designed receiver capable of tolerating crosstalk might fail this test for completeley different reasons, e.g. an adaptation loop might mistrain (False Negative)
For all the above reasons, this test should be designed to use a interference signal that is richer than a single sinusoid

SuggestedRemedy

Define the EIT to use either white noise, or shaped (colored) noise to mimic a real crosstalk power sum. The shaping filter could be built fairly easily with either R,C components, or even using cabling or PCB traces. This approach has been used for crosstalk testing of 1000BASE-T PHYs, and is also currently being specified in the 10GBASE-T draft.

Response *Response Status* **U**

REJECT.

Commented has not provided a technically complete remedy, and no specific changes to the draft are provided.

Straw Poll #9
Preference for interference type for Interference Tolerance Testing
A. Swept sinusoid interference
B. Broadband noise Interference

A. 0
B. 20

A broadband noise source may be superior from the standpoint of emulating crosstalk. However, there are several practical concerns that need to be addressed as part of this response:

1. How accurately must the interference source emulate crosstalk?
2. What is the bandwidth of the noise required to emulate crosstalk with the required precision?
3. Is there test equipment available that generates noise occupying this bandwidth? Does this device output sufficient noise power to stress the receiver under test (is amplification an option)?
4. Are there requirements on the shape of the noise PSD? Is there a filter structure that can enforce this shape over the required bandwith?

5. How does one calibrate the noise signal at the receiver input?

The merits and limitation of sinusoidal interference are well understood. The relative merits and limitations of a broadband noise model must also be understood to warrant a change to the specification.

Cl **69A** *SC* **69B.2.1** *P* **210** *L* **41** # 24

D'Ambrosia, John Tyco Electronics

Comment Type **TR** *Comment Status* **A**

This is essentially a pile-on to Comment #45 from Howard Baumer.

""For 10GBASE-KR.....meeting the requirements of 72.7.1.10 shall be included.""

This reference for the tx is in question, as the tx waveform template needs completed to bound the amount of Tx equalization for testing the Rx.

SuggestedRemedy

see contribution from Howard Baumer.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer to comment #45

As the commenter states, the text of 69A.2.1 states that the requirements of 72.7.1.10, must be met by the pattern generator. Any changes to 72.7.1.10 will be inherited by this subclause and no changes to this text are expected.

Cl **69b** *SC* **4.5** *P* **220** *L* **23** # 16

Mellitz, Richard Intel

Comment Type **TR** *Comment Status* **A**

ref: Eq 69b-12 & 69b-13 are not restrive enough when considering thru_worst.s4p which is in the high confidence regions for a IL and RL parameters. This channel does not have suffeciet eye opening a 1e-12 BER. See Dambrosia_01_0306

SuggestedRemedy

Change Eq 69b-12
RL(f)>=RLmax(f)=14-9.65*log10(f/350MHz)
Change frequency range for 69B-12 to
For 50MHz < f < 3000 MHz
and Eq. 69b-13
RL(f)>=RLmax=6
Change frequency range for 69B-13
For 3000 MHz to 10.312.5 MHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer to comment #23

Cl **69B** *SC* **69B.4** *P* **216** *L* **1** # 41

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **A**

The channel model limits do not adequately screen KR channels. These limits allow for false positive channels, channels that pass these limits yet have been shown through simulations not to work.

SuggestedRemedy

Modify the channel model per baumer02_200603

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Reference baumer_03_0306
Reference baumer_04_0306

See also #16, #23 for RLmin

Per the straw polls below, the Task Force could not agree to changes to Amax, Ilmax, ILD, and ICRmin.

Rlmin was changed per Comment #23

Straw Poll #2 - For Amax
a) Per Draft 2.3
b) Per baumer_03_0306

a) 13
b) 4

Straw Poll #3 - For Ilmax
a) Per Draft 2.3
b) Per baumer_03_0306

a) 15
b) 4

Straw Poll #4 - For ICR Min
a) Per Draft 2.3
b) Per baumer_03_0306

a) 14
b) 4

Straw Poll #5 - For ILD
a) Per Draft 2.3
b) Per baumer_03_0306

a) 11
b) 7

Cl **69B** *SC* **69B.4.1** *P* **216** *L* **6** # 22

D'Ambrosia, John Tyco Electronics

Comment Type **T** *Comment Status* **A**

The bounding of the informative characteristics to the EIT testing is not strong enough for the sake of conveying the validity of the informative channel characteristics.

Rewrord-
A series of informative parameters are defined for use in backplane channel evaluation. These parameters address the channel insertion loss and crosstalk. The informative parameters for channel insertion loss are
summarized in Table 69Bû1.

SuggestedRemedy

Change text to

""A series of informative parameters are defined for use in backplane channel evaluation. These parameters address the channel insertion loss and crosstalk.

The informative parameters for channel insertion loss are based on the amount of allowable loss permitted for the given amount of interference as stated by the Interference Tolerance Testing specified in Annex 69A.

The informative parameters for channel insertion loss are summarized in Table 69Bû1.""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Use proposed text as a basis, with editorial license granted to correct any spelling, grammar, and cross-reference issues the proposed text may contain.

Cl **69B** *SC* **69B.4.5** *P* **220** *L* **35** # 23

D'Ambrosia, John Tyco Electronics

Comment Type **TR** *Comment Status* **A**

Return Loss specification is insufficient.

SuggestedRemedy

See Presentation dambrosia_01_0306.
Replace Figure 69B-6 per updated equation.
Update formatting of figure so ""0"" is at top left corner, instead of bottom left corner.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer to comment #16

The range of applicability is from 50 MHz to the signaling speed of the PHY type of interest.

RL(f) >= RImin(f) = 15
For 50 Mhz to 275 MHz

RL(f) >= RImin(f) = 15 - 9.64*log10(f/275MHz)
For 275 MHz to 3000 MHz

RL(f) >= RImin(f) = 5
For 3000 MHz to 10312.5 MHz

Cl **69B** *SC* **69B.4.6.4** *P* **223** *L* **2** # 21

D'Ambrosia, John Tyco Electronics

Comment Type **E** *Comment Status* **R**

ICR Figure is inconsistent with other graphs in terms of formatting.

SuggestedRemedy

Label line on graph ICRmin
Invert y axis scale so ""0"" is in top left corner instead of bottom left corner.

Response *Response Status* **C**

REJECT.

There is no general rule here. The labeling of the "high confidence region" makes clear what the desired range of the parameter is.

Attenuation, insertion loss, and return loss are positive quanities, but the axes were inverted to appear more "natural" to those used to viewing channel parameters in terms of magnitude (see IEEE 802.3-2005, clause 54 for precedent).

Insertion loss deviation and insertion loss to crosstalk ratio are differences between two parameters, and the vertical axes are not inverted in these cases.

Cl **70** *SC* **70.7.1** *P* **66** *L* **52** # 36

Spagna, Fulvio INTEL

Comment Type **ER** *Comment Status* **A** *e*

Subscript on Random Jitter parameter is incorrect.

SuggestedRemedy

Change superscript form ""3"" to ""4""

Response *Response Status* **W**

ACCEPT.

Cl **70** *SC* **70.7.2.1** *P* **71** *L* **6** # 61

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **A** *check cl 72*

RMS jitter is a directly observable quantity: you record the jitter pdf and work out its RMS! A modern scope will do this for you. Therefore, you cannot define it in terms of other quantities.

SuggestedRemedy

Either change the name of your quantity, or change its definition to the usual one: the standard deviation of the edge timings, modulo modulo 1 average UI. You can say that true RMS jitter and your formula are apprioximately equal, if you like. Similarly in 71.7.2.1 and 72.7.2.1

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Change name "RMS Jitter" to "Applied Jitter" as this is the amount of jitter to be generated by the pattern generator in the Interference Tolerance test.

Specify the units of Applied Jitter to be RMS.

Change footnote to read
"The value of applied jitter is derived using the expression…"

Make similar changes to Clauses 71 and 72

Check Annex 69A for references to RMS Jitter that should now be renamed to "Applied Jitter"

Cl **70** *SC* **70.7.2.2** *P* **71** *L* **15** # 104

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A** *e*

Out of scope, but...

SuggestedRemedy

Consider changing '+/-' to the plus or minus symbol.

Response *Response Status* **C**

ACCEPT.

Cl **72** *SC* **72.6.10.2.3** *P* **105** *L* **12** # 34

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

The concept of update gain was originally introduced as a tool that could be used to reduce convergence time, anticipating that there may be a large number of steps. However, the step size and gain requirements imply that there could be a very limited number of steps, and this feature, if used, could simply drive the coefficient value to its limit with a single increment or decrement request.

SuggestedRemedy

Consider removing update gain from the coefficient update field and corresponding mirror register bits from Clause 45.

Response *Response Status* **C**

ACCEPT.

Note to Clause 45 editor to remove these fields from the appropriate management registers.

April editor note: Bit 15:14 are now 'reserved and transmitted as 0, ignored on reception'

Cl **72** *SC* **72.6.10.2.6** *P* **108** *L* **20** # 37

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

I have been told that there is no commercially available test pattern generator that can generate a prbs pattern of degree higher than 31. That being the case, it could be somewhat difficult to use a piece of test equipment to test or exercise the startup protocol in the receiver in a fashion that is equivalent to what happens in normal operation.

Since the startup protocol,as currently defined in Clause 69A, needs to be exercised in the EIT test I propose that the training pattern be changed to PRBS31.

SuggestedRemedy

Change figure and text to refer to the PRBS31 polynomial as defined by :

1 + x^28 + x^31

An example of such text and figure can be found in 802.3ae Clause 49.2.8

Response *Response Status* **W**

ACCEPT.

See Comment #5.

Cl **72** *SC* **72.6.10.2.6** *P* **109** *L* **21** # 5

Andre, Szczepanek Texas Instruments

Comment Type **TR** *Comment Status* **A**

The problem highlighted by Comment #130 on the previous draft regarding aligned training patterns is a real problem that must be addressed, however the solution implemented in the current draft is inappropriate.

1) Random seeding of the PRBS must be mandated (Whatever PRBS we use)

2) The change from PRBS11 to PRBS58 is unnecessary and detrimental

A PRBS58 sequence has a cycle time of 1 year at 10Gbps !.
With random initialization we have no guarantee of DC-Balance except over extremely long time scales. We went to a lot of trouble to ensure DC balance in the choice of both our previous training sequences, but now we have changed to a sequence with completely unknown DC balance during any reasonable training time.

Also the ability of the equalizer to converge will be very dependant on the section of PRBS58 sequence sent. With such a long sequence some sections of the sequence may have very little useful timing information for the equalizer to use. The time taken for equalizer convergence will be unpredictable and unrepeatable. The convergence point could also be off for the real traffic that the link will carry meaning the TX remains sub-optimal and could even stay sub-optimal if re-trained.

SuggestedRemedy

Return to the previous training sequence of two PRBS11 cycles plus two zero bits, but mandate random seeding of the PRBS11 register before the first training frame.
Subsequent frames can either use a rolling PRBS11 (that continues to shift through the 2 zero bits, frame marker and control channel), or re-use the same initial seed.

Response *Response Status* **W**

ACCEPT.

Reference #37
Return to the previous training sequence of two PRBS11 cycles plus two zero bits, but mandate random seeding of the PRBS11 register before every training frame.

Cl **72** *SC* **72.6.10.3.1** *P* **112** *L* **29** # 64

Noseworthy, Bob UNH-IOL

Comment Type **ER** *Comment Status* **A**

Root issue: Inappropriate subclause numbering.

Frame Lock and Training and Coefficient update (72.6.10.3.1,2,3) all indicate that the associated state diagrams shall be implemented, as well as the state variables of 72.6.10.2.7. But the state variable functions are defined in 72.6.10.2.8.

""72.6.10"" is PMD Control function.
""72.6.10.2"" is ""Training Frame Structure""
State variable definitions should not be a child of ""Training frame structure"", and all state variable subclauses (variables, timers, counters, and functions) should be children of the same parent clause.

SuggestedRemedy

Subclause ""72.6.10.2.7 State variables"" should be ""72.6.10.3 State variables""
Subclause ""72.6.10.2.7.1 Variables"" should be ""72.6.10.3.1 Variables""
Subclause ""72.6.10.2.7.2 Timers"" should be ""72.6.10.3.2 Timers""
Subclause ""72.6.10.2.7.3 Counters"" should be ""72.6.10.3.3 Counters""
Subclause ""72.6.10.2.8 Functions"" should be ""72.6.10.3.4 Functions""
Subclause ""72.6.10.3 State diagrams"" should be ""72.6.10.4 State diagrams""
Ammend cross references as necessary

Response *Response Status* **W**

ACCEPT.

Cl **72** *SC* **72.7** *P* **115** *L* **37** # 35

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

Table 72-8: The summary row for Differential Output Voltage is not necessarily accurate and at best misleading. The referenced subclause, 72.7.1.4, states that, for a 1010... pattern, the peak-peak differential output voltage shall not exceed 1200 mV. It also references 72.7.1.10, but at this time, this section currently does not bound the minimum peak-peak differential output voltage except in the special case where equalization is off. Only in this special case only is 800 mV peak-to-peak limit imposed, and there are no rules in place to guarantee that this holds in general.

SuggestedRemedy

The simplest path to consistency is to change the row to ""Differential peak-to-peak output voltage (max)"" with a value of 1200 mV.

However, if the Task Force elects to add new rules to the transmitter output waveform to make the 800 mV (or whatever number) minimum value apply in general, then that action would also satisfy this comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

change Table 72-6: from "Differential peak-to-peak output voltage" to ""Differential peak-to-peak output voltage (max)"" and change the value from "800-1200" to "1200" mV.

Cl **72** *SC* **72.7.1** *P* **115** *L* **49** # 38

Spagna, Fulvio INTEL

Comment Type **TR** *Comment Status* **A**

It is my recollection that at the San Diego interim an agreement was reached to the effect of reducing the Total Jitter from 0.30UI to 0.28UI (max. peak-to-peak). This has not been captured in the draft.

SuggestedRemedy

Change total jitter limit from 0.30 UIpp to 0.28 UIpp.

Response *Response Status* **W**

ACCEPT.

Motion #2
Change total jitter limit from 0.30 Uipp to 0.28 Uipp. Maximum DJ limit shall remain at 0.15UI p-p. Maximum RJ limit shall remain at 0.15UI p-p.

Moved by Fulvio Spagna
Second by Schelto van Doorn
Technical (>=75%)

All
Yes - 15
No - 0
Abstain - 11

Motion Passes

Cl **72** *SC* **72.7.1.10** *P* **120** *L* **1** # 40

Baumer, Howard Broadcom

Comment Type **TR** *Comment Status* **A**

This is a follow on to the unresolved comment number 45 from D2.2

SuggestedRemedy

Add in the transmit waveform template presented in baumer01_200603

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Refer to below motion #3.

Straw Poll #6
Adopt a transmit waveform template, as presented in baumer_01_0306, with the understanding that the proposed template would be subject to task force review during the balloting process.

Yes - 8
No - 12
Abstain - 8

Straw Poll #7
Adopt two test templates for the following -
1) Preset
2) Initialize

and the following-
Steady state ripple bound for each state

Yes - 13
No - 2
Abstain - 7

Straw Poll #8
Add a steady state ripple bound for each state

Yes - 14
No - 1
Abstain - 5

Motion #3
Move to add a steady state ripple bound for each state +/- 20 mV, T0+2UI to T1-2UI.
Move by Fulvio Spagna
Second by John D'Ambrosia
Technical (>=75%)
All
Yes - 20
No - 1
Abstain - 5

Motion passes

Cl **72** *SC* **72.7.1.10** *P* **120** *L* **34** # 28

Quackenbush, Bill independent

Comment Type **E** *Comment Status* **A**

The sentence "The changes in the transmitter output waveform resulting from coefficient update requests shall meet the requirements stated in Table 72-7." appears to apply to any update request regardless of the value of "Update gain" in the update request. However, this requirement is not clearly stated and thus potentially ambiguous. This requirement needs
to be unambiguously stated.

SuggestedRemedy

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See comment #34
Overtaken by events: Update gain field has been removed.

Cl **72** *SC* **72.7.1.10** *P* **121** *L* # 26

Quackenbush, Bill independent

Comment Type **T** *Comment Status* **R**

72.7.1.10 and 72.7.1.11: The definitions of Vpre and Vss in Figure 72-14 and the following text
of clause 72.7.1.11 are inconsistent with the required values of Rpre in Table 72-8 of clause 72.7.1.10. As defined, Vpre is a negative number and Vss is a positive number making Rpre, which is defined as Vpre/Vss, a negaitve number. However, Rpre is required to be a positive number in Table 72-8.

SuggestedRemedy

There are multiple ways of resolving this issue, some of which follow.

1) change the sign on the required values of Rpre in Table 72-8 to negative and "min" to "max",

2) change the definition of Vpre to be an absolute value or

3) change the definition of Rpre to be an absolute value.

Response *Response Status* **C**

REJECT.

Rpre= -Vpre/Vss which results in a positive number. (commenter did not see the negative sign)

Cl **72** *SC* **72.7.1.10** *P* **121** *L* **44** # 70

Noseworthy, Bob UNH-IOL

Comment Type **TR** *Comment Status* **A**

In D2.3, the variable ""Vpk"" is undefined.
The text was deleted in D2.2 for item (c) of 72.7.1.10 which did state: ""Vpk, which is defined as the sum Vpst - Vpre - Vss""

SuggestedRemedy

Restore definition of Vpk.

Change item (c) of D2.3 in 72.7.1.10 from:
""Any coefficient update equal to decrement applied to c(û1) or c(1) that would result in Vpk greater than 600 mV shall return a coefficient status value maximum.""

to:

""Any coefficient update equal to decrement applied to c(û1) or c(1) that would result in Vpk greater than 600 mV shall return a coefficient status value maximum. Vpk is defined as as the sum Vpst - Vpre - Vss""

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Change item (c) of D2.3 in 72.7.1.10 from:
""Any coefficient update equal to decrement applied to c(-1) or c(1) that would result in Vpk greater than 600 mV shall return a coefficient status value maximum.""

to:

""Any coefficient update equal to decrement applied to c(-1) or c(1) that would result in a violation of 72.7.1.4 shall return a coefficient status value maximum."

and change 'A' in figure 72-14 to 'Vpk'

Cl **72** *SC* **72.7.1.10** *P* **121** *L* **8** # 25

D'Ambrosia, John Tyco Electronics

Comment Type **TR** *Comment Status* **R**

""The transmiiter output waveform shall meet the requirements...""
No reference to meeting the waveform in 72.7.1.11. It also should be to a tx waveform template in 72.7.1.11.

SuggestedRemedy

Add a reference to meeting requirements of 72.7.1.11.
See Howard Baumer contribution on Tx waveform.

Response *Response Status* **W**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **72** *SC* **72.7.1.11** *P* **121** *L* # 27

Quackenbush, Bill independent

Comment Type **T** *Comment Status* **A**

The falling edge of the transmitter output waveform is completely unspecified. As currently specified, a transmitter with output waveform that has a compliant rising edge and a falling edge that would not be compliant if subjected to the same requirements as the rising edge would be compliant. This is not acceptable. Both edges need to specified.

SuggestedRemedy

There are multiple ways of resolving this issue, some of which follow.

1) require that the inverted transmitter output waveform shall also comply with the requirements of Tables 72-7 and 72-8 or

2) specify Vpre, Vpst and Vss for both rising and falling edges and require that these voltages and Rpre and Rpst meet the requirements of Tables 72-7 and 72-8 for both rising and falling edges.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the following into appropriate text and figures -

Specify Vpre, Vpst and Vss for both rising and falling edges and require that these voltages and Rpre and Rpst meet the requirements of
Tables 72-7 and 72-8 for rising edges.

The absolute value of Vrpre and Vfpre must be within 5%.
The absolute value of Vrpst and Vfpst must be within 5%.
The absolute value of Vrss and Vfss must be within 5%.

Add definitions for Vrpre, Vfpre, Vrpst , Vfpst,
Vrss and Vfss.
For example - Vrpre is equivalent to Vpre for the rising edge, while Vfpre is equivalent to Vpre for the falling edge.

Update equations for Rpre and Rpst to be-
Rpre = (-Vrpre / Vrss)
Rpst = (Vrpst / Vrss)

Update PICS

Cl **72** *SC* **72.7.1.8** *P* **119** *L* **39** # 60

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

per comment 34 reconsidered, I thought this was to become peak-to-peak duty cycle distortion. Otherwise we have a clash with the definition of DCD built into oscilloscopes, where an eye diagram from a mixed-frequency pattern is expected.

SuggestedRemedy

Change name per comment, or change pattern from 1010 to a mixed frequency pattern

Response *Response Status* **W**

REJECT.

The editor contacted test equipment vendor, and the test equipment vendor verified that duty cycle distortion is measured at the mean of the high and the low, and the algorithm will work equally with PRBS or clock-like patterns.

Reference comment #42 for method of measurement.

Cl **72** *SC* **72.7.1.8** *P* **119** *L* **41** # 42

Valliappan, Magesh Broadcom

Comment Type **TR** *Comment Status* **A**

When DCD is measured with AC coupling, the measured DCD is always less than the true DCD in the source clock. If the 1's are longer than the 0's, the waveform will shift lower after AC coupling. The zero crossing moves up, reducing the size of the +1s relative to the 0s, causing the measured DCD to be lower.

For slow edges of 40ps rise time, the measured DCD can be 0.6 times the true DCD. (0.08UI DCD may appear as 0.05UI). As the edges get faster this effect is reduced.

SuggestedRemedy

Removing the AC coupling clause may not be practical. Identify suitable test, otherwise spec measured DCD at a lower number like 0.03UIpp.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

DCD will be measured at the mean of the high and low voltage levels.

Cl **72** *SC* **72.7.2.1** *P* *L* # 62

Ghiasi, Ali Broadcom

Comment Type **TR** *Comment Status* **R**

This is pile on comment on Howard Baumer Unsatisfied comment

SuggestedRemedy

SuggestedRemedy: Accept remedy proposed by Howard Baumer in draft 2.2.

Response *Response Status* **W**

REJECT.

It is believed that the commenter is referring to Draft 2.2 comment #39 (22039).

No new information has been provided to rationalize the change. The response to Draft 2.2 comment #39 copied the response to Draft 2.1 comment #56, which indicated that Clause 74 FEC Sublayer could be used to achieve a BER better than 10^-15.

Cl **72** *SC* **72.7.2.1** *P* **123** *L* **42** # 69

Noseworthy, Bob UNH-IOL

Comment Type **TR** *Comment Status* **A**

There is no standard means to perform an EIT test of a clause 72 PMD, due to the use of the PRBS23 and the lack of any standard means of reporting BER information for this pattern.

The ability to perform the EIT Test on evaluation components, modules, as well as complete systems is necessary for validation.

Clause 49 10GBASE-R PCS requires a test pattern generator to be present (49.2.2). Table 72-1 indicates that 10GBASE-R PCS is required for 10GBASE-KR systems, hence, I would propose re-using the test pattern generator(49.2.8), checker(49.2.12) and management reporting mechanisms present in clause 45.

Note, this test pattern generation is already required for Transmit jitter testing per 72.7.1.9.

With this modification, all three 802.3ap PMDs could have approximations of the EIT testing performed in system with no non-standard system features required. It is noted that the frame-based EIT test patterns of clause 70 and clause 71 already allow for in-system testing, refer to Annex 58A for further discussion on frame based testing.

SuggestedRemedy

In Table 72-10, Replace ""PRBS23"" with ""Pseudo-random pattern defined in 49.2.8 with seed values shown in Table 52-2""

Response *Response Status* **W**

ACCEPT.

Cl **73** *SC* **73.10.1** *P* **155** *L* **21** # 85

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

The desire_np variable has been removed from the definition on page 155. However the desire_np variable is still showing up on Arbitration State diagram 73-12 on page 165. (Next page exchange happens irrespective of LD device desire to send NP) So Fix this problem in the state machine.

SuggestedRemedy

Fix the problem as per comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Delete statements that set the desire_np variable in states ABILITY DETECT and COMPLETE ACKNOWLEDGE.

Since the variable is never used, this does not change state machine behavior.

Cl **73** *SC* **73.10.1** *P* **156** *L* **48** # 13

Joergensen, Thomas Vitesse Semiconducto

Comment Type **E** *Comment Status* **A**

Incorrect reference to ""register 7""

SuggestedRemedy

Just reference Clause 45.2.7.9

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
This is for the next page to transmit so the reference should be 45.2.7.8.

Cl **73** *SC* **73.10.1** *P* **157** *L* **15** # 14

Joergensen, Thomas Vitesse Semiconducto

Comment Type **E** *Comment Status* **A**

Reference to ""Auto-Negotiation expansion register""

SuggestedRemedy

This should be the AN status register (Register 7.1)

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.10.4** *P* **165** *L* **24** # 15

Joergensen, Thomas Vitesse Semiconducto

Comment Type **E** *Comment Status* **A**

Figure 73-12: desire_np is no longer used

SuggestedRemedy

Delete ""IF(base_page = true * tx_link_code_word[NP] = 1) THEN desire_np <= true"" in state COMPLETE ACKNOWLEDGE

Delete ""desire_np <= false"" in state ABILITY DETECT

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.6.10** *P* **145** *L* **49** # 84

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

In the description for Next Page bit, If the device
does not have any Next Pages to send, the NP bit shall be set to logic zero.

However Next Page exchanges will occur if either the device
or its link partner sets the Next Page bit to 1.

So when setting NP bit to logic zero, it is also essential to write a Null Message to the local device NP registers. However this is not explicitly stated.

To avoid incorrect programming by the Station Management entity (interoperability) explicitly state that the LP NP registers need to be programmed to NULL message. So that even if the LD does not have a next page to transmit it is possible that the NP exchange will happen if the link partner indicates a desire to exchange next page. It may help to clear ACK2 bit to 0 to indicate to the remote partner that the local device cannot act on the next pages.

Right now the NULL message information is only provided in 73.7.7 (pg 149, line 3) for exchanging additional next pages, so modify text to include base page(or no next page) as well.

SuggestedRemedy

Add text as suggested in the comment to section 73.6.10 or to 73.7.7 Next page function.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add to 73.6.10 before the last sentence:
If a device has no next pages to send and its link partner has set the NP bit to logic 1, it shall transmit Next Pages with Null message codes and the NP bit set to logic zero while its Link Partner link partner transmits valid Next Pages.

Also, in the existing text change "1" to "logic one" for consistency.

Cl **73** *SC* **73.6.5** *P* **144** *L* **45** # 119

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

It would be just as simple or simpler to tread each direction independently: save power, latency, possible debug reasons. It's the receiver that has reasons to ask for FEC or not; the transmitter doesn't care, and the FEC status of the opposite direction is immaterial.

SuggestedRemedy

Change 'The FEC function shall be enabled on the link if both devices advertise FEC ability on the F0 bits and at least one device requests FEC enable on the F1 bits.' to 'The local device shall transmit with FEC if both devices advertise FEC ability on the F0 bits and the link partner requests FEC enable on the F1 bit.'.

Response *Response Status* **C**

REJECT.
The power and latency burden of bidirectional operation vs. unidirectional operation is not enough to justify adding extra operating modes to run FEC unidirectionally. Doing so adds extra operating modes that will need to be tested.

Also, we already considered this in the last ballot and no one except the original commentor has objected to our resolution so this comment is out of scope.

Cl **73** *SC* **73.7.7** *P* **148** *L* **31** # 83

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

Consider rephrasing the following sentence to remove the word ""arbitrary pieces of data"":

The Next Page function uses the Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data.

SuggestedRemedy

Here is a suggested remedy to rephrase the sentence:

The Next Page function uses the Auto-Negotiation arbitration mechanisms to allow exchange of Next Pages of information, which may follow the transmission and acknowledgment procedures used for the base Link Codeword.

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.8** *P* **150** *L* **38** # 59

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **A**

Response to comment 139 says 'Autonegotiation does require management intereaction with the PHY to complete because link code words must be read from and written to advance negotiation process.' I'm not convinced: for example, 73.3 says 'A management interface provides control and status of auto-Negotiation, but the presence of a management agent is not required.': I assume the link code words go across the link to the link partner, not over the MDIO to/from (not required) station management. And I assume AN (it's called AUTO-negotiotion, not MANAGED negotiation) will work without anything connected to any MDIO. Therefore there is no need to use the clause 45 Management Data Input/Output (MDIO) interface or logical interface to access the device registers for Auto-Negotiation or other management purposes.

SuggestedRemedy

Rewrite paragraph: 'A management interface may be used to communicate Auto-Negotiation information to a management entity. The optional Clause 45 Management Data Input/Output (MDIO) interface is recommended for access to the device registers for Auto-Negotiation and for management purposes. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended. Table 73û6 provides the mapping of state variables to management registers.' If you have genuine technical need for management access to one or two specific AN registers (not the whole of Clause 45!), call them out.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change
"The Clause 45 Management Data Input/Output (MDIO) interface shall be used for logical interface to access the device registers for Auto-Negotiation and other management purposes."

to

"MMD7 of the Clause 45 Management Data Input/Output (MDIO) interface shall be provided as the logical interface to access the device registers for Auto-Negotiation and other management purposes."

The commenter is correct that the document should be more specific about what part of 45 is mandatory, but we continue to want this part to be mandatory for the following reasons-

It is called auto-negotiation because hardware runs most of the negotiation but that doesn't mean it runs with no management interaction.

For example, there are state machine inputs from management: e.g. mr_next_page_loaded which must be set to transition from Complete Acknowledge state to Next Page Wait state.

Also you requested this change in the last ballot and no other voters have supported the request.

Cl **73** *SC* **73.8** *P* **151** *L* **1** # 45

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **R**

From D2.2 comment 139: 'state variable' not 'state diagram variable'.

SuggestedRemedy

Delete 'diagram'.

Response *Response Status* **C**

REJECT.
Same response as last time you submitted this.

Cl **73A** *SC* **73A.2** *P* **226** *L* **17** # 29

Law, David 3Com

Comment Type **T** *Comment Status* **A**

The current figure is non-optimal with all the lines that cross-over. The bit order is also the opposite to that shown in Figure 28C-1.

Now I agree that the bit order of Figure 28C-1 is not particularly clear as neither LSB/MSB of D0/D15 is marked however I believe that based on the greyed out portion to the right of each user code representing the T,Ack2,MP,Ack & NP bits, Figure 28C-1 shows the pages in the order they are transmitted, with the first transmitted page on the left, but shows the bits from each page with the first transmitted bit of each page on the right. Based on this I have placed a comment against IEEE P802.3an to mark D0 and D15 on Figure 28C-1 as well as adding a note to Figure 28C-1 that the bit order is the opposite from normal, and in particular from Figure 28-11 and 28-12 which define the Message and Unformatted Next Pages used.

SuggestedRemedy

[1] Redraw Figure 73A-1 to be the same bit order as Figure 28C-1.

[2] Add a note to Figure 73A-1 that the bit order is the opposite from normal, and in particular from Figure 28-11 and 28-12 which define the Message and Unformatted Next Pages used.

Please find FrameMaker file of the redrawn figure as well as suggested text for note.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Keep existing picture.

The message code will be fixed and a note will be added to indicate bit order and convention is different than that used in Annex 28C.
Figure 28C-1 shows the order Next Pages are transmitted, with the first transmitted Next Page shown in the leftmost position. While Figures 28-11 and 28-12 use the convention that the most significant bit (i.e. the last bit to be transmitted) is the rightmost bit, Figure 28C-1 uses the opposite convention, i.e., the most significant bit of each page is shown in the leftmost position. This is a pictorial difference only; there is no difference in the actual order of bits transmitted

Cl **73A** *SC* **73A.2** *P* **226** *L* **17** # 39

Baumer, Howard Broadcom

Comment Type **T** *Comment Status* **A**

The message code bits in Figure 73A-1 are reversed, shown msb to lsb. The picture has the bits labeled lsb to msb

SuggestedRemedy

Flip the message code bits to be lsb to msb

Response *Response Status* **C**

ACCEPT.

Cl **73A** *SC* **73A.2** *P* **226** *L* **24** # 66

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

The Figure 73A-1 is incorrect.

Figure 73-7 and Figure 73-8 defines the message code field and unformated code field word order.

A DME page is D0:D47, where D0 is sent first on the medium.
The message code field, M10:M0 (as defined in Table 73A-1) is sent such that bit M0 is sent first, thus a message code #5 would be sent M0:M10=1010 0000 000(b)

The original Clause 28 encoding for message code #5, per 28C.6 utilized 5 11-bit code fields to convey the 11bit message code and the 24bit OUI + 20bit user-defined message. Figure 28C-1 correctly shows this process and is consistent with the definition of 28C.6

Figure 73A-1 displays the message code in the incorrect order. Displays ""reserved bits"" between 11-bit blocks of the unformated message code field for both the Message Next Page and the Unformatted Next Page. The 11-bit grouping is artificial and unnecessary. The unformatted message code field in a message next page is 32-bits, and 42 bits in a unformatted next page.

SuggestedRemedy

Redefine 73A.2 as follows:
""
The OUI tag code message shall consist of a Message Next Page followed by one Unformatted Next Page where the pages are defined as follows. This message code conveys the 24 bit OUI and a 20 bit user-defined code. The message code field of the Message Next Page shall be encoded per Table 73A-1. The Message Next Page contained unformatted code field bits U[23:0] shall contain the OUI (bits 23:0), and unformatted code field bits U[31:24] shall contain bits 19:12 of the user-defined code. In the Unformatted Next Page, the unformatted code field bits U[11:0] shall contain bits 11:0 of the user-defined code.
""

Strike figure 73A-1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Accept that the message code is reversed in the figure. It will be reversed.

The packing of bits to use 11 bits of each 16 was to have the bit packing in this Message 5 be the same as the Clause 28 Message 5 to help management agents that interface to both kinds of auto-negotiation.

Also, the figure was added to Clause 28 because it was requested in the Rev-am ballot. It is just as needed here.

Cl **73A** *SC* **73A.3** *P* **226** *L* **44** # 67

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

Referencing the clause 22 MII registers 2 and 3 seems improper here.
As each clause 45 MMD has seperate identifiers, a single next page message code to identify a systems ""PHY"" seems unwieldy.

SuggestedRemedy

Delete 73A.3 and message code 6 from Table 73A-1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change to reference the AN device identifier from registers 7.2 and 7.3

Cl **74** *SC* **74** *P* **176** *L* **1** # 33

Healey, Adam Agere Systems

Comment Type **T** *Comment Status* **A**

There are no delay constraints for the Clause 74 FEC sublayer. Implementations wishing to use MAC Control PAUSE need to know that the upper bound on this delay is constrained.

SuggestedRemedy

Add section titled ""Delay Constraints"" that places an upper bound on the round-trip through the FEC encoder/decoder. Use subclause 72.4 as a template.

This new bound should also be reflected in Table 69-3 - Round-trip delay constraints for 10GBASE-KX4 and 10GBASE-KR.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Also refer to comment #86, #49, #81

Use subclause 49.2.15 as template
Discuss the proposed max delay .
74.4 Delay constraints
49.2.15 Delay constraints
Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay contributed by the 10GBASE-R FEC shall be no more than 6144 BT.

Also insert the following line to 802.3-2005 table 44-2 Round trip delay constraints and to table 69-3 (refer comments #49, #81)
10GBASE-R FEC maximum 6144 BT, maximum pause quanta 12, see 74.4

Cl **74** *SC* **74.** *P* **194** *L* **35** # 7

Szczepanek, Andre Texas Instruments

Comment Type **E** *Comment Status* **A**

"Figure 74-13 - Reconstructing sync bits in 64b66b blocks" - doen't provide any information on how to reconstruct the sync bits.

SuggestedRemedy

Add text indicating
SH.1 = about T
SH.0 = T
where T is the unscrambled transcode bit

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In subclause 74.8.4.5.1 in a,b,c,d instead of x0, x1 replace with SH.0 and SH.1 as per suggested remedy, and add reference to figure 74-8 Receive bit ordering. Also delete figure 74-7 which is redundant, and highlight SH.0, SH.1 and descrambled Transcode bit T in the figure 74-8.

Cl **74** *SC* **74.10** *P* **197** *L* **38** # 114

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Subclauses not properly nested

SuggestedRemedy

should be 74.9.1, 74.9.2 and so on to current 74.14.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

All subclauses that refer to Management variables are to be nested under 74.9 FEC MDIO function mapping as suggested.

The subclause with title "10GBASE-R PHY test-pattern mode" does not fall under this category and hence move this subclause to be after the 74.9 FEC MDIO function mapping.

Cl **74** *SC* **74.10** *P* **197** *L* **40** # 11

Andre, Szczepanek Texas Instruments

Comment Type **T** *Comment Status* **A**

The first line of 74.10 makes the implementation of FEC decoding error indication via sync bits mandatory. In conjunction with the requirement to indicate decoding errors on the 1st 64b66 word of a block this DOUBLES the decoder latency.
In order to indicate an uncorrectable block in word zero 4K bits of latency are required. One frame time is required to generate the frame error syndrome. A second frame time is required to test all possible burst error locations. Only then after 2 frame latencies is it known whether the frame is correctable or not.
Making this mandatory will require all implementations to implement a second frame buffer to hold the frame awaiting error corrector completion, this buffer can be bypassed if error indication is disabled.

SuggestedRemedy

Remove the mandatory implementation of this option.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Replace "shall" with "may" in 74.10 line 1 as follows:

"The FEC sublayer may have the option to enable the 10GBASE-R FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-R PHY as defined in 74.8.4.5, if this ability is supported."

Modify appropriate PICS.

Modify clause 45.2.1.84.1. Add FEC error indication ability bit to register 1.170.

Cl **74** *SC* **74.12** *P* **197** *L* **5** # 116

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Stray capital

SuggestedRemedy

10GBASE-R PHY test-pattern mode

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.13.1** *P* **198** *L* **22** # 9

Szczepanek, Andre Texas Instruments

Comment Type **E** *Comment Status* **A**

We should define somewhere what a corrected block actually is.
A corrected block is not necessarily the original block. It is a block that had a syndrome equivalent to a <12 bit burst error.
Some non-burst errors in a block will have the same syndrome as a <12 bit burst and be corrected as the equiavelent <12 bit burst. The error corrector cannot discriminate between them. Error correction is a best-effort thing.

SuggestedRemedy

Add definition:
A corrected block is a block that had bad parity that the error corrector has attempted to correct.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add the following text to 74.13.1 FEC_corrected_blocks_counter

"A corrected block is a block that has invalid parity and that the error corrector in the FEC decoder has attempted to correct."

Cl **74** *SC* **74.13.2** *P* **198** *L* **28** # 52

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

There is no definition of what an uncorrected block is.

SuggestedRemedy

Assuming you don't mean a block that hasn't been corrected (including a perfect block), add a sentence saying what you do mean: a block that the FEC sublayer has determined contains errors and that it has not confidently corrected. And change 'uncorrected' to 'uncorrectable' throughout the draft.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Also refer to comment #10

Add definition for uncorrected block to 74.13.2 line 1 as follows:

An uncorrected block is a block that has invalid parity and that the error corrector in FEC decoder could not correct.

Proposal to rename uncorrected to uncorrectable was discussed on D2.2 and was not accepted (refer to comment #22114)

Cl **74** *SC* **74.13.2** *P* **198** *L* **28** # 10

Szczepanek, Andre Texas Instruments

Comment Type **E** *Comment Status* **A**

We should define somewhere what a uncorrected block actually is.
An uncorrected block is is a block that had a syndrome that does not map to a <12 bit burst error.

SuggestedRemedy

Add definition:
An uncorrected block is a block that had bad parity that the error corrector could not attempt to correct.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer response to comment #52

Cl **74** *SC* **74.14** *P* **198** *L* **47** # 118

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

Thinking about unidirectional FEC: I don't believe there is any burden of managing asymmetric operation, it may even be a simplification to treat each direction independently. It's the receiver that has reasons to ask for FEC or not; the transmitter doesn't care. So a very simple algorithm is: LD asks for FEC when it wants to recieve FEC, LP obliges by transmitting FEC if it wishes. No attempt to, or need to, consider the opposite direction.

SuggestedRemedy

Change 'The FEC function is only enabled on the link if both link partners advertise they have FEC ability and either one of them requests to enable FEC through the Auto-Negotiation function.' to 'A local device enables the FEC function on its transmitter if both link partners advertise they have FEC ability and its link partner requests to enable FEC through the Auto-Negotiation function.'.

Response *Response Status* **C**

REJECT.

This comment on D2.2 was discussed in the task force during Feb'06 interim. Refer response to comment #22116.

The proposal to change to assymmetric operation was discussed and not accepted by the Task Force.

Refer to comment #120

Cl **74** *SC* **74.15.2** *P* **199** *L* **13** # 65

Noseworthy, Bob UNH-IOL

Comment Type **ER** *Comment Status* **A**

Inappropriate subclause numbering.

""Constants"", ""Variables"", ""Functions"" and ""Counters"" should be children of the parent subclause ""74.15.2 State Variables""

SuggestedRemedy

Replace ""74.15.3 Constants"" with ""74.15.2.1 Constants""
Replace ""74.15.4 Variables"" with ""74.15.2.2 Variables""
Replace ""74.15.5 Functions"" with ""74.15.2.3 Functions""
Replace ""74.15.6 Counters"" with ""74.15.2.4 Counters""
Replace ""74.15.7 State diagrams"" with ""74.15.3 State diagrams""

Renumber subclauses and cross references accordingly.

Response *Response Status* **W**

ACCEPT.

Cl **74** *SC* **74.15.7** *P* **199** *L* **1** # 57

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

This unnecessarily prescriptive state diagram looks very much like specifying an implementation. It's far harder to understand than the previous flow diagram 74-15, and therefore very hard to debug.

SuggestedRemedy

Revert to the previous flow diagram 74-15 with any modifications agreed. If you want something mandatory, write down what OUTCOME you actually want: ' shall gain sync in X us at a BER of Y, shall lose sync within Z us at a BER of A' or whatever it is that you care about. Don't specify the method unnecessarily.

Response *Response Status* **W**

REJECT.

The state machine was added in response to comments #22159 & #21181 and was discussed in the task force during Feb'06 interim. Refer response to comment #22159.

The state machine captures the desired behavior in a manner consistent with similar functions in the IEEE 802.3 specification.

Cl **74** *SC* **74.15.7** *P* **199** *L* **1** # 44

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **R**

Why is this state diagram so many subclauses away from 74.8.4.7 FEC block synchronization?

SuggestedRemedy

Re-order the subclauses

Response *Response Status* **C**

REJECT.

The subclauses for FEC MDIO function and control/status variables of FEC sublayer are organized after the subclauses that define FEC functions, so that the reader can clearly understand the control/status of the functional sub-blocks.

Also the state machine at the end of the Clause is consistent with organizing state machines in other Clauses.

Cl **74** *SC* **74.15.7** *P* **200** *L* **26** # 56

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **A**

This state machine doesn't do what the text says.

SuggestedRemedy

In order to count CONSECUTIVE good/bad blocks, the counters parity_good_cnt and parity_invalid_cnt each need to be reset when the opposite one increments.

Response *Response Status* **W**

ACCEPT.

Fix the state machine as proposed

Refer to comment #87

Cl **74** *SC* **74.15.7** *P* **200** *L* **28** # 68

Noseworthy, Bob UNH-IOL

Comment Type **T** *Comment Status* **A**

Normative reference to state machines does not reference state machine explicitly nor are the state variables normatively cited.

SuggestedRemedy

Replace:
""The FEC Lock state machine shown in Figure 74û16 determines when the PCS has obtained lock to the received data stream.
The FEC sublayer shall perform the functions of FEC Lock function as specified in these state machines.""

With:
""The FEC sublayer shall implement the FEC Lock state machine shown in Figure 74-16 including complance with the associated state variables as specified in 74.15.2. The FEC Lock state machine determines when the receiver has obtained FEC block lock on the received data stream.""

Response *Response Status* **C**

ACCEPT.

Replace
""The FEC Lock state machine shown in Figure 74û16 determines when the PCS has obtained lock to the received data stream. The FEC sublayer shall perform the functions of FEC Lock function as specified in these state machines.""

To

""The FEC sublayer shall implement the FEC Lock state machine shown in Figure 74-16 including compliance with the associated state variables as specified in 74.15.2. The FEC Lock state machine determines when the receiver has obtained FEC block lock on the received data stream.""

Cl **74** *SC* **74.15.7** *P* **201** *L* **16** # 58

Dawe, Piers Avago Technologies

Comment Type **TR** *Comment Status* **R**

I understand the wish to seach for perfect (don't need correcting) blocks when looking for sync: allows to slip much faster and sync quicker. But this machine will throw away lock on 8 consecutive corrected blocks (no errors at PCS) and then take on the order of 1000+ blocks to regain sync. If bursts of interference are possible, perhaps if a neighbouring card is being plugged in, this is not the desired behavior: truly losing sync is not a likely thing to happen so the algorithm should be really sure before giving up the link. It costs just one FEC latency to count just uncorrectable blocks when losing sync, rather than errored but correctable and uncorrectable blocks

SuggestedRemedy

Change the algorithms to count just uncorrectable blocks when losing sync. Consider increasing m.

Response *Response Status* **U**

REJECT.

Verifying a parity match is simpler to determine whereas identifying correctable parity requires the complete correction machine to test all syndromes and correct errors which adds to latency and complexity.

8 consecutive blocks in error is indicative of a BER no better than 10^-4. The error correcting code can't improve this to an acceptable BER, therefore there is no need to maintain lock.

Cl **74** *SC* **74.16.1** *P* **202** *L* **7** # 47

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Should mention the clause number

SuggestedRemedy

Here: Clause 74, Forward Error... At line 36, IEEE Std 802.3ap-200x, Clause 74, Forward Error...

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.16.4** *P* **204** *L* **39** # 48

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

FEC_able

SuggestedRemedy

FEC_ability ?

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change FEC_able to FEC_ability on row M7

Cl **74** *SC* **74.3** *P* **176** *L* **32** # 107

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

10GBASE-R PCS and PMA

SuggestedRemedy

10GBASE-R PCS, PMA and PMD

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.4** *P* **177** *L* **16** # 108

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Thank you for your attention to font size!

SuggestedRemedy

You missed one: PMA

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.4.1** *P* **180** *L* **5** # 109

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Thank you for the changes to this diagram. A few still to do:

SuggestedRemedy

PCS (and other) service interface (scrub Clause 74 for 'Service Interface'), BER, FEC functional block diagram

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "Ber" to "BER" as suggested
Change to "FEC functional block diagram as suggested".

Changed capitalization in "Service Interface" to "service interface" in the diagram and to the rest of clause 74 as suggested.

Cl **74** *SC* **74.5** *P* **43** *L* **44** # 86

Ganga, Ilango Intel

Comment Type **TR** *Comment Status* **A**

Provide Maximum Delay constraints for the 10GBASE-R FEC sublayer.

SuggestedRemedy

Add a subclause 74.5 to include the maximum delay constraints for 10GBASE-R FEC

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer response to comment #33 for remedy

Cl **74** *SC* **74.5.2** *P* **181** *L* **12** # 43

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Subclauses not nested appropriately. All the primitives should come under 74.5 FEC Service Interface.

SuggestedRemedy

74.4.1 FEC_UNITDATA.request 74.5.1.1 Semantics of the service primitive 74.5.1.2 When generated 74.5.1.3 Effect of receipt 74.5.2 FEC_UNITDATA.indication and so on to 74.5.3.3 Effect of receipt

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.8.4.2** *P* **184** *L* **38** # 6

Szczepanek, Andre Texas Instruments

Comment Type **E** *Comment Status* **A**

The first 2 sentences of 74.8.4.2 read:

The FEC encoder connects to the PCS Gearbox function using the 16-bit tx data-group. The FEC encoder takes 32x64b/66b blocks from the PCS and encodes it into a single FEC block of 2112 bits.

This ignores the existence of the Reverse Gearbox.

SuggestedRemedy

I think it should read :

The FEC encoder connects to the Reverse Gearbox function using the 64b66b blocks. The FEC encoder takes 32x64b/66b blocks from the Reverse Gearbox and encodes them into a single FEC block of 2112 bits.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Also refer to comment #79

Modify the text as follows:

The FEC encoder connects to the reverse gearbox function using the 66-bit wide data path. The FEC encoder takes 32 x 64b/66b blocks from the reverse gearbox and encodes it into a single FEC block of 2112 bits.

Cl **74** *SC* **74.8.4.2** *P* **184** *L* **39** # 79

Ganga, Ilango Intel

Comment Type **ER** *Comment Status* **A**

Rephrase the sentence (line 39) to include Reverse Gear box function as follows:

The FEC encoder takes 32 x 64b/66b blocks from Reverse Gearbox and encodes them into a single FEC block of 2112 bits.

SuggestedRemedy

As per comment

Response *Response Status* **C**

ACCEPT.

Also refer to comment #6

Cl **74** *SC* **74.8.4.3** *P* **187** *L* **13** # 102

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

There's a symbol for circled plus which should be available in Frame.

SuggestedRemedy

When you find it, use it in Fig 74-5 and 74-14,and have it added to the table of 'Special symbols and operators'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "Circle Plus" symbol to XOR in figures 74-5 and 74-14.

Cl **74** *SC* **74.8.4.3** *P* **187** *L* **19** # 110

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Thank you for the changes to this diagram. Some stray capitals remain.

SuggestedRemedy

Aggregate 32 65b blocks plus 32b Parity. Also, Reconstruct 64b/66b blocks in fig 74-10, error correction in fig 74-14.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change text to Fig 74-5 as follows: "Aggregate 32 65b blocks plus 32b Parity"

Change text to Fig 74-10 as follows: "Reconstruct 64b/66b blocks"

In figure 74-14, Decoder and Error correction are two separate functions so capital letter for Error correction function is justified. So no changes are made to Error correction.

Cl **74** *SC* **74.8.4.4** *P* **187** *L* **39** # 112

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Wrong table number?

SuggestedRemedy

74-7?

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change to Figure # of FEC encoder 74-4

Cl **74** *SC* **74.8.4.4** *P* **189** *L* **9** # 111

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Thank you for your attention to font size!

SuggestedRemedy

You missed two: 64b/66b blocks<65:0> and tx_data-group<15:0> (to PMA). In fig 74-14, tx_data-group<0> (PCS) tx_data-group<15> (PCS)

Response *Response Status* **C**

ACCEPT.

Cl **74** *SC* **74.8.4.5.1** *P* **192** *L* **37** # 113

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Don't know what Operation Mode Flags are: it's not Clause 45 language.

SuggestedRemedy

Control registers? variables?

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change to "Control/status variables" (from MDIO registers)

Cl **74** *SC* **74.8.4.5.1** *P* **194** *L* **30** # 54

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **R**

If the code can correct up to an 11-bit burst (i.e. no implementation could correct all 12-bit bursts), is it in the tradition of Ethernet to demand an essentially perfect implementation? Would we gain significantly in cost, heat or latency by relaxing the 'shall be able' to 8 or 10 bits?

SuggestedRemedy

Choose a value that represents reasonable, not excellent, implementations.

Response *Response Status* **C**

REJECT.

The Task Force believes that relaxing the implementation will not provide any significant gains in cost, heat, or latency. The Task Force believes that correcting for an 11-bit burst is a reasonable rather than an excellent implementation.

Cl **74** *SC* **74.8.4.7** *P* **196** *L* **44** # 51

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

This text is not clear what 'evaluate parity' means: it could be that correctable blocks are counted as OK, or just perfect blocks. The state machine detail talks about 'parity check matches' but still this is not precise information.

SuggestedRemedy

Whatever is decided, make this text, and FEC_PARITY_CHECK (if it remains) clearer

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change74.8.4.7 a(2)(1) from
"If it fails shift candidate start by one bit position and try again"

to

"If the parity does not match (the received parity does not match the computed parity), shift candidate start by one bit position and try again."

Cl **74** *SC* **74.8.4.7** *P* **196** *L* **49** # 87

Ganga, Ilango Intel

Comment Type **TR** *Comment Status* **A**

Currently there is a descrepancy between the lock state machine 74-16 and the description in 74.8.4.7: (d) ""If 'm' consecutive blocks are received with bad parity, drop Block Sync and restart again at 1"".

The state machine does not look for 'm' consecutive blocks to go out of sync. Instead it goes out of lock when there were no n good blocks when the bad parity counter reaches m.

Either fix the state machine to follow conventional n/m locking technique or change the text to reflect the lock state machine

SuggestedRemedy

As per comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer response to comment #56. Fix the FEC lock state machine. The FEC Lock state machine will then be consistent with Clause 49 64b/66b lock state machine.

Cl **74** *SC* **74.8.4.7** *P* **196** *L* **50** # 8

Szczepanek, Andre Texas Instruments

Comment Type **E** *Comment Status* **A**

In section 74.8.4.7 is item e) really necessary ?.
Once block sync is established Block Sync should be reported continuously unless m consecutive bad parity blocks are received. item e) implies that block sync will be dropped if the previous n blocks didn't have good parity.

SuggestedRemedy

Either remove item e)
or make it sub-item 2 of item b)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Remove item (e) and make it a sub-item of item b)
And in item d) modify the last sentence to "restart again at (a)" instead of "restart again at 1"

Cl **74** *SC* **74.9** *P* **197** *L* **30** # 115

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **R**

The language of the subclause and table titles should follow the bit name

SuggestedRemedy

Change 'capability' to 'ability' in titles of Table 74-3 and 74.14.

Response *Response Status* **C**

REJECT.

FEC capability indicates that the 10GBASE-R PHY supports variables FEC ability and FEC Enable. Also the same title is used in other clauses 45 and clause 73 to refer FEC capability.

Cl **74A** *SC* **74A** *P* **229** *L* **8** # 96

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

Annex (or clause) gets a capital when it's part of a specific (numbered) noun e.g. 'Clause 45', not without: 'this annex'

SuggestedRemedy

Change to 'annex'. Similarly 'clause' in 74.1.

Response *Response Status* **C**

ACCEPT.

Cl **74A** *SC* **74A.1** *P* **229** *L* **16** # 97

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

output of PCS layer

SuggestedRemedy

output of the PCS layer

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make changes as suggested in remedy.

Also make similar changes to 74A2 and 74A.3, change to "output of the FEC (2112,2080) encoder" instead of "output of FEC(2112,2080) encoder".

Cl **74A** *SC* **74A.2** *P* **229** *L* **16** # 98

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **R**

Table 74A-1 appears to be the same as all but the last row of Table 74A-2 (I didn't check it all!) It would be easier for the reader to have that stated in words.

SuggestedRemedy

Delete table 74A-1, refer to 'all but the last row of Table 74A-2' (which will become Table 74A-1).

Response *Response Status* **C**

REJECT.

Table 74A-2 is different from Table 74A-1.

Table 74A-1 is uncoded 64b/66b symbols whereas
the Table 74A-2 is the FEC block in which the two sync bits are compressed to 1 transcode bit and the FEC parity is appended to the end of the frame.

Cl **74A** *SC* **74A.2** *P* **229** *L* **16** # 99

Dawe, Piers Avago Technologies

Comment Type **E** *Comment Status* **A**

The Table 74A-1

SuggestedRemedy

Delete 'The'. Also in 74A.2.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

As proposed delete "The" before "Table" in 3 places 74A-1, 74A-2 and 74A-3.

Cl **74A** *SC* **74A.2** *P* **229** *L* **19** # 117

Dawe, Piers Avago Technologies

Comment Type **T** *Comment Status* **A**

You say 'The first bit out on the wire starts at the top left hand corner.' Top left corner contains a hex symbol 4 (not a bit). Is that sent MSB first or LSB first?

SuggestedRemedy

Please add a sentence to specify which order the bits in a hex symbol are sent.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Remove

"The first bit out on the wire starts at the top left hand corner" from each of the subclauses in 74A.

Instead add the following paragraph to the end of first paragraph of 74A to indicate this is applies globally to all subclauses in this annex.

"The data pattern in this annex is represented in a tabular form. For the tables within this annex the contents are transmitted from left to right within each row and from top to bottom between rows. The first bit out on the wire starts at the top left hand corner. Note that there is both binary representation and hexadecimal symbol representation in the table; in case of the hex symbol, the most significant bit of each hex symbol is sent first."

Refer to ganga_01_0306.

Cl **74A** *SC* **74A.3** *P* **230** *L* **35** # 12

Andre, Szczepanek Texas Instruments

Comment Type **T** *Comment Status* **A**

The Scambled Frame Sequence shown in Table 74A-3 incorrect.

SuggestedRemedy

Ilango has prepared a new table which I have verified. Replace Table 74A-3 with it.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Replace table 74A-3 as as in ganga_01_0306. Also refer to comment #88

Cl **74A** *SC* **74A.3** *P* **230** *L* **40** # 88

Ganga, Ilango Intel

Comment Type **TR** *Comment Status* **A**

Scrambling the data pattern in Table 74A-2 with PN-2112 sequence provides a different result as compared to the pattern in Table 74A-3.

Fix the data pattern in Table 74A-3 as per attached document.

SuggestedRemedy

Fix the data pattern in Table 74A-3 as per attached document.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Refer response to comment #12

Cl **74A** *SC* **74A.4** *P* **230** *L* **53** # 82

Ganga, Ilango Intel

Comment Type **T** *Comment Status* **A**

To avoid any ambiguity in generating the PN-2112 sequence, consider to include the PN-2112 sequence in a separate table (say 74-A4) to informative annex 74A.

SuggestedRemedy

As per comment

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Include table 74A-4 with PN2112 sequence with appropriate text as in ganga_01_0306

Cl **99** *SC* **99** *P* **2** *L* **23** # 32

Healey, Adam Agere Systems

Comment Type **E** *Comment Status* **A** *e*

In the ""Keywords"" sections, strike the word ""for"" following ""Forward Error Correction (FEC)"".

SuggestedRemedy

Per comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Changed text to ""forward error correction (FEC)"" as per comment #103