TP3 Stressed Receiver Test System Progress Report

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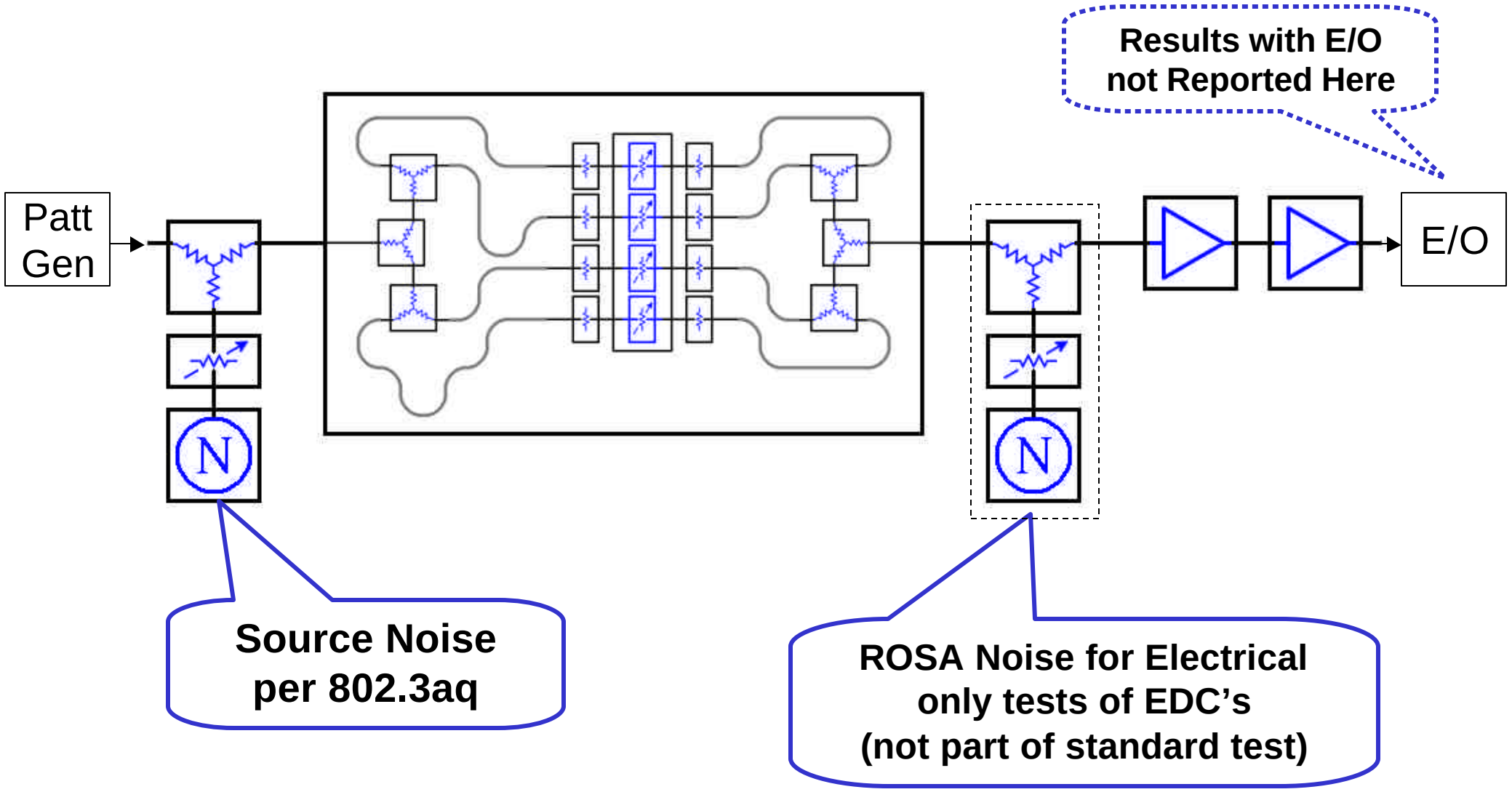
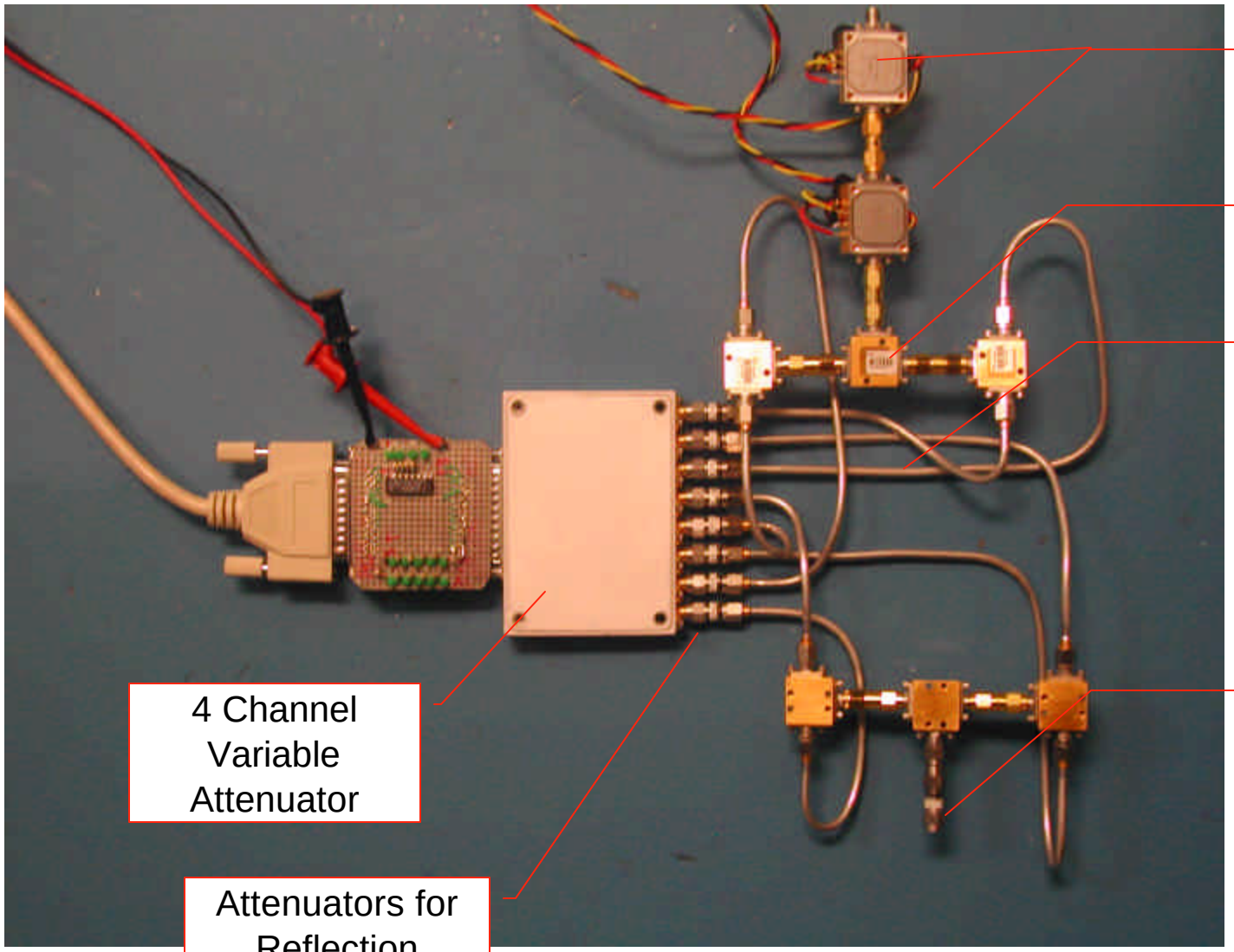
Introduction

- TP3 Comprehensive Stressed Receiver Test is Critical EDC Compliance Test.
- D1.1 Defines System with 4-Tap ISI Generator, Noise Loading and Optical to Electrical Converter.
- Practicality of Test and Achievable Accuracy of Impulse Response Generation is Critical
  - Errors in Impulse Generation Could Result in Significant Under- or Over Stress of Receiver.
  - If Errors are Large, Test IPRs Would Need to Be Less Than Worst Case Channel Responses to Avoid Overly Difficult Tests.
- This Work Describes First Results of Test System Development

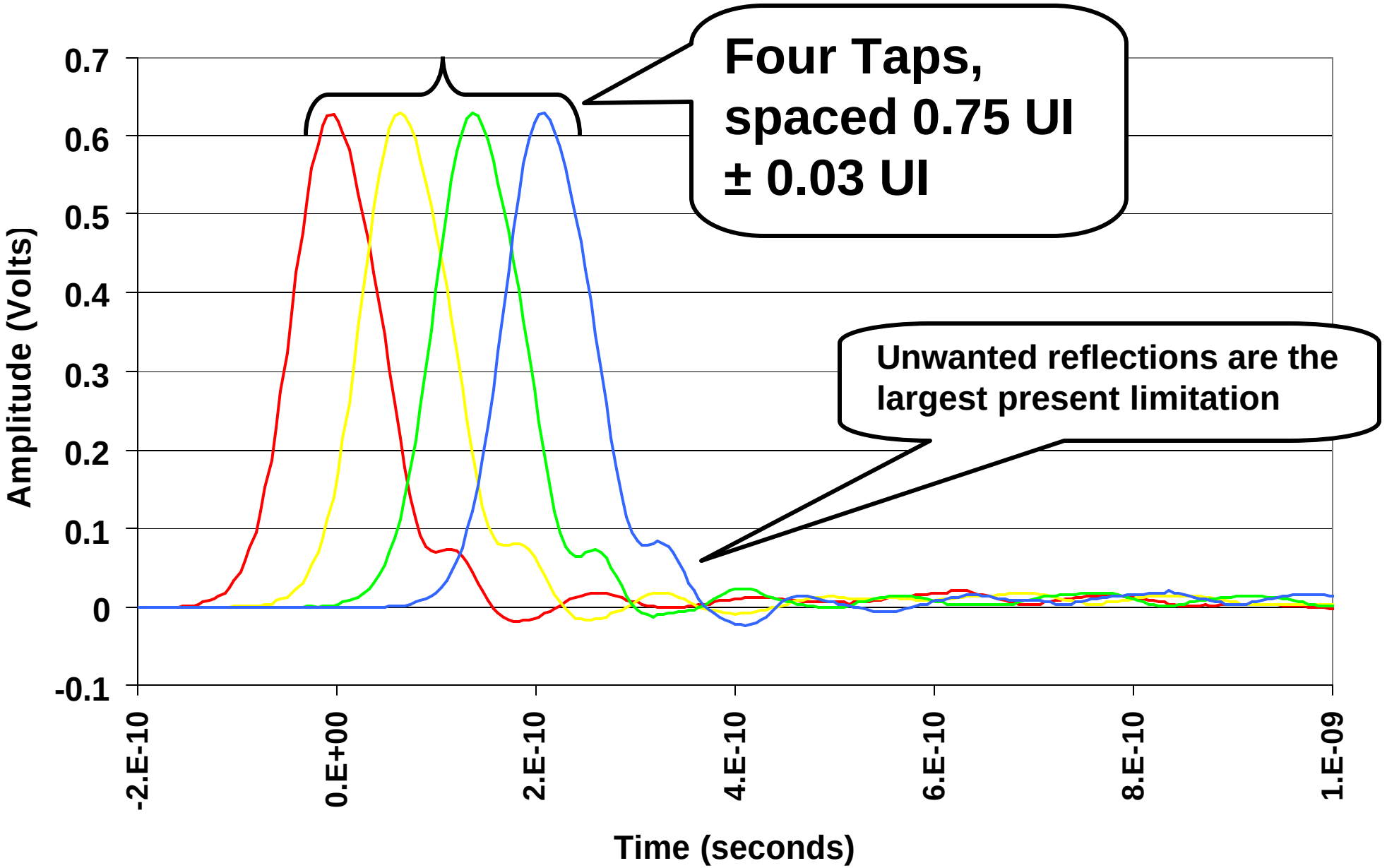
4-Tap Noise & ISI generator



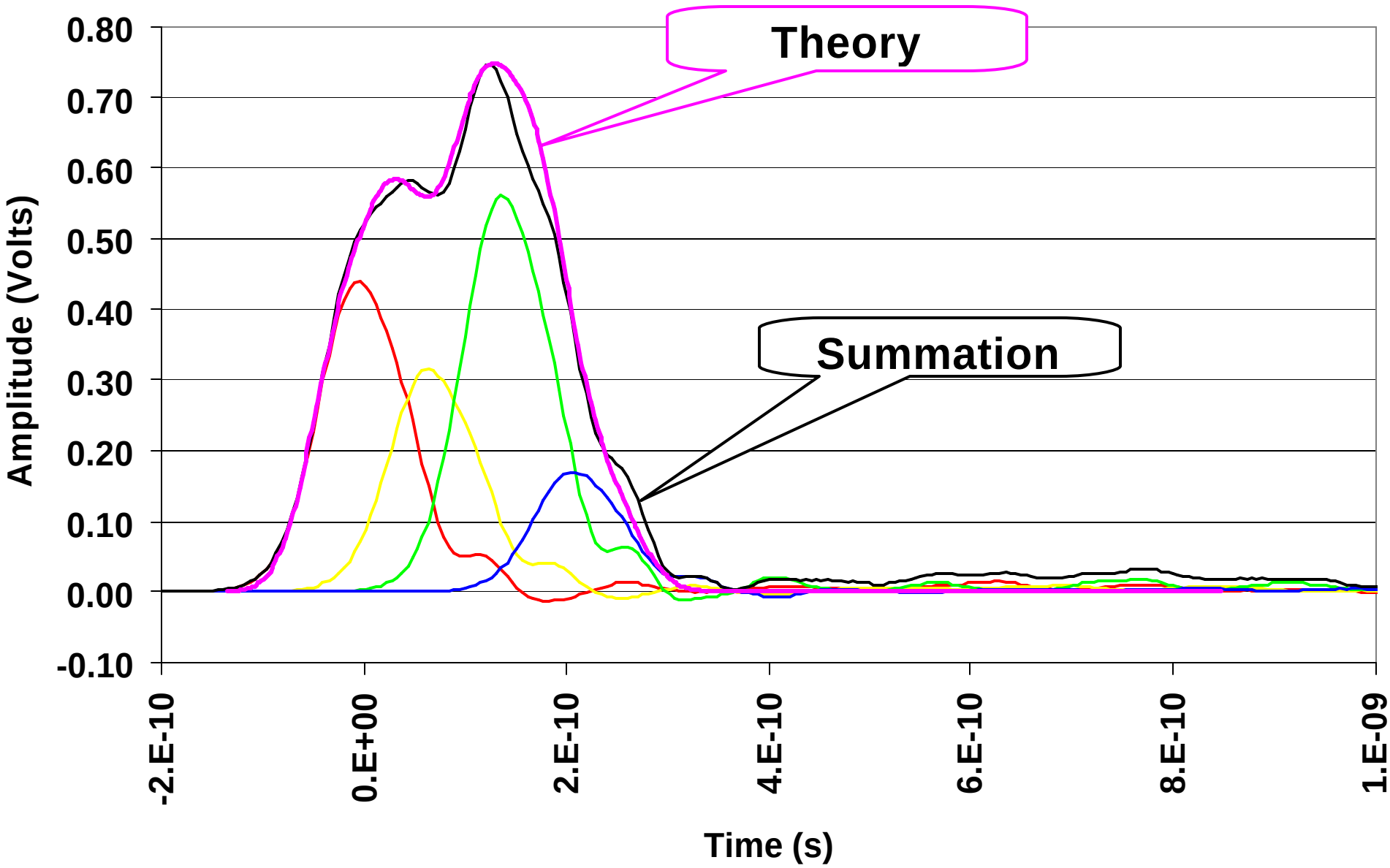
4-Tap ISI Generator Hardware



Composite Voltage vs Time Plot for 4 Tap ISI Generator



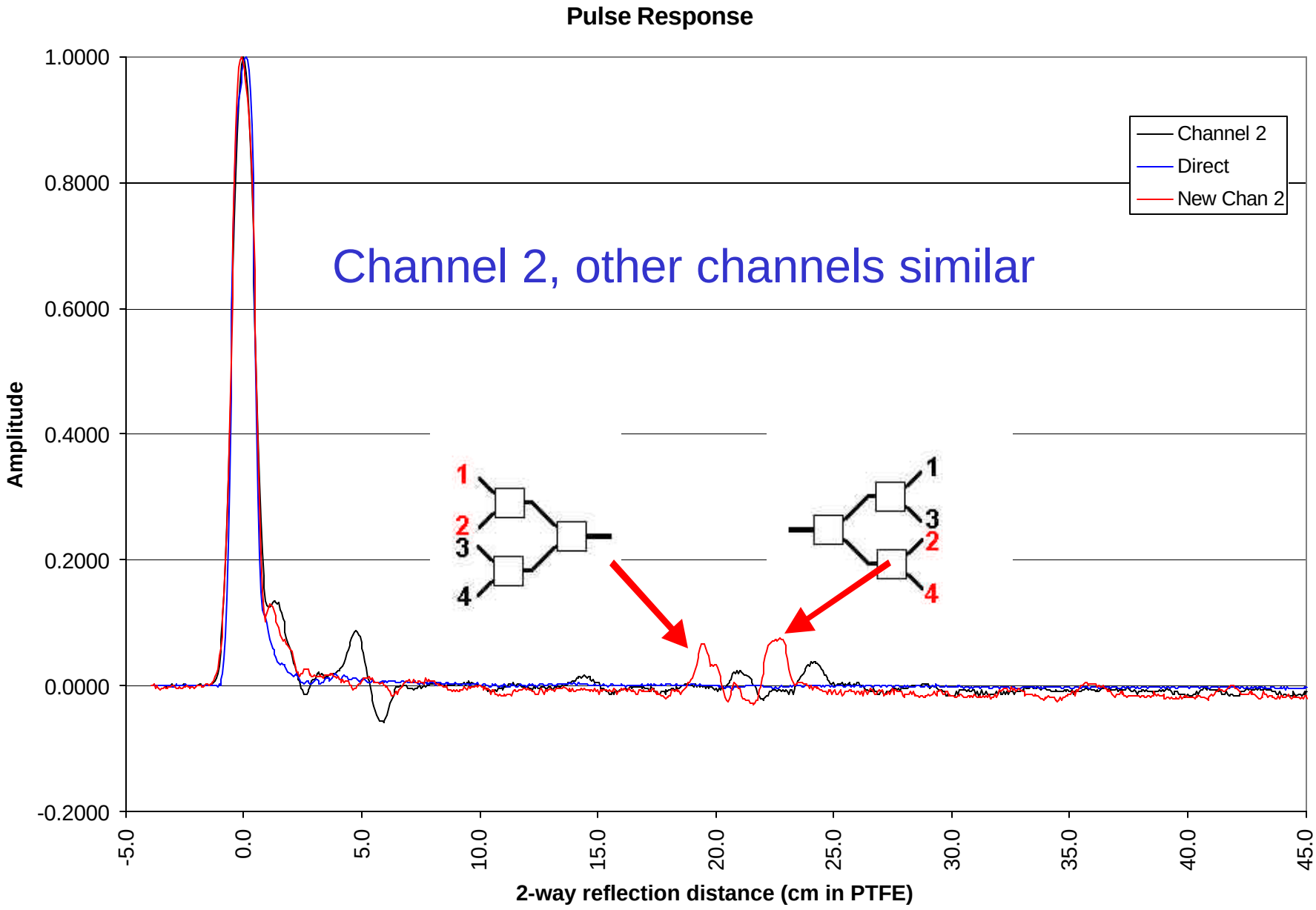
Generating Precursor Pulse by Weighted Addition of Present Measured Tap Responses



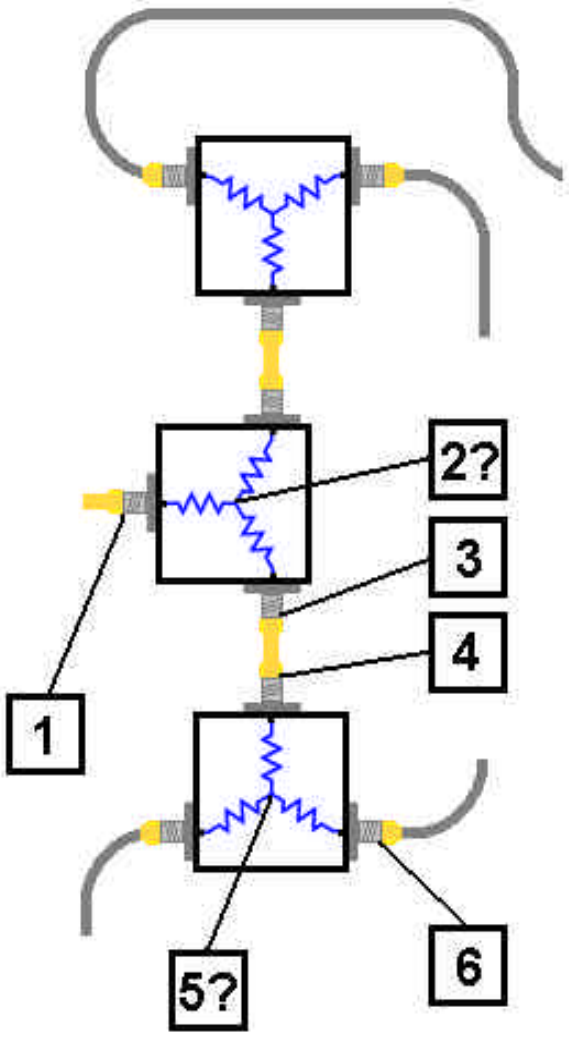
Unwanted Reflections Limit Current System Performance

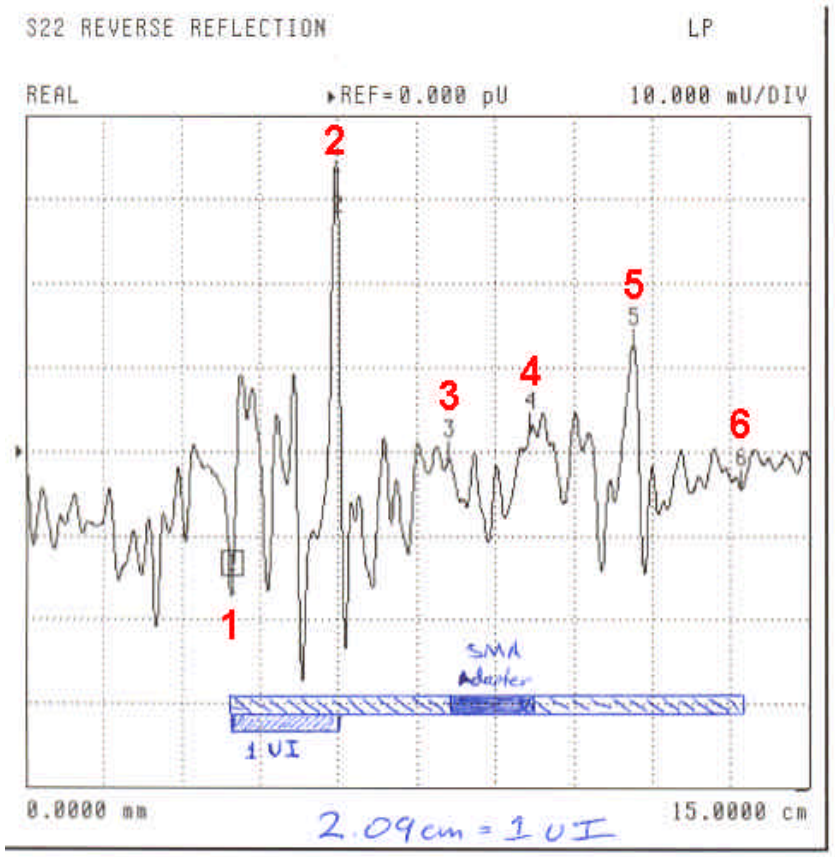
- Very tight control of reflections required
  - Reflections 20 dB down in optical domain require 40 dB return loss (electrical power domain)
  - Requires high quality microwave components
- Main areas of reflections are:
  - Electronic variable attenuator
    - Attempt to control with fixed attenuators, but need enough attenuation and very high quality attenuators
  - Inside and between the power dividers
    - Connectorized, off-the-shelf power dividers are nearly 2 UI long.
    - Have evaluated several different types, and have (hopefully) a workable solution on order

Long Reflections from Attenuator Plane



TDR measurements of Power Dividers Section using 64 GHz Network Analyzer



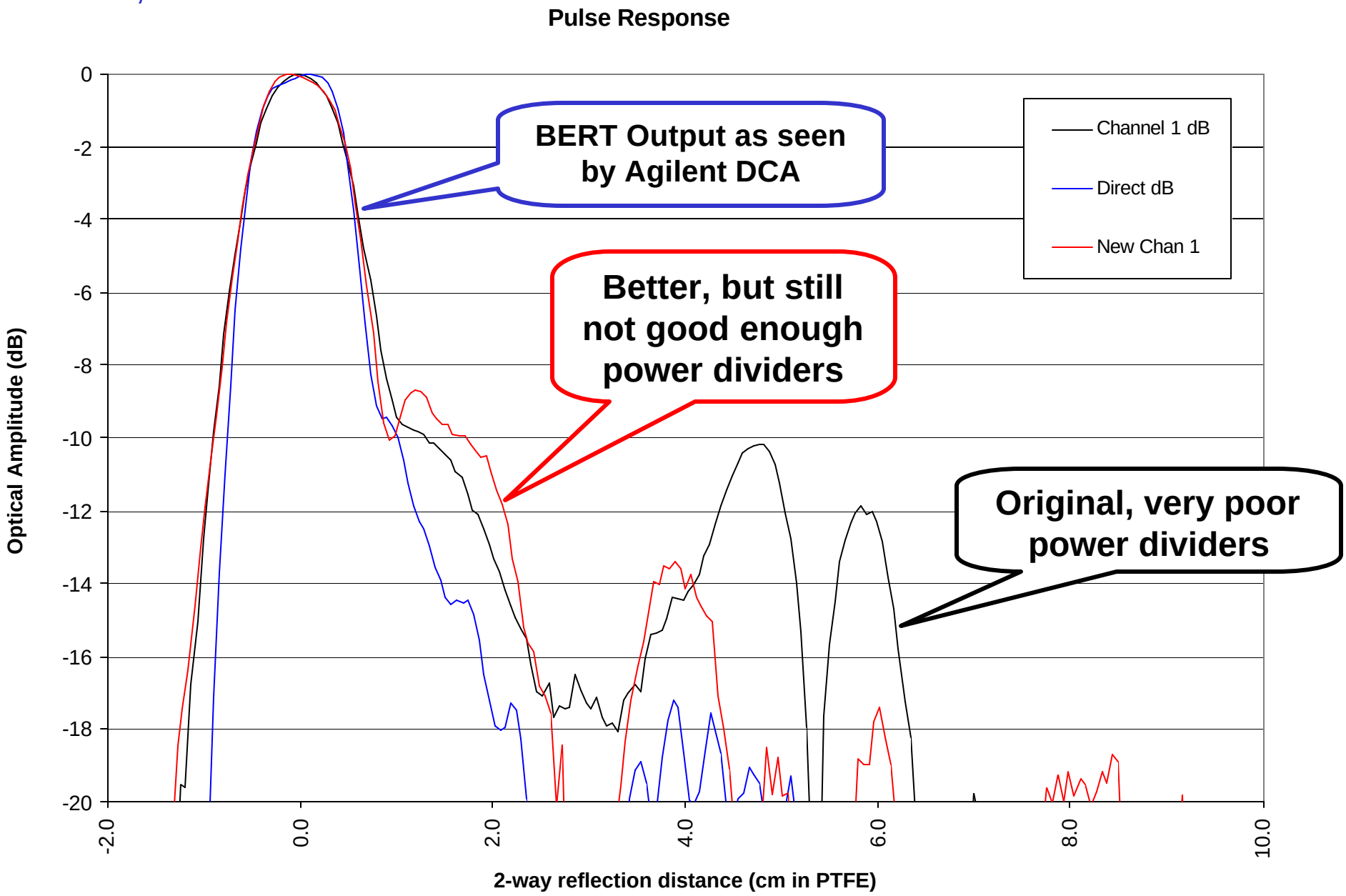


SET MARKERS

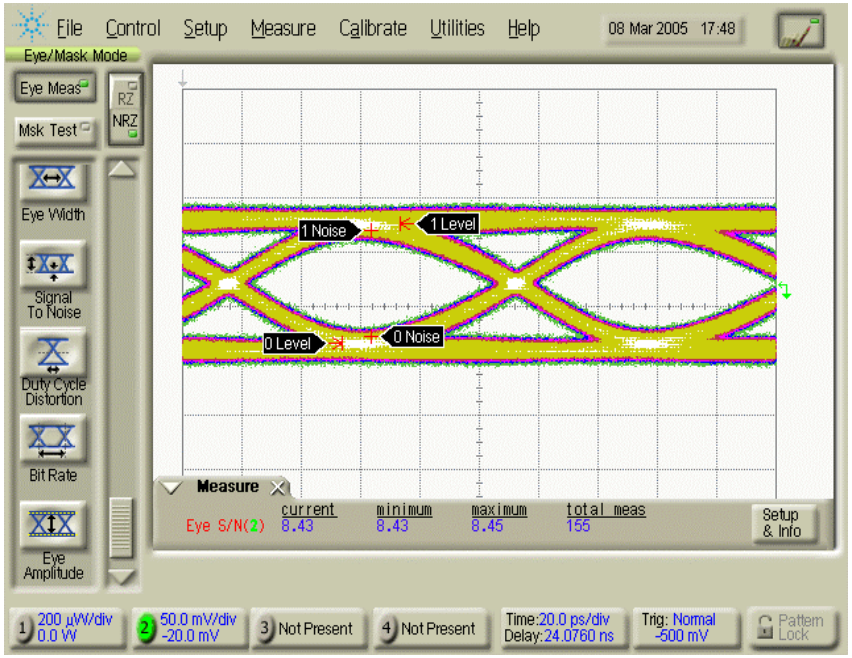
▸MARKER 1 3.9750 cm	ON	-16.99 mU
MARKER 2 5.9906 cm	ON	3339 mU
MARKER 3 8.1094 cm	ON	-1.25 mU
MARKER 4 9.6844 cm	ON	2.24 mU
MARKER 5 11.6438 cm	ON	12.47 mU
MARKER 6 13.6875 cm	ON	-4.24 mU
DISPLAY MARKERS	ON	
ΔREF MODE	OFF	
SELECT ΔREF MARKER		
MARKER READOUT FUNCTIONS		

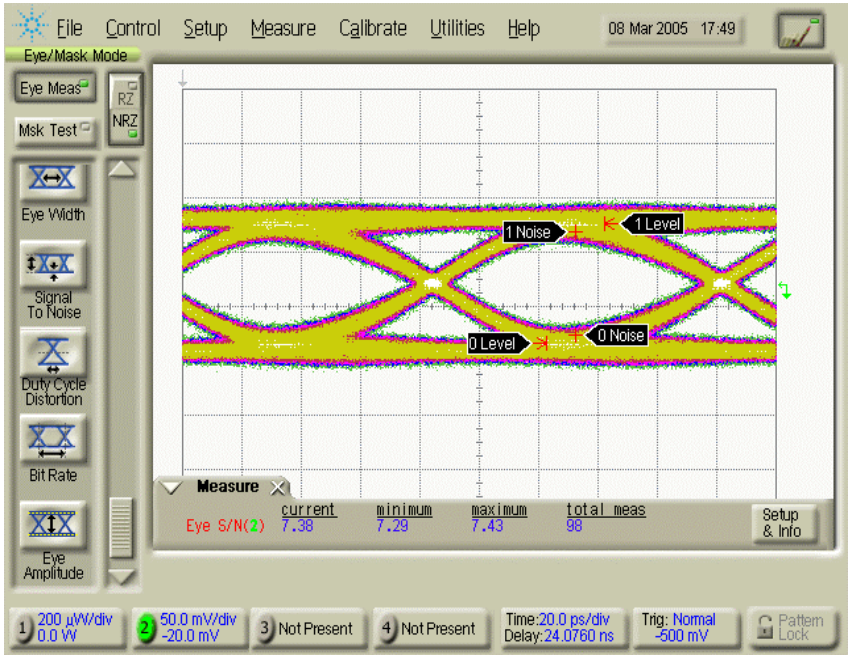
Short Reflections Within Power Divider Network

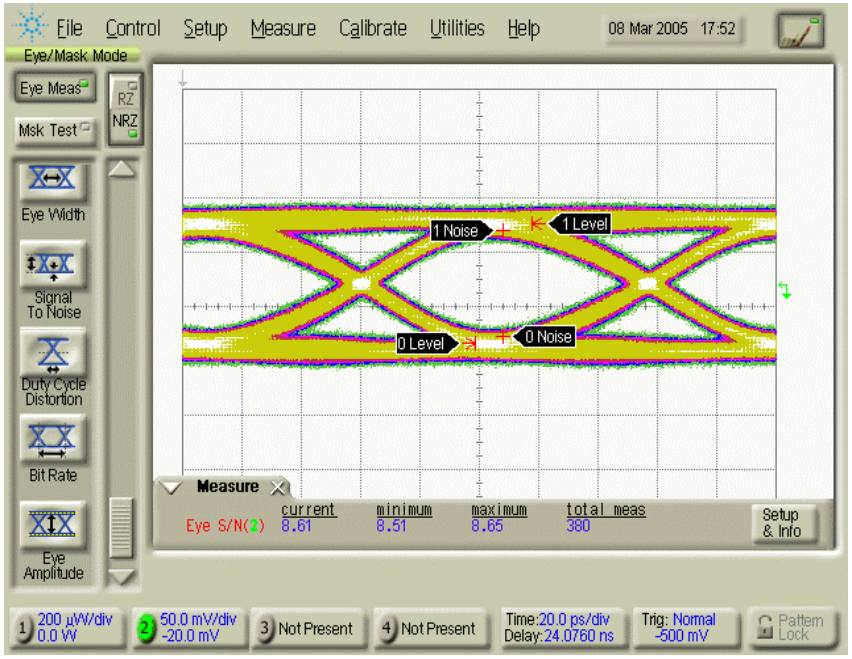
Channel 1, other channels similar

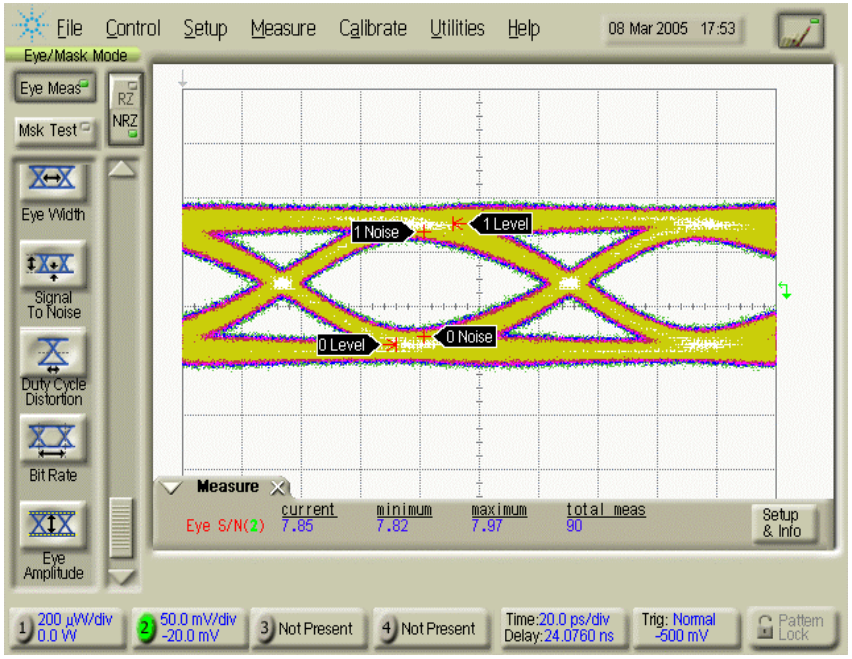


Eye diagrams of individual taps showing deterministic ‘fuzz’ and possibly eye closure due to short and long reflections





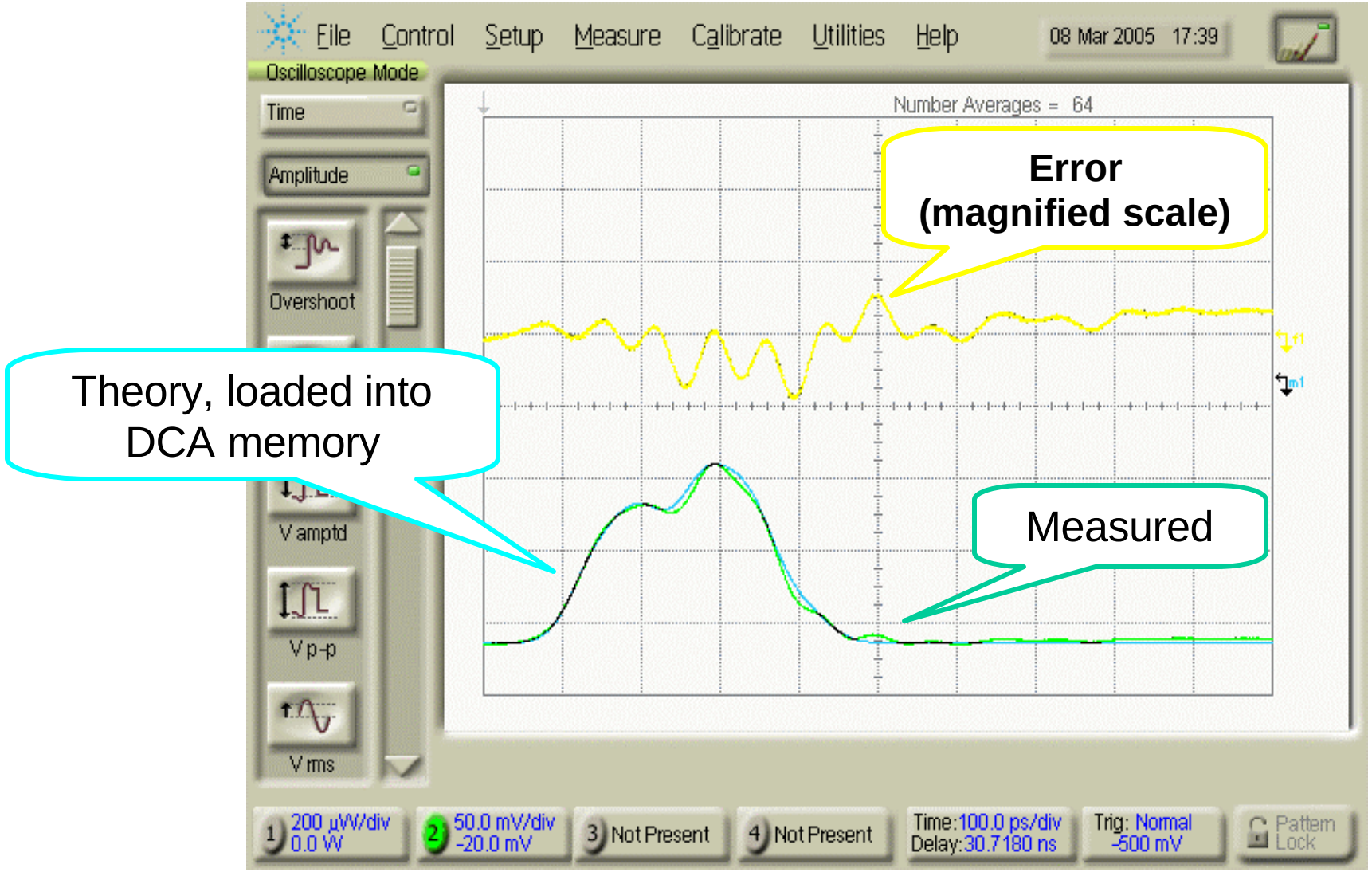




Precursor per 802.3aq D1.1

PSR = 24.3 dB, Target PIE-D = 4.82 dBo, Actual PIE-D = 4.86 dBo

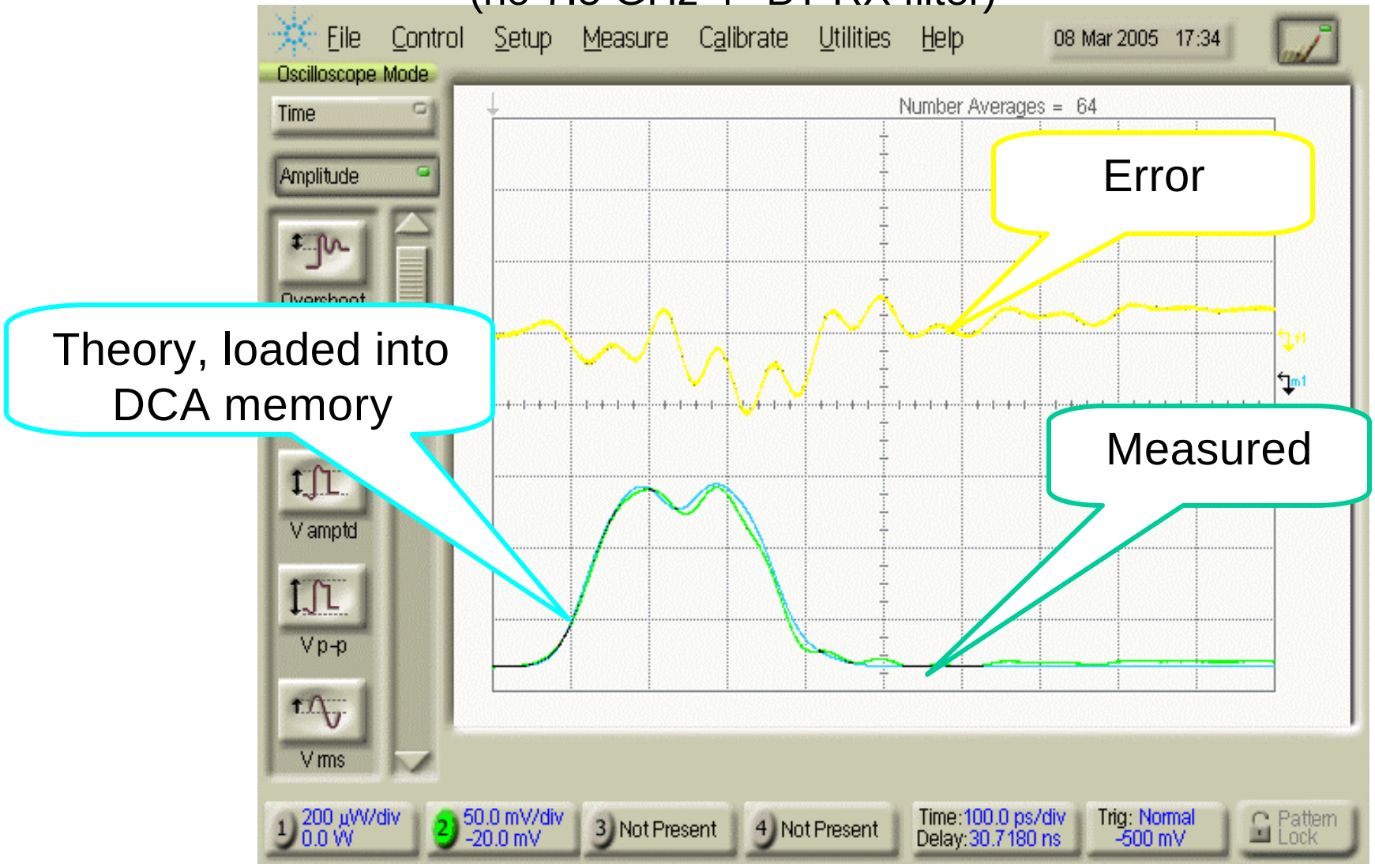
(no 7.5 GHz 4th BT RX filter)



Split-Pulse Symmetric per 802.3aq D1.1

PSR = 24.5 dB. Target PIE-D = 4.54 dBo. Actual PIE-D = 4.58 dBo

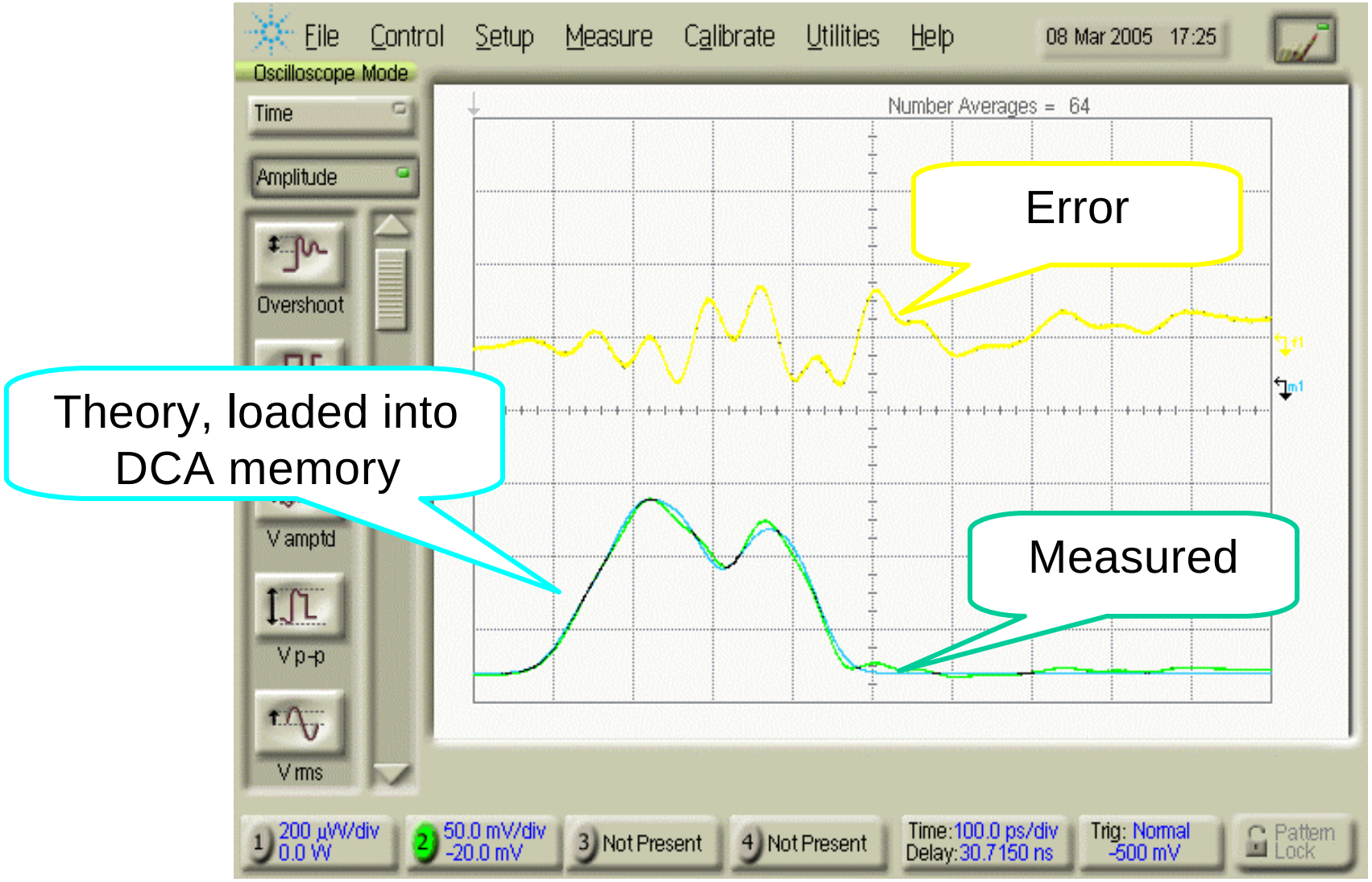
(no 7.5 GHz 4th BT RX filter)



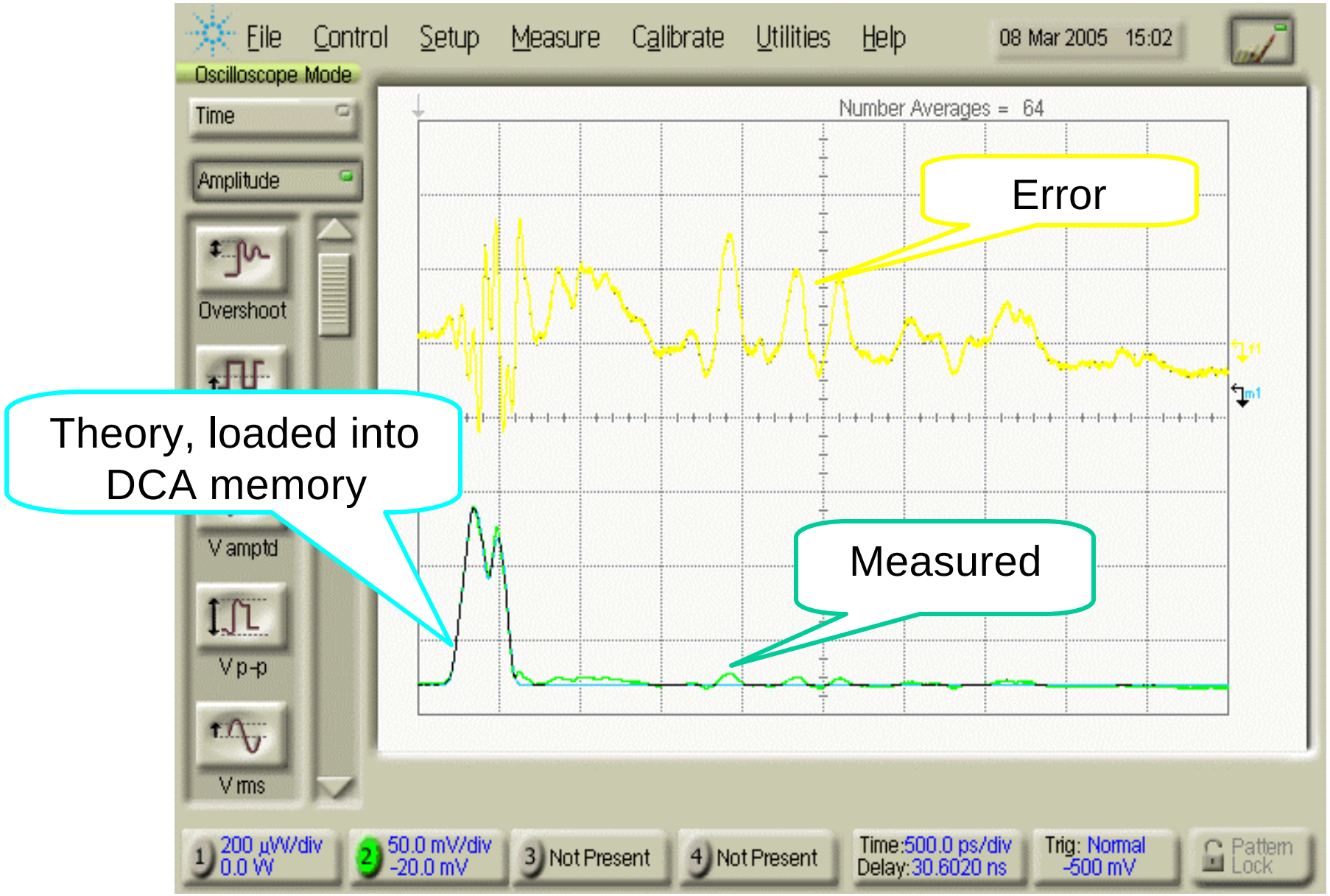
Post cursor per 802.3aq D1.1

PSR = 25.1 dB, Target PIE-D = 4.85 dBo, Actual PIE-D = 4.86 dBo

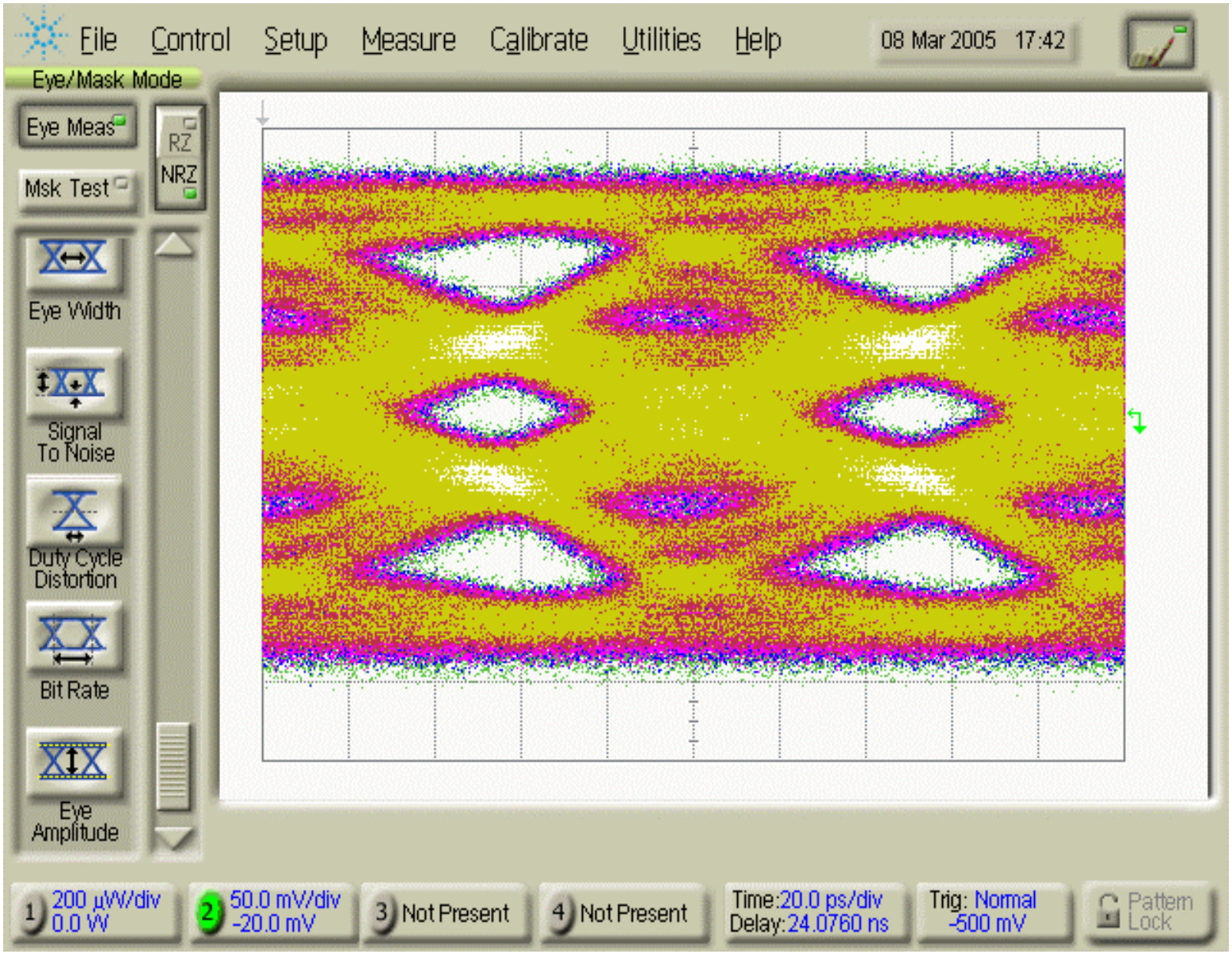
(no 7.5 GHz 4th BT RX filter)



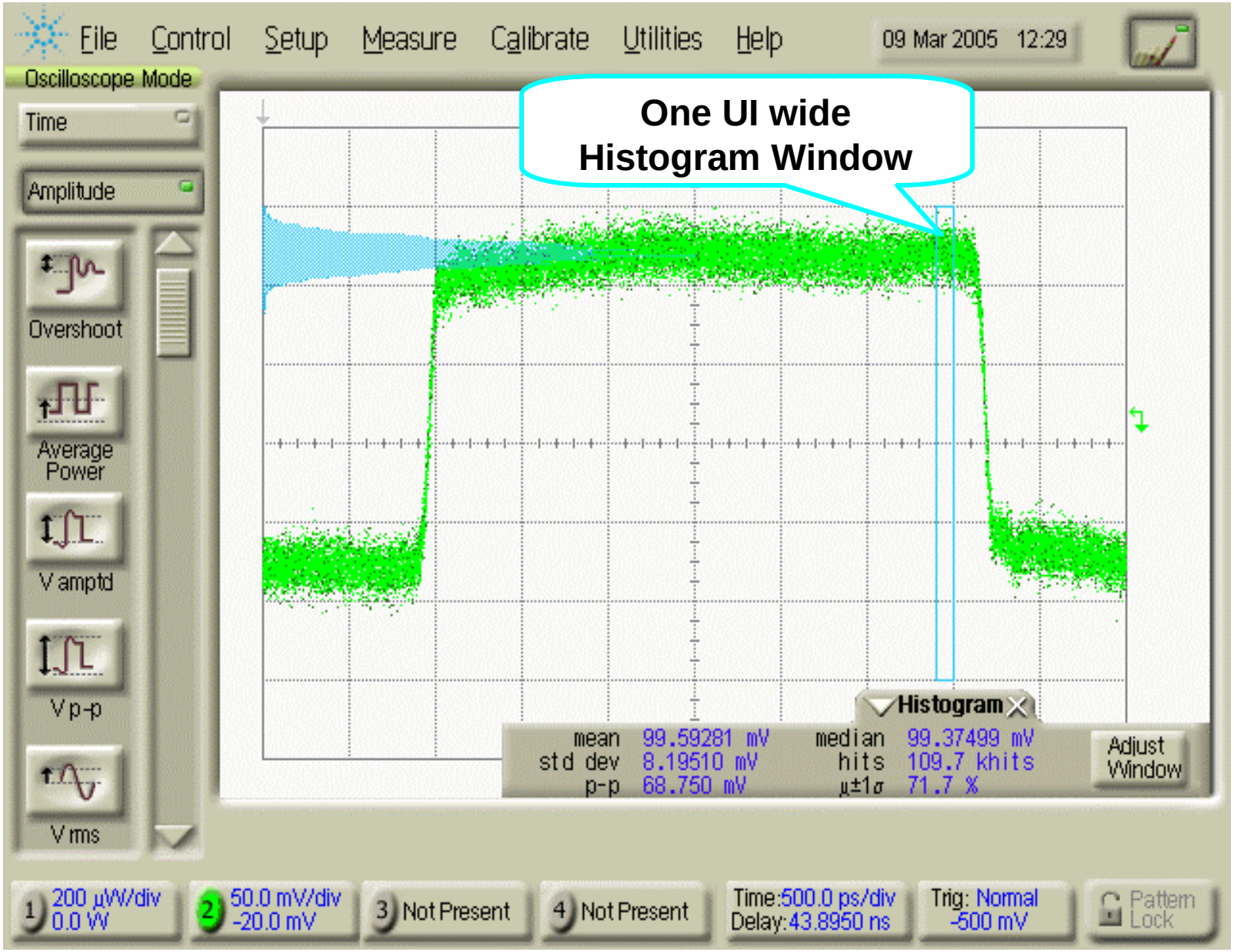
Post cursor, the whole story including long reflections



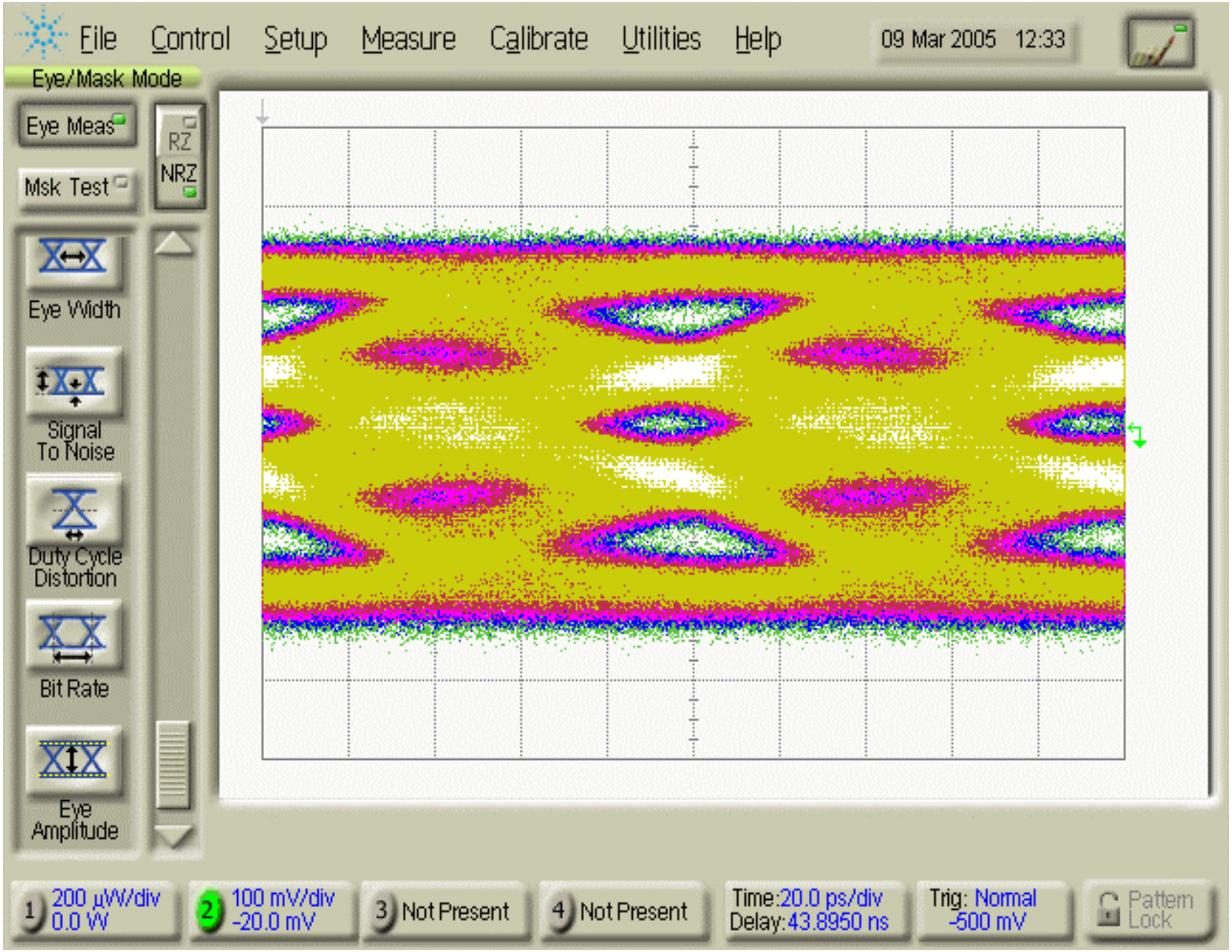
Precursor Eye Diagram , No Source Noise



Calibration of Source Noise Using Histogram and Slow Square Wave

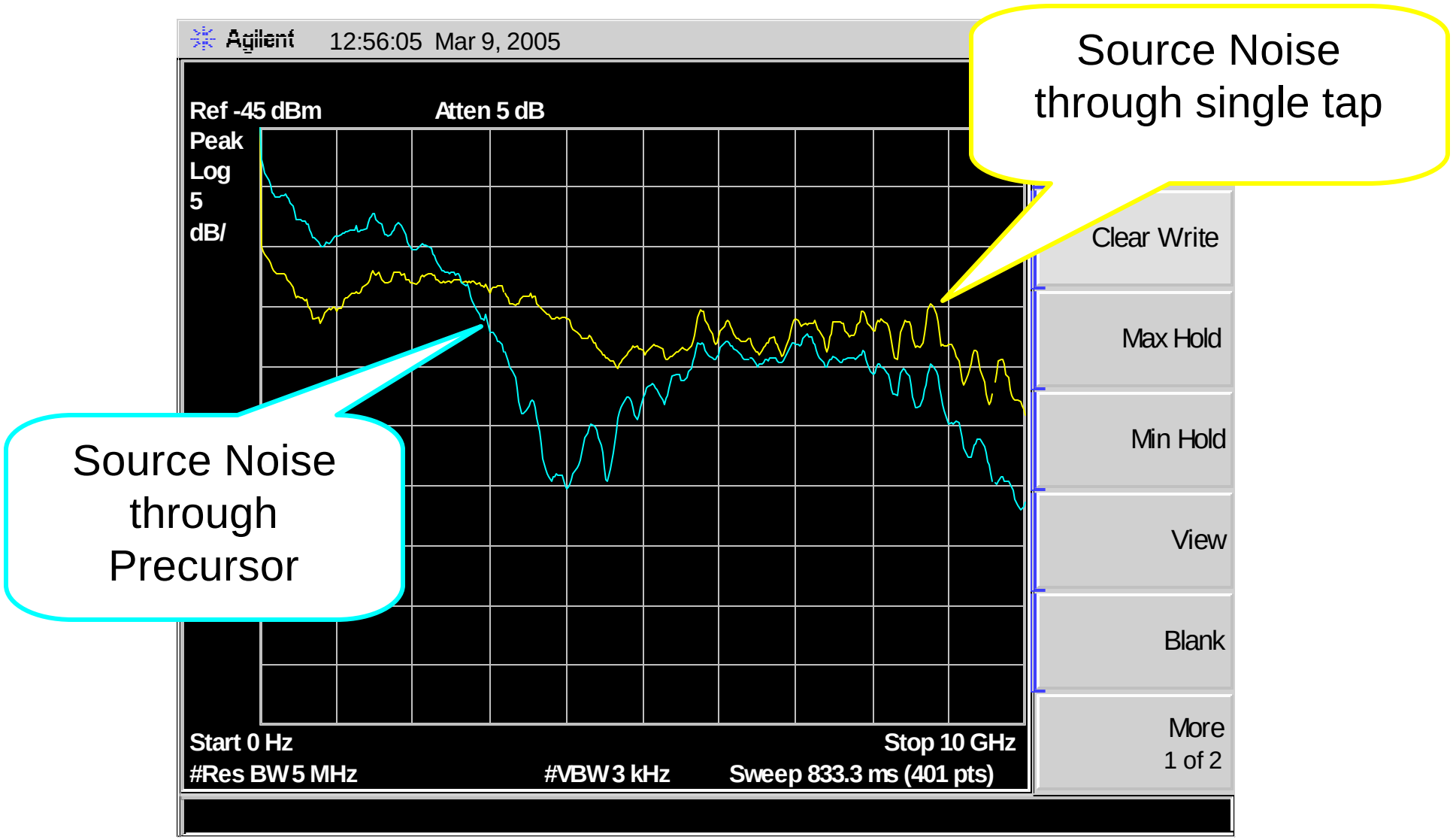


Precursor Eye Diagram with Source Noise



Frequency Domain Measurements

Reduced Bandwidth of emulated channel visible in impact on source noise



Rapid wiggles are caused by long reflections

Further Work

- Reduce Reflections to Acceptable Levels:
  - Make Ripple Induced Eye Closure Small Compared to Noise Loading
  - Ensure Reflections Don't Generate Significant Errors in Impulse Shape
  - Ensure Reflections Do Not Result in Significant Long Delay Features
- Measure Accuracy of Generated Impulse Response
  - Calculate Resulting Error in PIE-D and/or Finite Equalizer Metric
- Add E/O Converter
  - Verify Accurate Impulse Response in Optical Domain, 3.5 dB ER, Desired Noise Loading Amplitude and Frequency Content.

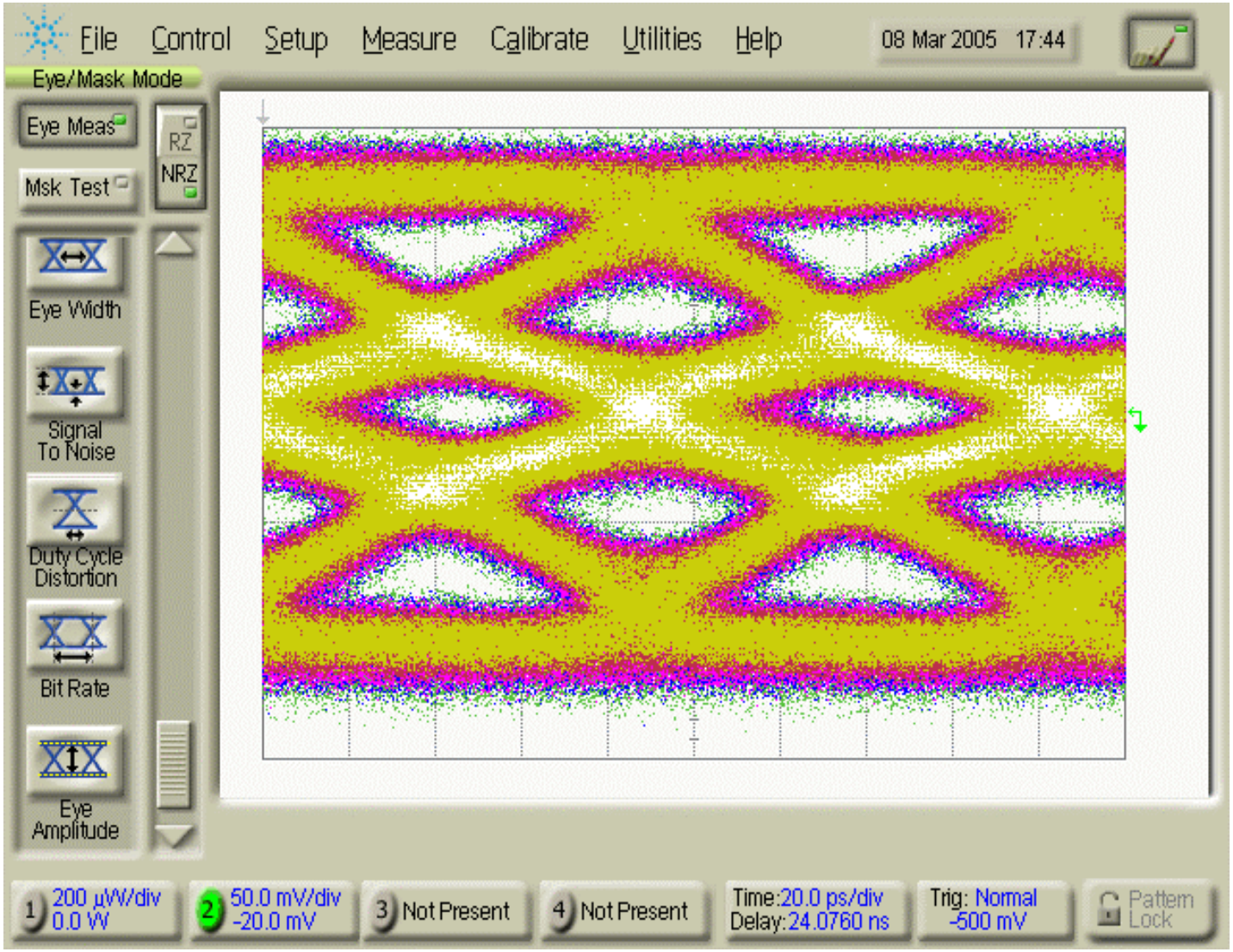
Back Up Material

PIE-D Sensitivity versus tap weights

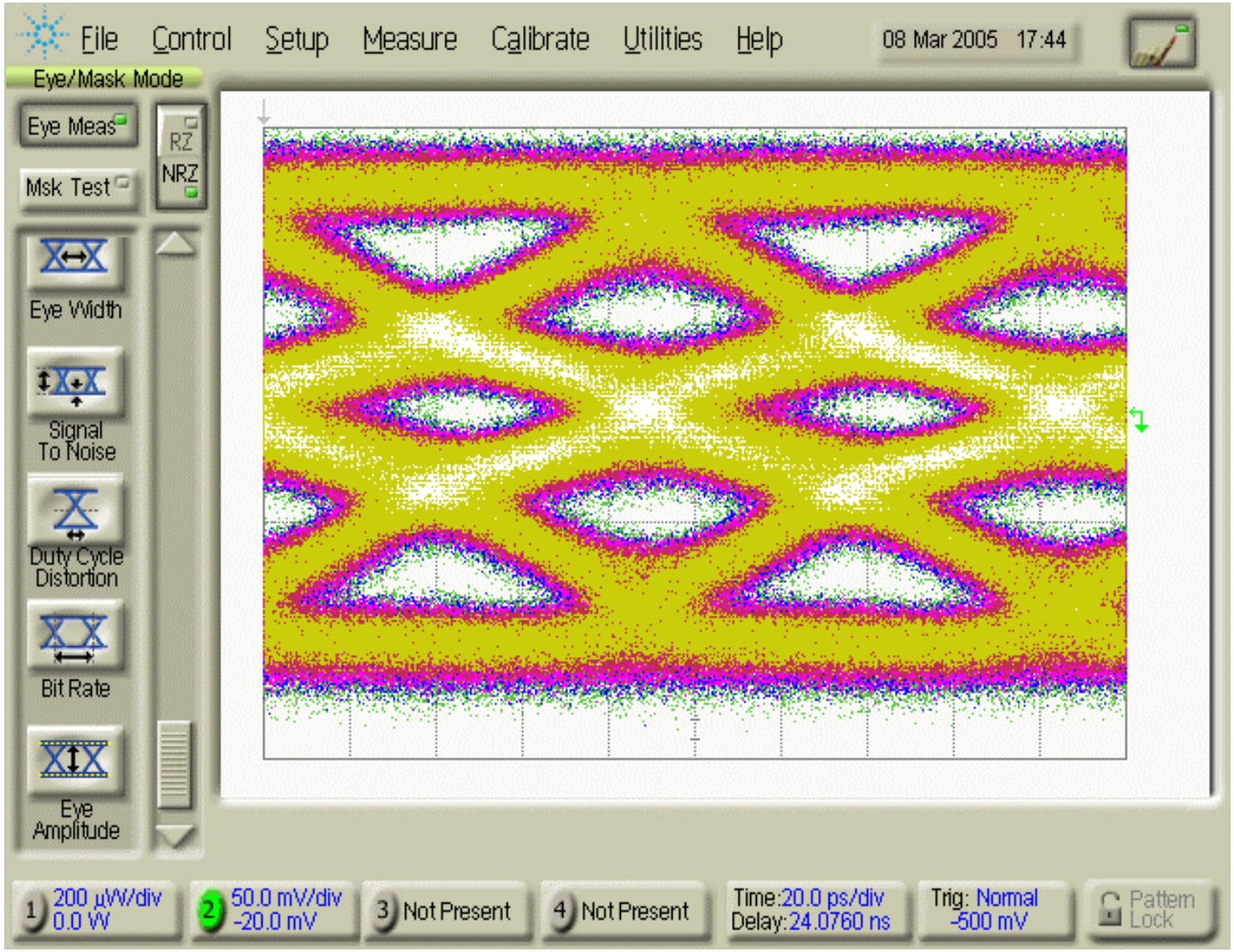
- PIE-D is surprisingly insensitive to errors in the tap weights
  - Analyzed assuming that the taps would be electrical attenuators specified by dB electrical power loss
  - Assume quantization of 0.125 dB, 0.25 dB, 0.5 dB and 1 dB

	D1.1	0.125 dB	0.25 dB	0.5 dB	1 dB
Precursor	5.091	5.102	5.072	5.163	5.095
Symmetric	4.761	4.760	4.753	4.766	4.740
Post Cursor	5.108	5.103	5.112	5.075	5.075

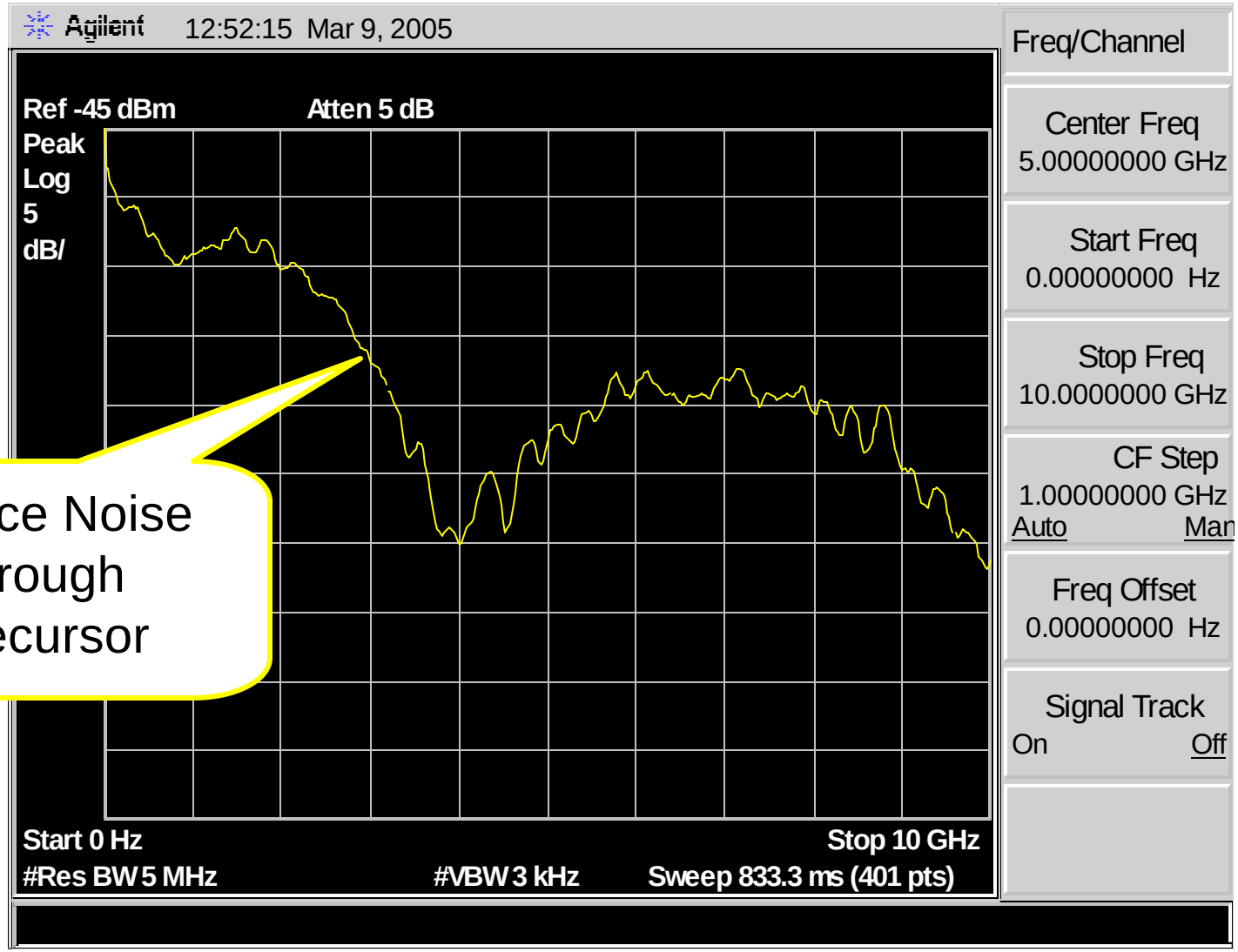
Split-Symmetric Eye Diagram , No Source Noise



Post Cursor Eye Diagram, No Source Noise



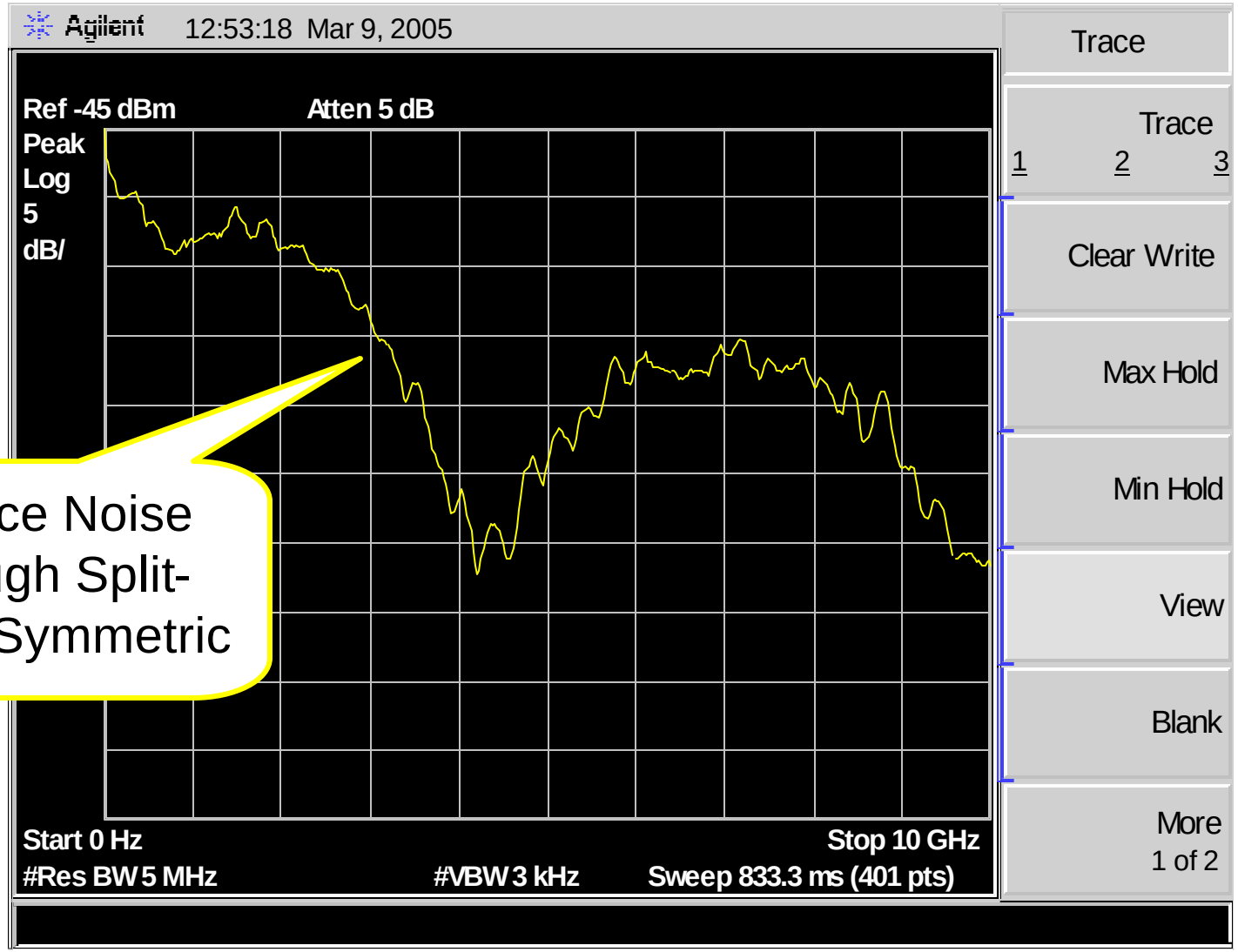
Frequency Domain Measurements



Source Noise through Precursor

Rapid wiggles are caused by long reflections

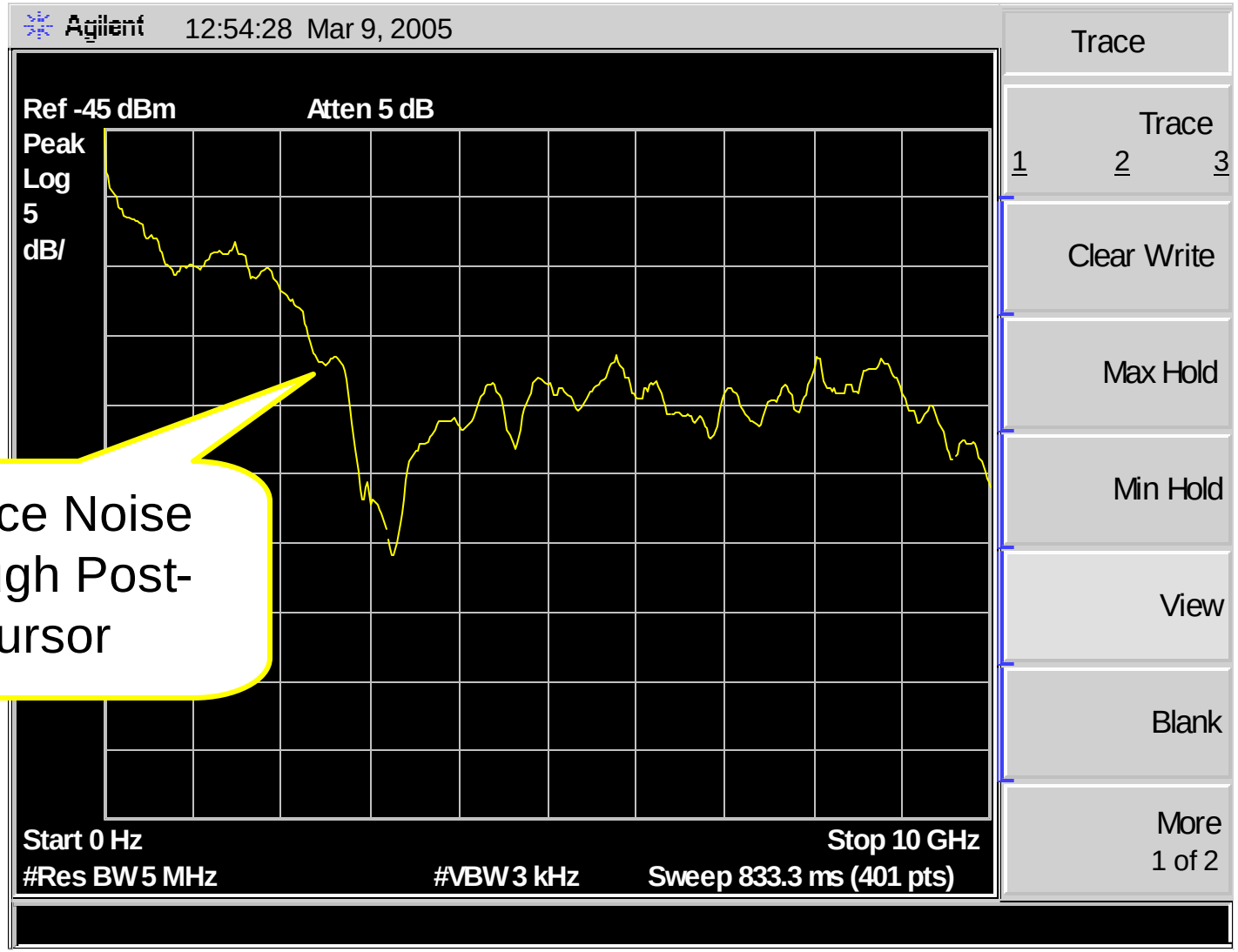
Frequency Domain Measurements



Source Noise through Split-Pulse Symmetric

Rapid wiggles are caused by long reflections

Frequency Domain Measurements

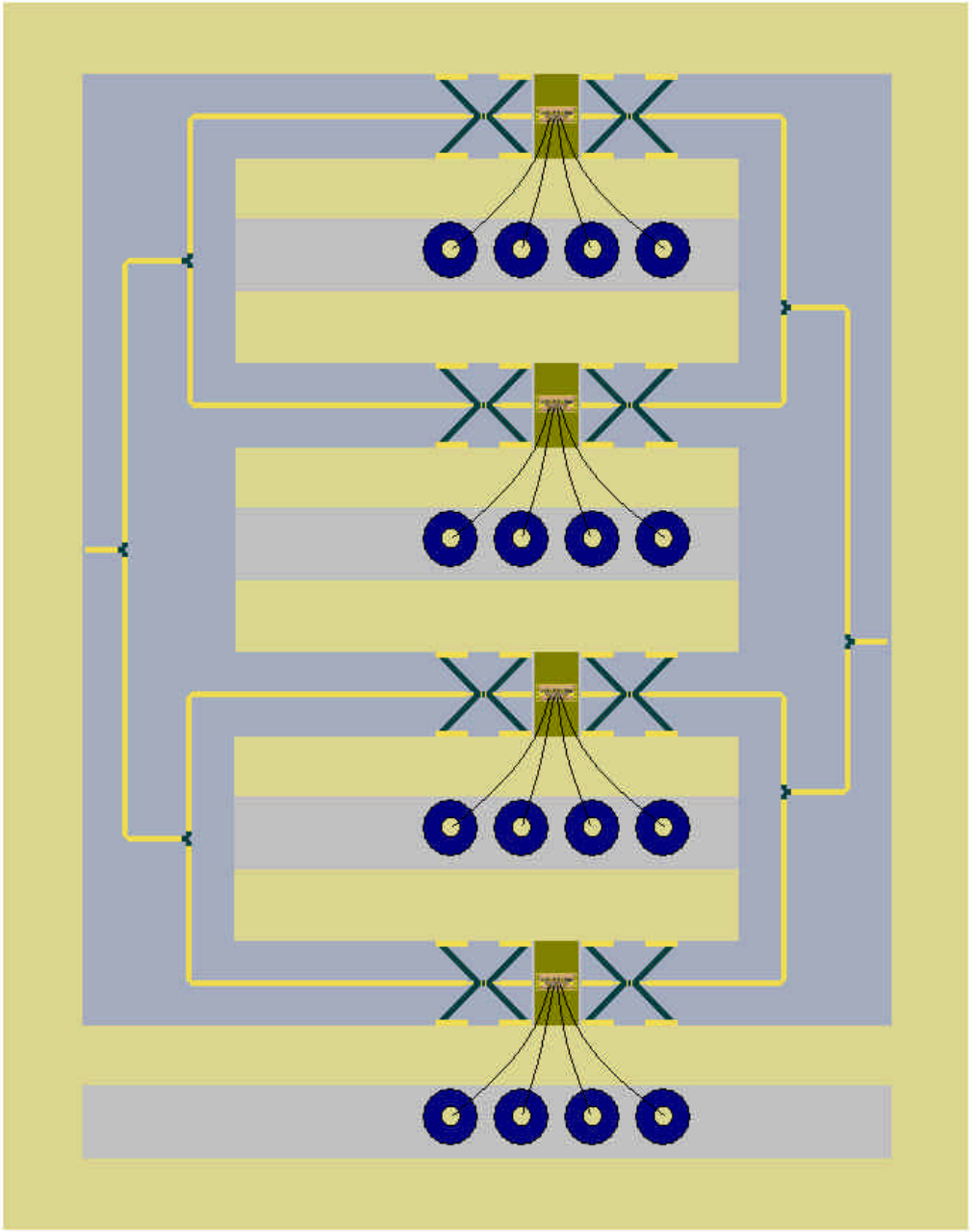


Source Noise through Post-cursor

Rapid wiggles are caused by long reflections

Other possible implementations considered:
Microcircuit

- Agilent HMMC-1002 DC to 50 GHz GaAs attenuator
- Thin film substrate (sapphire or polished alumina)
- Needs PCB with DAC's to control attenuators
- Biggest risk is design of resistive elements (power dividers and pads)
- Still difficult to control magnitude of reflections, and although reflections length is reduced, it is still well beyond 1UI



Other possible implementations considered:
Microcircuit with tapped delay line structure rather than power divider tree