## Report from TP3 Conference Calls

November 8th 2004

#### **TP3 Regular Participants:**

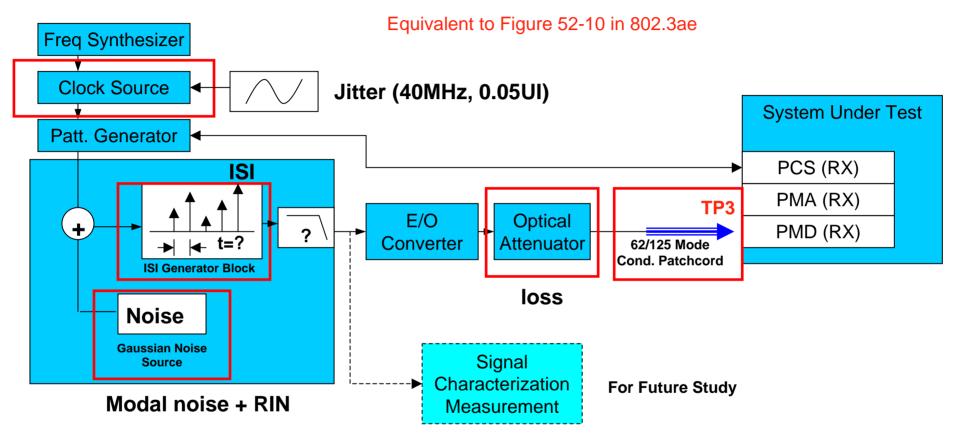
Lew Aronson
Piers Dawe
John Jaeger
Tom Lindsay
Jan Peters Weem
Vivek Telang
Kevin Witt

Venu Balasubramonian John Ewen Ryan Latchman Rob Lingle Petre Popescu Andre Van Schyndel Sudeep Bhoja Jesper Hanberg Mike Lawton Jim McVey Abhijit Shanbhag Nick Weiner

## **Report from Conference Calls on TP3 Specification**

- Summary diagram for current test
- TP2 and the Link Budget
- Jitter testing
- OSNR calculations
- Conclusions and Further Work

### **Latest Stressed Receiver Sensitivity Test Proposal**

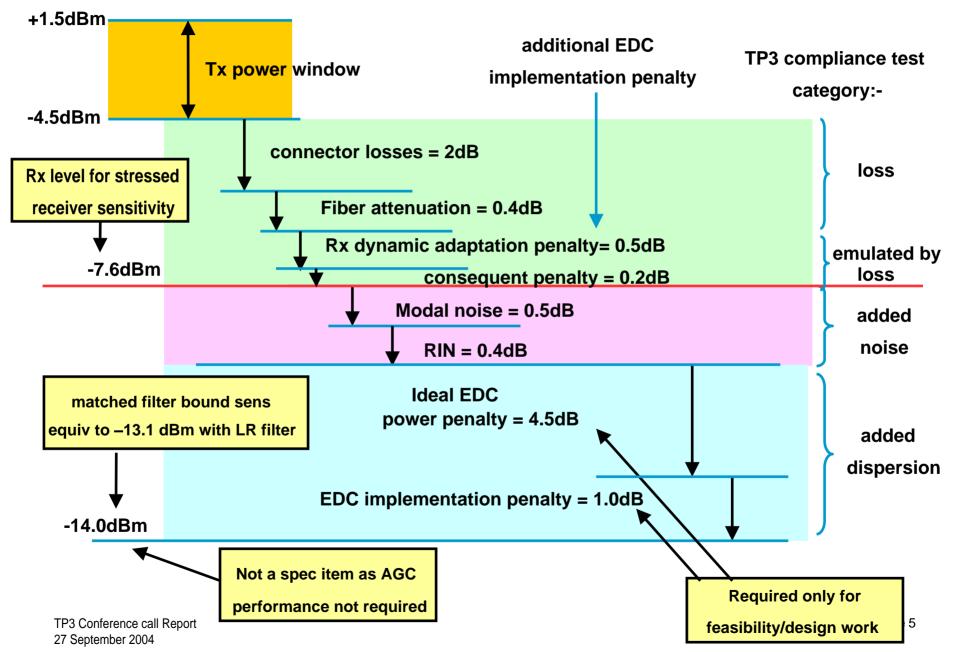


- Leverages strongly off 10GBASE-LR
- Motivated to keep it simple whilst still represent all the key stressors
- Motivated to have practical test with reproducible results

# TP2 and the Link Budget presentation from Tom Lindsay

- The group agreed the following:-
  - TP2 and TP3 testing should both be test configurations which seek to represent the relevant aspects within the link budget
- We have a link budget from the Oregon meeting.
  - http://grouper.ieee.org/groups/802/3/aq/public/jul04/lawton\_1\_0704.pdf
- The group is working with the following assumptions:-
  - connector losses can be reduced from 2.0 to 1.5dB
- The following still needs to be done:-
  - Establish figures for Modal noise and RIN
  - Determine the need for an Adaptation penalty ... and location above or below "waterline"
  - Agree on consequent penalty ... and location above or below "waterline"
  - Determine appropriate representation of equaliser power penalty and associated implementation losses

## Interpreting the EDC Link Budget (OMA)



# "Jitter Tolerance for Receiver Stressed Sensitivity Test" presentation from Petre Popescu

Channel Model Ad-hoc, TP3 - Jitter Tolerance for Receiver Stressed Sensitivity Test

10/26/04

#### 3. Jitter Sources and Impact on the Receiver Test

Jitter Source	Jitter Characteristics	Receiver impact	10GBASE-LRM Receiver
Transmitter clock, random jitter	High peak-to-peak ampli- tudes at low frequencies	The recovered clock will track the incoming jitter	Needed EDC will not correct
Laser random jitter	Small peak-to-peak ampli- tudes at low frequencies, uniform distribution at high-frequency	The recovered clock will not track the high-fre- quency incoming jitter	Needed EDC will not correct
Transmitter, pattern (data) dependent jit- ter (correlated)	Transmitter bandwidth limitation and phase non-linearities (ISI), high frequency components, (above 10 LB*)	The recovered clock will not track the high-fre- quency incoming jitter	Negligible com- pared with the chan- nel contribution. Partially reduced by EDC.
Channel jitter contri- bution	Small for SMF, not generated in the "stress conditioning", for 10GBASE-L.	Equalizer required for MMF.	Not needed. Jitter generation is included in the "non-quasi-symmetrical stressed signal generator".

<sup>\*</sup>LB - PLL loop bandwidth.

#### **Jitter Testing choices ...**

- 1. Define mask and leave it to the implementer to determine appropriate testing
- 2. Define mask and advise a single frequency for stressed receiver testing.
- 3. Use of a PRBS to simultaneously modulate the Tx source with broadband jitter
- Group agreed to define a test in line with option 2:-
  - 40MHz, 0.05UI source for stressed receiver normative test
  - include a separate low frequency test, 40kHz 5UI

## OSNR Calculations (Contributions from Lew Aronson and Nick Weiner)

- The purpose of the work is to establish the OSNR required at the Rx given that both Modal noise and RIN are represented by additional noise power penalties
- Calculation carried out with 2 techniques:-
  - Lew Aronson for non-equalising case without ISI
  - Nick Weiner for a channel with ISI and a perfect equaliser
- Both techniques were in close agreement and yielded a figure of 11dBo for Modal noise and RIN power penalties totaling 0.9dB
- Also agreed to measure S/N with the ISI OFF:-
  - consistent with TP2
  - avoids issues with different channels having different "gains"

## **Conclusions and Further Work**

- Key Progress since last meeting:-
  - Agreed parameters for jitter testing
  - Determined approach for representing power penalties with reduced OSNR
- Further Work items:-
  - Select appropriate channels for compliance testing
  - Determine methodology for measuring OMA
  - Work with TP2 to refine link budget (primarily above the "waterline")
    - Determine what is above and below the line
  - Finalize simplified normative test
  - Build and validate test