A pathway to Asymmetric EEE GPHY

March 2008
IEEE 802.3az Task Force

Presenter: Joseph Chou

Realtek Semiconductor Corp.

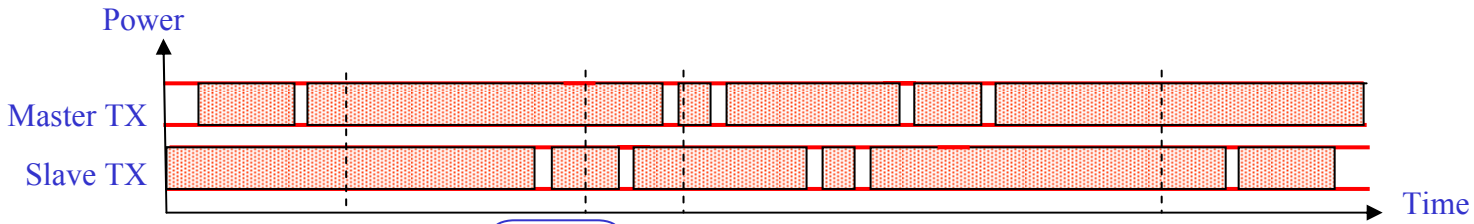
Contributors: Albert Kuo, Leon Lin, Jerome Yu

Outlines

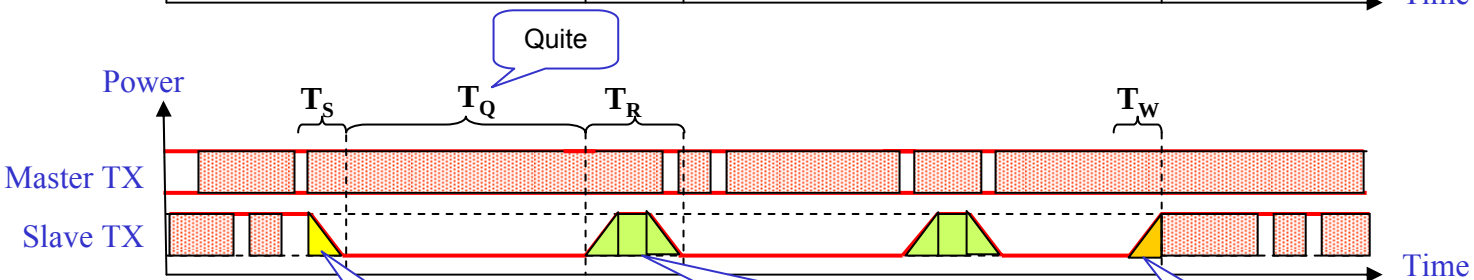
- Line States of Asymmetric EEE GPHY
- Concerns of Asymmetric EEE GPHY
- Effects of TR Clock Phase Offset
  - Case 2 is not an issue at all
  - Case 4 is a necessary evil
  - Case 3 is troublesome with trade-off
- How to determine the Quite Duration
- GPHY Symmetric only Operation
- GPHY Partially Asymmetric Operations
- GPHY Fully Asymmetric Operations
- Summary

Line States of Asymmetric EEE GPHY

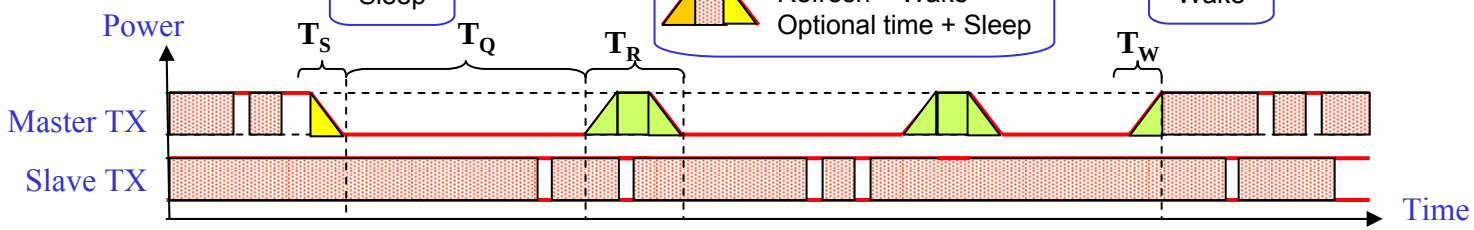
Case 1. Symmetrical; Both Master & Slave Active



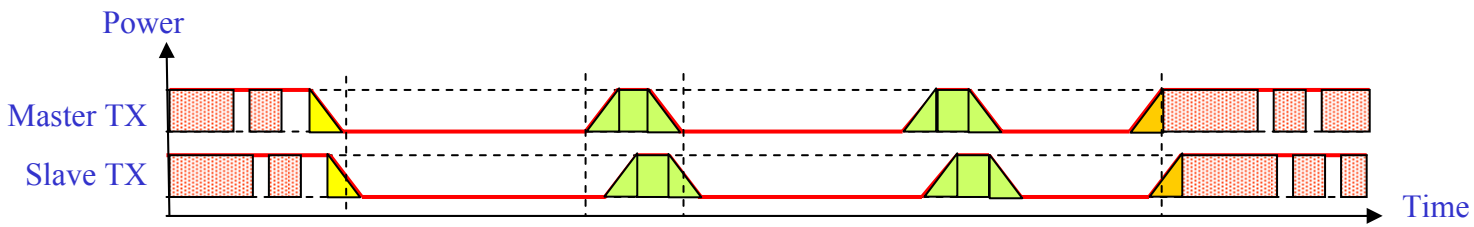
Case 2. Asymmetrical; Master Active, Slave Low-Power
- Slave sends Refresh freely with Tq= Tq-max



Case 3. Asymmetrical; Master Low-Power, Slave Active
- Master sends Refresh with shorter Tq≤Tq-max



Case 4. Symmetrical; Both Master & Slave Low-Power
- Master initiate Refresh
- Slave sends Refresh tracking Master Refresh



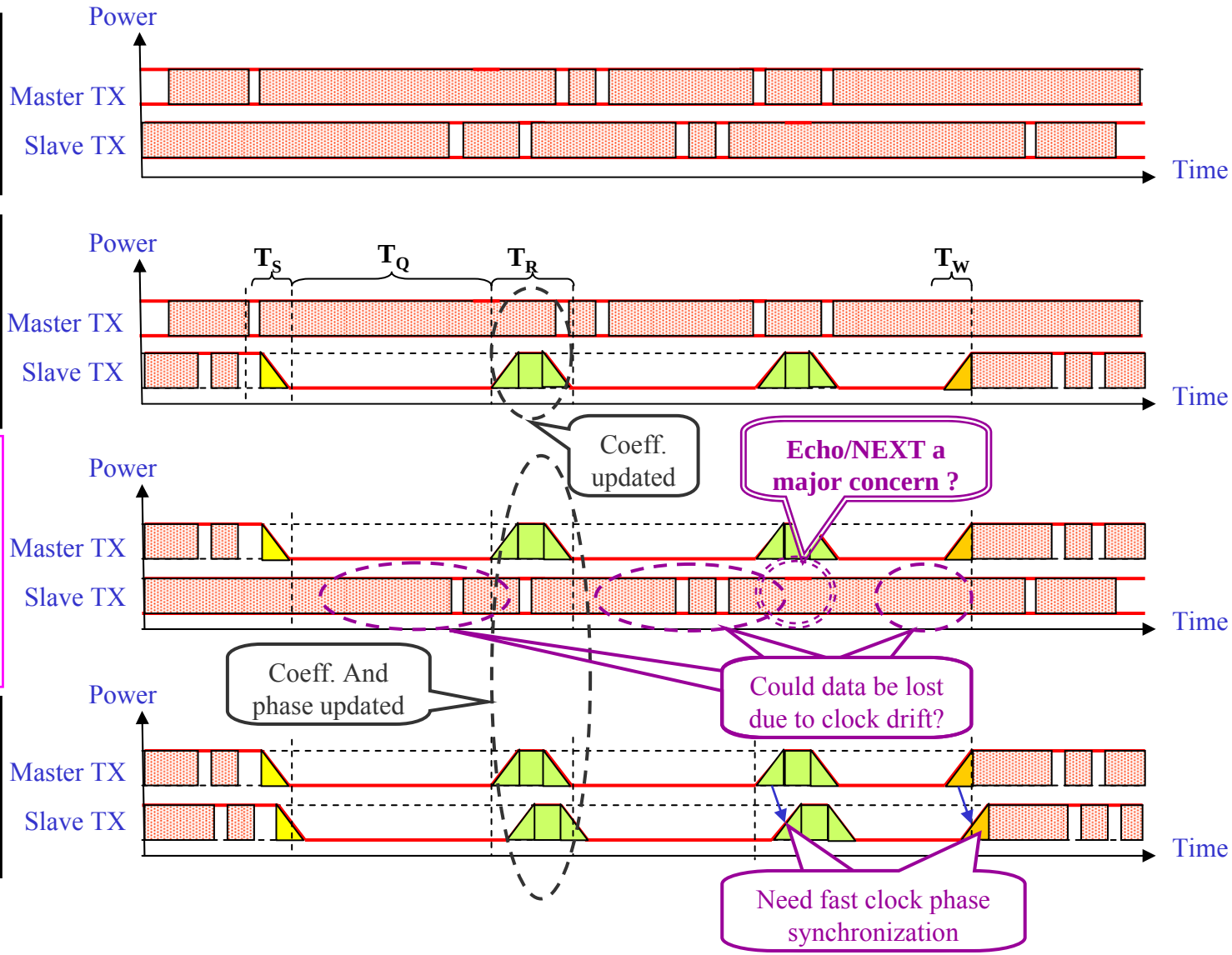
Concerns of Asymmetric EEE GPHY

1. Symmetrical; Both Master & Slave active
- Clock phase tracked
- No data missed
- Coefficients updated

2. Asymmetrical; Master Active, Slave LPI
- Clock phase tracked
- No data missed
- Coefficients updated

3. Asymmetrical; Master LPI, Slave Active
- Clock phase tracked ?
- Data could be damaged or lost due to echo/next
- Coefficients updated

4. Symmetrical; Both Master & Slave LPI
- Clock phase tracked ?
- Don't care lost Data
- Coefficients updated

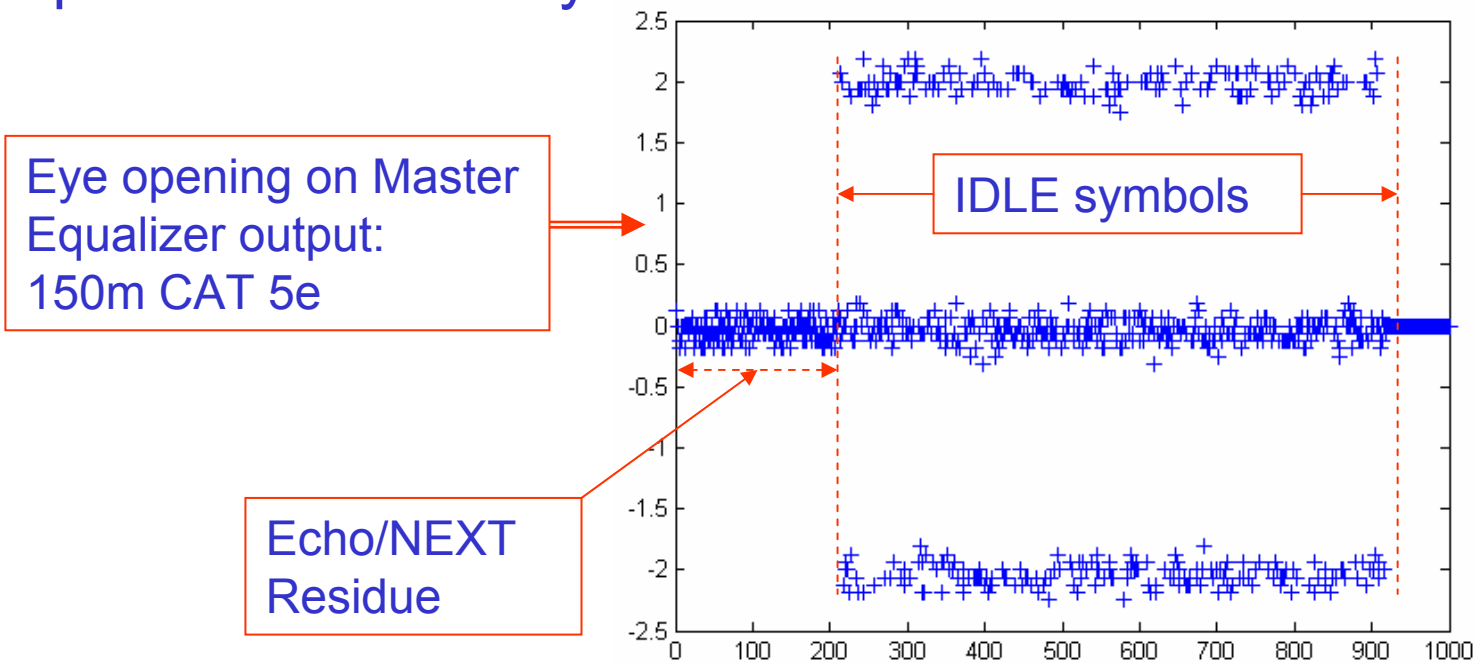


Effects of TR Clock Phase Offset

- Clock Frequency and Phase needs fast Re-synchronization.
  - Slave clock frequency depends on the continuous incoming Master traffic. (Loop-timing).
  - May drift away on Case 3 & 4 when Master ceases transmission.
  - The offset of clock phase depends on
    - The resolution of frequency value held on Slave DPLL.
    - The Phase noise of Master TX PLL.
    - The duration of Quite state (Tq).
- Echo/ NEXT Cancellation Residue may Blow out (Case 3)
  - If the Master TX clock phase is different from the Master RX clock phase when Master RX is tracking drifted Slave Clock.
  - Can be avoided if the Master RX clock phase is frozen during the absence of TX traffic until the Refresh signal kicks in.
- RX Equalizer (FFE/FBE) may not be optimized (Case 3)
  - If the Master RX clock phase is frozen during the absence of TX traffic.
  - Can be avoided if Master RX is tracking Slave traffic all the time.

Case 2 is not an issue at all

- The Slave PHY always tracks the Master Clock phase through incoming traffic. (loop timing)
  - The Echo/NEXT of Slave Refresh is fully cancelled
- The Master PHY can receive Slave Refresh with eye opened immediately.



Case 4 is a necessary evil

- A minimum supported feature of LPI GPHY
- If Quite Duration (Tq) is short enough, then
  - The eye is still open when Master Refresh hits Slave PHY.
  - The Slave tracks Master clock quickly and echoes Refresh.
- Otherwise
  - The Eye is severely blurred or closed.
  - Timing Recovery loop of Slave RX needs start from scratch.
  - An implementation dependent fast synchronization of clock may be needed to shorten the time of Refresh and Wake.
- On either case, the Echo/NEXT ceof. are all frozen until clock phase is realigned.
- The Quite Duration (Tq) and Refresh Duration (Tr) are correlated.

Case 3 is troublesome with trade-off

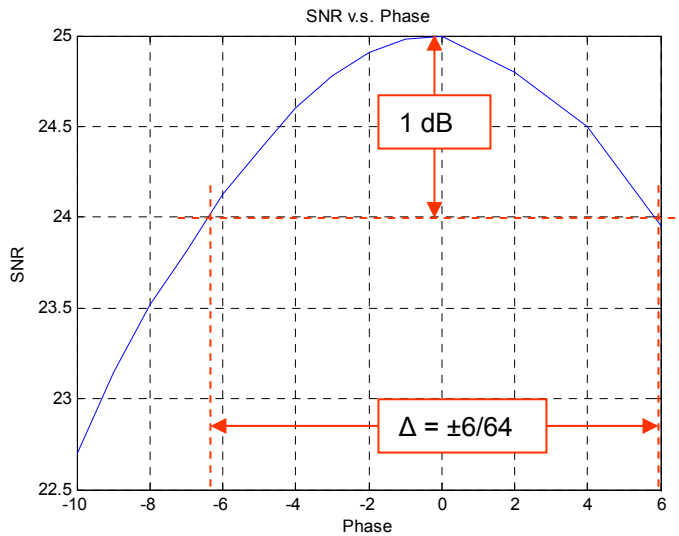
- Both FFE/FBE and Echo/NEXT of a certain set of coefficients work well on the best sampling phase and decrease SNR quickly on phase drift.
- The clock phase and frequency of slave PHY will drift anyway during the quite time of master PHY.
- Trade-off does exist by choosing the clock recovery strategy of Master RX :
  - Recovered clock tracks slave traffic if SNR is more sensitive to the offset of optimal clock phase of Equalizer.
  - Recovered clock is frozen until the Refresh signal starts if SNR is more sensitive to the offset of optimal clock phase of Echo/NEXT cancellers. (**See traeber_01_0308.pdf**)
- The Quite Duration (Tr) is determined by the drift speed of clock phase between Master and Slave PHYs.

How to determine the Quite Duration

- Leverage the Formula from **traeber_01_0308.pdf**

$$T_q = 1e6 * \frac{\Delta\varphi_{acc}}{\Delta F[ppm]}$$

- Find the proper value of $\Delta\Phi_{acc}$ and ΔF[ppm]
  - $\Delta\Phi_{acc}$ (=UI*Δ) depends on the SNR sensitivity to **Master** clock phase.
  - ΔF[ppm] depends on the resolution of frequency value holder of **Slave** DPLL.
  - An example: UI=8ns, Δ=0.2, ΔF[ppm] =8(ppm), => Tq = 200us

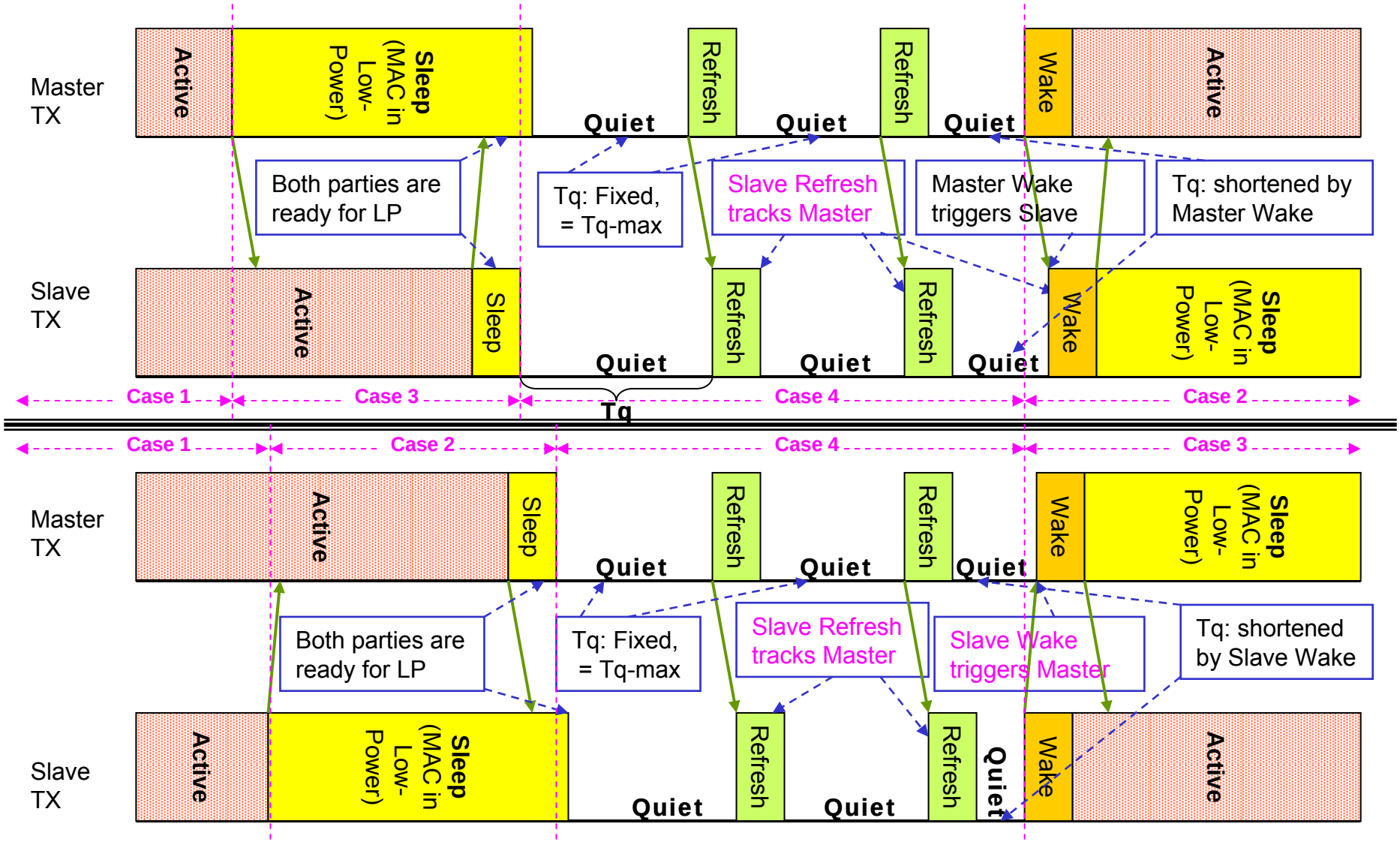


Master RX clock phase tracks Slave and drifts.

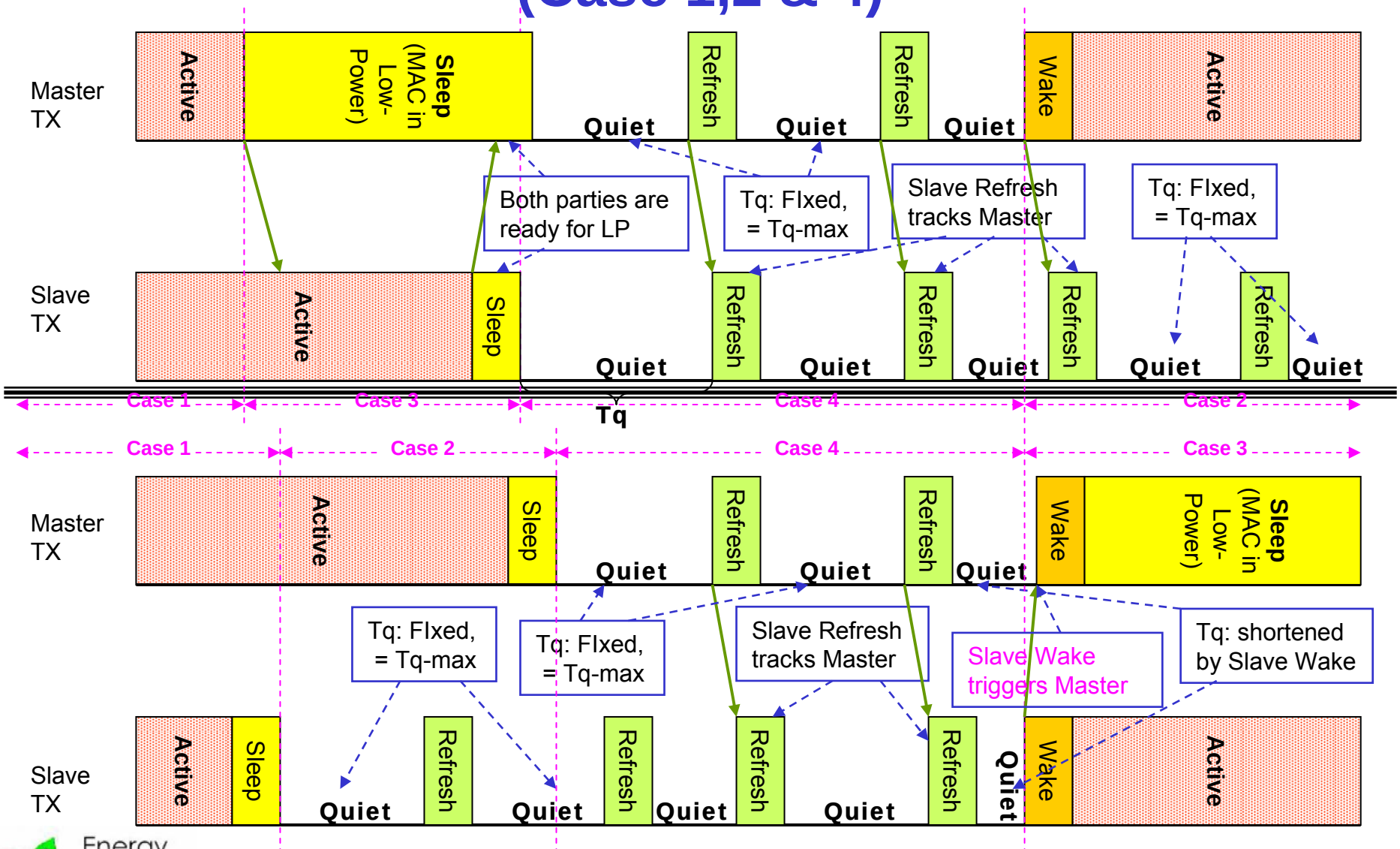
Freq value holder	Freq Resolution
S13.11f	~8 ppm
S14.12f	~4 ppm
S15.13f	~2 ppm
Floating Point	~0.25 ppm

S13.11f means 2^11=2000 symbols to update one clock phase (=1/64 UI). 1UI=128000 sym. ΔF=1/128000≈8 ppm

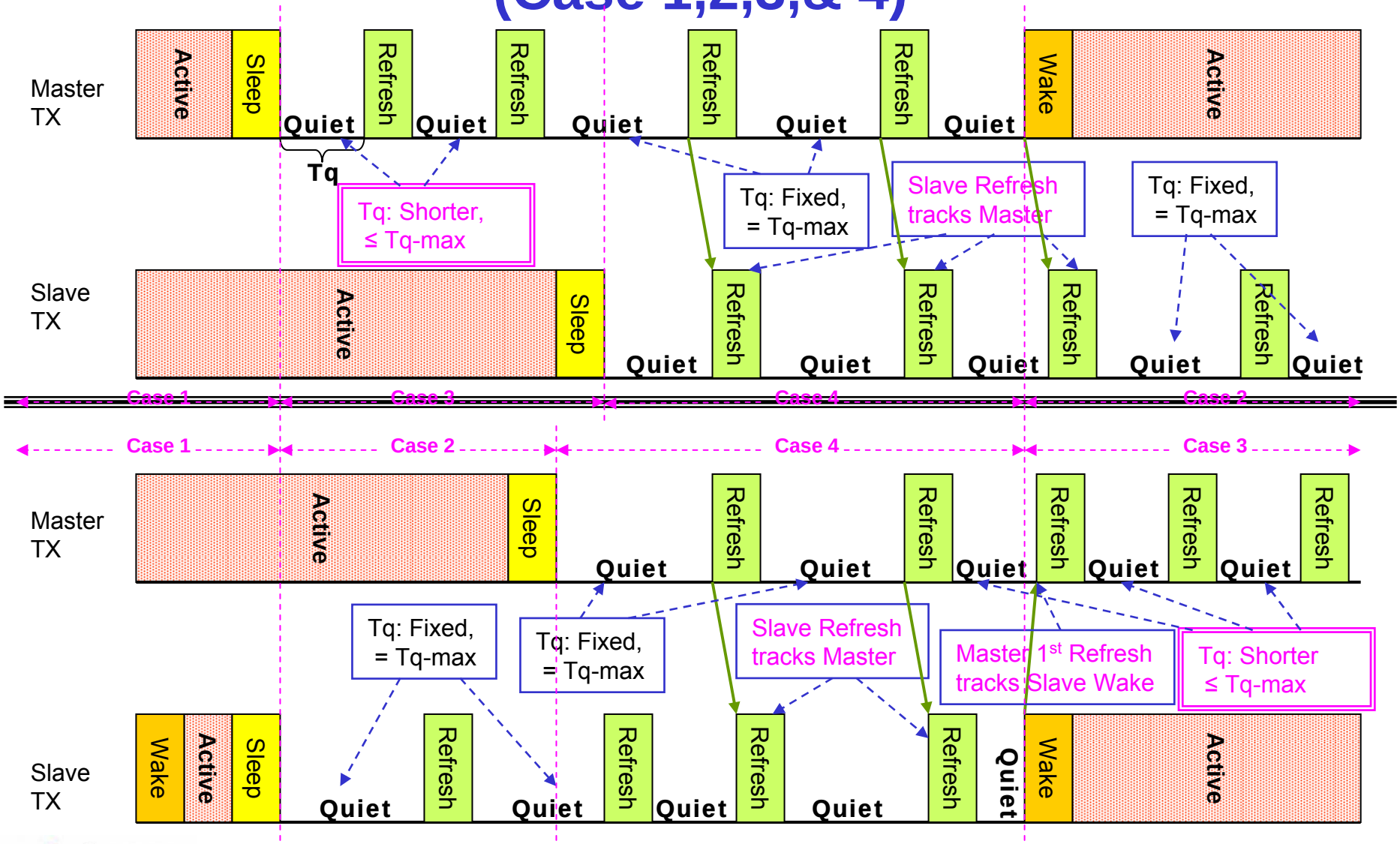
GPHY Symmetric only Operation (Case 1 & 4)



GPHY Partially Asymmetric Operations (Case 1,2 & 4)



GPHY Fully Asymmetric Operations (Case 1,2,3,& 4)



Summary

- Asymmetric EEE GPHY Can homogenously work with Asymmetric EEE MAC and system interface.
  - Master active, slave LPI: Natural one way operation.
  - Master LPI, slave active: Most sensitive to Timing drift and Echo/NEXT noise. Master needs to send Refresh with duration based on the estimation of frequency drift of slave PLL and SNR sensitivity of clock phase of master.
  - Master and slave LPI: Slave needs to send Refresh by tracking Master's Refresh to synchronize the clock and coefficients.
  - Symmetric mode becomes a special case.
- The Refresh and Quite durations are correlated and can be negotiated using AN, possibly adjusted using MCF.
- Advantageous to allow Asymmetric modes which can save more power and have negligible cost to implement

Thank you

Questions?