Lane Bonding Considerations

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Lane Bonding Mechanisms

- 40G and 100G channels require multiple-lane PHYs based on MMF/SMF optical fibers, copper cables, PC traces, or WDM wavelengths.

- Bonding mechanisms are required to unify the lanes into a single channel.
  - 40G channel architecture may be 4X10G…1X40G (future)
  - 100G channel architecture may be 10X10G, 4X25G …1X100G (future)

- Lane bonding proposals have been presented to HSSG…
  - Aggregation (at the) Physical Layer (APL)
  - 100G Ten Bit Interface (CTBI)
  - Physical Bundling Layer (PBL)

- Desirable to use a common mechanism for both 40G and 100G channels

- Other desirable objectives…
  - Simplicity
  - Ease of implementation
  - Scalability
  - Minimum size, power, heat
• Aggregation (at the) Physical Layer (APL) provides “variable-length fragment-based” lane bonding with packet fragmentation and reassembly mechanisms.
• Uses 64B/66B PCS technology as in 10GE.
• Frames are decimated into variable lengths that complicate reassembly and error control procedures…sublayer processing overhead may be high.
• May re-use 10G PHY technology.
• Potentially scalable to 4X25G SMF and 1X40G SMF channels.

• 4X25G SMF or 1X40G SMF with APL would require new VLSI technology.
  – Requires PCS functions in optical transceiver modules...for example, two chip development cycles, one in CMOS, another in SiGe.
• 100G Ten Bit Interface (CTBI) concept based on inverse muxing to “Virtual Lanes”, bit mapping to/from electrical lanes with alignment and skew compensation at Rx PCS.
• Uses 64B/66B PCS technology as in 10GE.
• Efficient for all 802.3ba channel architectures…
  – supports full MAC line rate
• By inspection, PCS processing overhead is low.
• Flexible Virtual Lane architecture…
  – Independent of frame size
• Single PCS works with multiple, different PMDs.
• Can be implemented in current FPGA technology.
• 4X25G SMF and 1X40G with CTBI will require CMOS chip development, but no new technology.
Physical Bundling Layer (PBL) bonding is similar to APL…
  - Bonds physical layers with PCS for each PMD

Uses 64B/66B PCS technology as in 10GE

PBL performs distribution and reassembly of fixed-size, 64-bit data blocks over multiple lanes
  - Fixed-size blocks simplify implementation

Multiple lane alignment mechanism may be complex…now under study.

4X25G SMF and 1X40G SMF with PBL will require new VLSI technology.
  - Requires PCS functions in optical transceiver modules…for example, two chip development cycles, one in CMOS, another in SiGe.
40G KR Backplane

**APL**
- MAC(40G)
- RS
- APL(40G)
- PCS
- PCS
- PCS
- PCS
- FEC
- FEC
- FEC
- FEC
- PMA
- PMA
- PMA
- PMA
- PMD
- PMD
- PMD
- PMD
- \(4 \times 10\text{GBASE-KR}\)

**CTBI**
- MAC(40G)
- RS
- PCS (40G)
- PCS
- PCS
- PCS
- PCS
- FEC
- FEC
- FEC
- FEC
- PMA
- PMA
- PMA
- PMA
- PMD
- PMD
- PMD
- PMD
- \(4 \times 10\text{GBASE-KR}\)

**PBL**
- MAC(40G)
- RS
- PBL(40G)
- PCS
- PCS
- PCS
- PCS
- FEC
- FEC
- FEC
- FEC
- PMA
- PMA
- PMA
- PMA
- PMD
- PMD
- PMD
- PMD
- \(4 \times 10\text{GBASE-KR}\)

\[\text{FEC} = 10\text{GBASE-KR FEC (Clause 71)}\]
1 X 40G SMF

**APL**
- MAC (40G)
- RS
- APL (40G)
- PCS

**CTBI**
- MAC (40G)
- RS
- PCS (40G)
- CTBI

**PBL**
- MAC (40G)
- RS
- PBL (40G)
- PCS

- 40G PCS
- PMA
- PMD

1x40G, SMF

- PMA
- PMD

1x40G, SMF

- 40G PCS
- PMA
- PMD

1x40G, SMF
Lane Bonding Mechanism Evaluation

• Desirability of the three lane bonding proposals was evaluated with four criteria…
  – Simplicity
  – Ease of implementation
  – Scalability
  – Minimum size, power, heat
• The five criteria were considered with five 802.3ba cases…
  – 4X10G KR Backplane
  – 4X10G MMF
  – 10X10G MMF
  – 4X25G SMF
  – 1X40G SMF
• “Relative Desirability” was estimated for each case.
Evaluation Observations

- **APL...**
  - High-level complexity, probably with high sublayer processing overhead
  - Difficult implementation...new VLSI technology for 4X25G SMF
  - Scalability diluted by complexity
  - Complexity drives increased size, power, heat

- **CTBI...**
  - Lower-level complexity compared with APL and PBL
  - Implementation with current VLSI technology for 4X25G SMF
  - Scalable from 4X10G KR to 1X100G SMF
  - Simplicity drives reduced size, power, heat

- **PBL...**
  - Moderate-level complexity in current proposals
  - Difficult implementation...new VLSI technology for 4X25G SMF
  - Scalability diluted by complexity
  - Complexity drives increased size, power, heat
Relative Desirability

Desirability Criteria
- Simplicity
- Ease of implementation
- Scalability
- Minimum size, power, heat

Technology

CTBI
PBL
APL

4 X KR Backplane
4 X 10G MMF
10 X 10G MMF
4 X 25G SMF
1 X 40G SMF

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Conclusions

• With 4X10G KR, 4X10G MMF, 10X10G, APL, CTBI and PBL have similar Relative Desirability

• With 4X25G 10/40km SMF, APL and PBL have decreased Desirability due to protocol functionality in the optical module, requiring new VLSI.

• With 1X40G SMF, APL and PBL have decreased Desirability, requiring new VLSI technology in the optical module.

• In the future, the simplicity of CTBI will enable scaling to 1X100G SMF.

• CTBI emerges as the most Desirable lane bonding mechanism.

• Recommendation…adopt CTBI as the lane bonding mechanism for IEEE 802.3ba.