Link budget for 40GBASE-CR4 and 100GBASE-CR10

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Comment #287: Problem statement

• 2.5 dB of the 3.0 dB signal-to-noise (SNR) ratio penalty allocated for reflective loss has been re-assigned to crosstalk

• Stated rationale is that tighter constraints on insertion loss deviation (ILD) reduce the penalty

• ILD constraints apply to the cable assembly and not the channel

• ILD penalty is a function the transmitter and receiver return loss and the channel input and output return loss

• The channel does not appear to be sufficiently constrained to ensure the 2.5 dB trade-off
### Summary of cable assembly and channel parameters

#### Cable assembly parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Expression</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion loss limit</td>
<td>$IL_{ca,max}(f) = 0.192749\sqrt{f} + 0.001494f$</td>
<td>Insertion loss limit</td>
</tr>
<tr>
<td>Insertion loss to crosstalk ratio limit</td>
<td>$ICR_{ca,min}(f) = 23.3 - 18.7\log_{10}(f / 5\text{ GHz})$</td>
<td>Insertion loss to crosstalk ratio limit</td>
</tr>
<tr>
<td>Power-sum crosstalk loss limit</td>
<td>$PSXT_{ca,max}(f) = IL_{ca,max}(f) + ICR_{ca,min}(f)$</td>
<td>Power-sum crosstalk loss limit$^1$</td>
</tr>
</tbody>
</table>

#### Channel parameters

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<tbody>
<tr>
<td>Insertion loss limit</td>
<td>$IL_{ch,max}(f) = IL_{ca,max}(f) + 2IL_{pcb,max}(f)$</td>
<td>Insertion loss limit$^2$</td>
</tr>
<tr>
<td>Insertion loss to crosstalk ratio limit</td>
<td>$ICR_{ch,min}(f) = (23.3 - 2.5) - 18.7\log_{10}(f / 5\text{ GHz})$</td>
<td>Insertion loss to crosstalk ratio limit</td>
</tr>
<tr>
<td>Power-sum crosstalk loss limit</td>
<td>$PSXT_{ch,max}(f) = IL_{ch,max}(f) + ICR_{ch,min}(f)$</td>
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<td>$PSXT_{ch,max}(f) = PSXT_{ca,max}(f) + 2IL_{pcb,max}(f) - 2.5$</td>
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$^1$ Inferred from $ICR_{min}(f)$ assuming insertion loss $IL_{max}(f)$

$^2$ Not explicitly stated in the draft, but inferred from discussions related to the original proposal
Observations on channel limits

• Consider a cable assembly with worst case ICR

• The channel ICR limit implies that, when the host printed circuit board (PCB) insertion loss is zero, the channel may have 2.5 dB more noise than the cable assembly
  – In this case, the channel is identical to cable assembly and one would expect it to have the same noise

• As the PCB insertion loss increases, eventually the channel must have a negative contribution to the total noise
  \[
  PSXT_{ch}(f) = PSXT_{ca}(f) + 2IL_{pcb}(f) - 2.5
  \]

• Is it feasible to have a channel that satisfies these constraints with a worst-case cable assembly and worst-case host trace?
Insertion loss deviation (ILD)

\[ ILD(f) = IL(f) - IL_{fit}(f) \]

\[ IL(f) = 20 \log_{10}|s_{21}| \]

• Difference between measured insertion loss and fitted insertion loss

• Consider the voltage transfer function from TP0 to TP5

\[ ILD_v(f) = ILD(f) + 20 \log_{10} \left| \frac{1 + \Gamma_L}{D(f)} \right| \]

\[ D(f) = 1 - \Gamma_S s_{11} - \Gamma_L s_{22} - \Gamma_S \Gamma_L (s_{12} s_{21} - s_{11} s_{22}) \]
Observations on ILD penalty

• The ILD penalty is based on the voltage transfer function from TP0 to TP5

• The transfer function is influenced by the channel return loss \((s_{11} \text{ and } s_{22})\) and the transmitter and receiver return loss \((\Gamma_S \text{ and } \Gamma_L)\)

• Draft 1.1 currently only limits ILD of the cable assembly

• The ILD penalty cannot be limited unless the channel ILD and return loss are also limited

• There is no way to ensure that the penalty will be limited to 0.5 dB
Path to resolution

• Explicitly define the channel insertion loss limit

• Add channel insertion loss deviation (ILD) specifications

• Add channel input and output return loss specifications

• Demonstrate sub-0.5 dB penalty for specification set

• Reconsider the relationship between the cable assembly and channel ICR
Comments #666 and #667: Problem statement

• ICR as a function of log-frequency may not necessarily be linear for components that otherwise function acceptably in practice

• Line fit and comparison to mask could cause such components to be rejected

• Alternate curve fits could be explored, but this leaves to the door open to bias against other, otherwise acceptable, implementations at some point in the future
**Salz SNR**

- Maximum achievable signal-to-noise ratio at the decision point of an ideal MMSE-DFE (minimum mean-squared-error decision feedback equalizer)
- Channel parameters measured over a frequency grid (interval $\Delta f$) spanning the range $[f_{\text{min}}, f_{\text{max}}]$
  - Assume the signal energy is zero outside of the measured range
  - This will reduce the calculated Salz SNR (conservative)
- Considering no folds, the calculation simplifies to...

$$SNR_{\text{Salz},0} = 2T\Delta f \sum_{i} 10 \log_{10} \left[ 10^{\frac{\text{ICR}(f_i)}{10}} + 1 \right], \quad 0 \leq f_i \leq \frac{1}{2T}$$

- To determine fitness for use, the computed Salz SNR is compared to SNR required for operation at the target bit error ratio
  - Let $SNR_0$ be the required SNR (e.g. approximately 17 dB for $BER \leq 10^{-12}$)
  - Enforce margin $M$ to account for DFE implementation constraints

Example: 10GBASE-KR

- For 10GBASE-KR, $ICR(f)$ is recommended to be:

\[
ICR_{\text{min}}(f) = 23.3 - 18.7 \log_{10}\left(\frac{f}{5 \text{ GHz}}\right), \quad 100 \text{ MHz} \leq f \leq 5.15625 \text{ GHz}
\]

- From this equation, the Salz SNR (0 folds) is approximately 30 dB
Proposal

• Replace linear fit to ICR with integral expression based on Salz SNR

• Metric is insensitive to exact shape of the ICR characteristic

• Metric is rooted in fundamental theory of DFE performance

• Propose that the channel SNR be better than 30 dB for compatibility with implementations based on 10GBASE-KR
  – Cable assembly SNR should be better to account for host PCB traces
Questions?