40G/100G Implementations with 10G FPGA

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Accepted Baseline 40GE/100GE Architecture

“n” Lane MAC/PCS to PMA/PMD Electrical Interface
a) n= 10 Lanes for 100GE initially
b) n= 4 Lanes for 40GE initially
Each lane runs at 10.3125 Gbps

1: Includes MLD functionality
2: For 40GE Backplane
Baseline Architecture Expected
PCS/MLD ↔ PMA Interfaces

n = 4 for 40G and
n = 10 for 100G,
@10.3125 Gbps
for each lane
40 nm FPGA SERDES Test Chip
Eye Diagram and BER Bathtub Curve @ 10.3125 Gbps

- Pattern
  - PRBS $2^{31-1}$
- Vod
  - 600 mV
- DJ ($\delta-\delta$)
  - 5.08 ps
- RJ (rms)
  - 1.46 ps
- TJ (@ BER = $10^{-12}$)
  - 25.6 ps (exceeds XLAUI/CAUI requirement)

FPGAs that embed 10.3125G SERDES will be available in early 2009
Test Chips are available since early 2008
FPGA 10.3125G SERDES have pre/de-emphasis, FFE/CTLE equalization capabilities
10.3125 Gbps FPGA Transceiver Enables a Direct PCS/MLD ↔ PMA Interfaces
Characteristics for Integrated & Direct 10.3125 Gbps Interfaces

- 10.3125 Gbps FPGA transceiver will be available in the near future
- 10.3125 Gbps transceiver eliminates the needs of “SERDES mux”, offering minimum transceiver pin count, power consumption, simple and fully integrated chip-to-chip interfaces
- 10.3125 Gbps transceiver is in-line with the XLAUI/CAUI chip-to-chip electrical interfaces for 40G/100G
- 10.3125 Gbps FPGA transceiver can also support 8x/20x 5.15625 Gbps (lower per lane rate) electrical interfaces for 40G/100G as needed
Summary

- FPGAs with 10.3125 Gbps transceivers will be available in the near future.
- 40G/100G implementation with 10G FPGA transceivers do not need “SERDES muxes”
  - 10.3125 Gbps transceivers offer minimum transceiver count, lower power consumption & easier layout
  - Increase the # of VL to support the 40G implementation with lower data rate transceiver is not necessary.
- 10.3125 Gbps transceiver is in-line with the XLAUI/CAUI chip-to-chip electrical interfaces for 40G/100G.
- 10.3125 Gbps FPGA transceiver can also support 8x/20x5.15625 Gbps (or even lower per lane rate) electrical interfaces for 40G/100G as needed.
Thank you
Backup

40G Implementation

5.15625G Implementation

MAC (40G)
RS
PCS
MLD

8x 5.15625G

5.15625G Implementation

MAC (40G)
RS
PCS
MLD

4 x 10.3125G

100G Implementation

5.15625G Implementation

MAC (100G)
RS
PCS
MLD

20x 5.15625G

5.15625G Implementation

MAC (100G)
RS
PCS
MLD

10 x 10.3125G

100G Implementation

MAC (100G)
RS
PCS
MLD

10 x 10.3125G

8x 5.15625G

4 x 10.3125G

CAUI

PMA
PMD

XLAUI

PMA
PMD

XLAUI

PMA
PMD