

40GE and 100GE Transport over OTN

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Abstract & Purpose

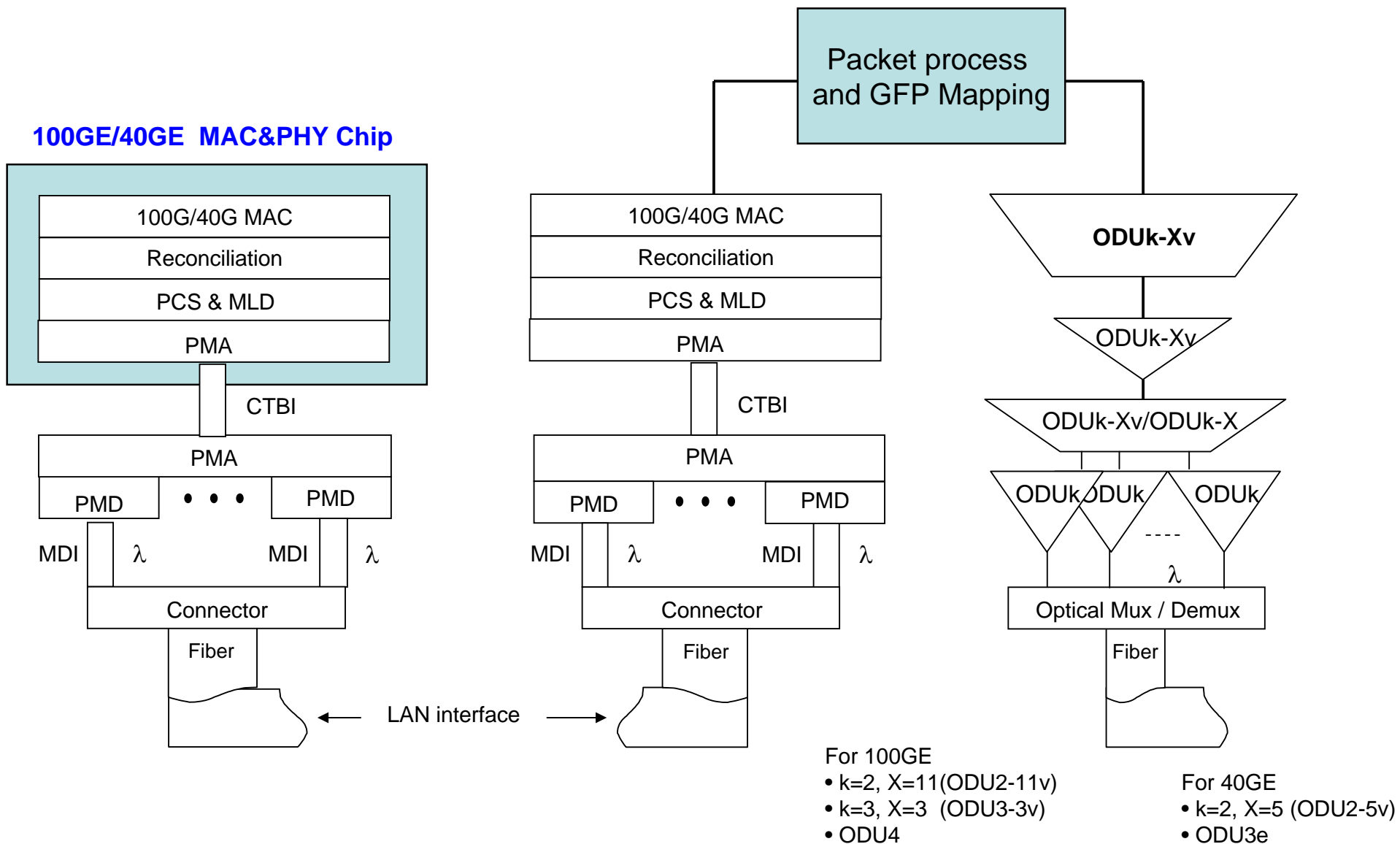
- **This contribution discusses the deskew budget requirement for 100GE & 40GE to be bit-transparently transported over a single domain OTN in addition to the deskew margin reserved for supporting future possible new multi-lane PMD objectives. The total deskew budget value is open for further discussions.**
- **We propose to allow both Lane-Aggregate and Lane-Independent transport models to meet different requirements for multi-lane HSE over OTN, or at minimum treat the Lane-Independent transport model as an option for supporting bit-transparency in addition to supporting PCS code word transparency by the Lane-Aggregate transport model.**
 - **Lane-Aggregate transport is PCS codeword transparency oriented. It is an approach with broad support in the task force for the OTN support objective.**
 - **Lane Independent transport is bit-transparency oriented. It is simpler to implement than the Lane-aggregate transport while supporting bit transparency for 100GE&40GE transport over a single OTN domain.**
- **Propose to support a larger skew tolerance at the HSE multi-lane receiver side to allow Lane Independent transport over OTN**

Ethernet Transparency Requirement over OTN

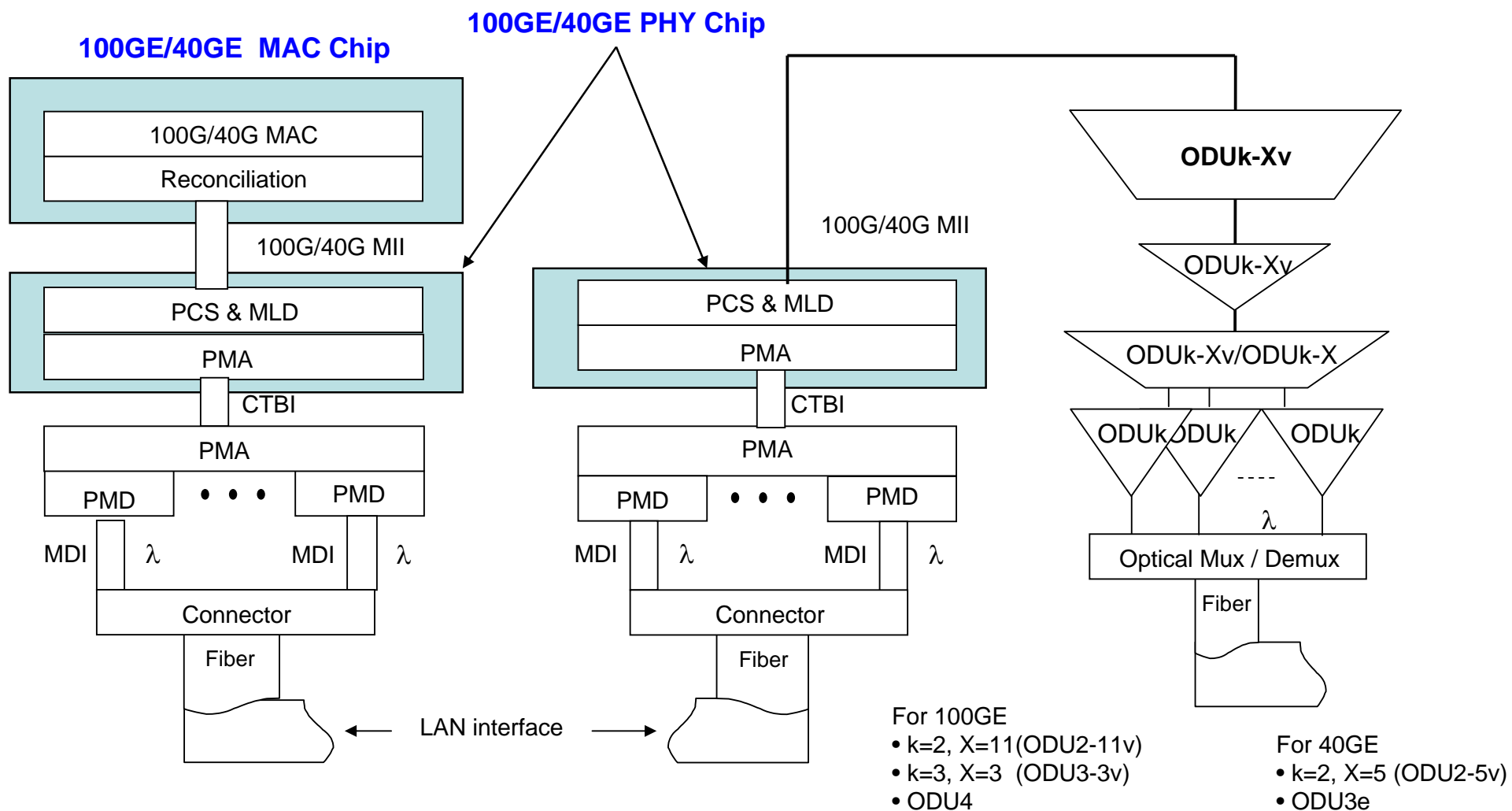
	Transparency Requirement	100GE	40GE
(1*)	MAC Frame Transparency	Packet Transparency (supporting packet based service) (Out of Scope of this contribution)	Packet Transparency (supporting packet based service) (Out of Scope of this contribution)
(2*)	MAC Frame & Preamble Transparency		
(3*)	PCS codeword transparency support by Lane-Aggregate Mapping	PCS Codeword Transparency in standard ODU2-11v, ODU3-3v, & future ODU4. PCS termination is not required. However, Deskew and Lane Aggregation are required,	PCS Codeword Transparency in standard ODU3 (64/66b to 512/513b transcoding is required). PCS termination is required, thus Deskew and Lane-Aggregation are required based on MLD Architecture
(4*)	Bit transparency support by Lane-Independent Mapping	Bit transparency in time slotted standard ODU2-11v, ODU3-3v, & future ODU4. PCS termination is not required. Deskew and Lane Aggregation are not required,	Bit transparency in time slotted ODU3e, standard ODU2-5v, or future/other possible OTN container (ODUg, which is Under study in ITU-T Q11), etc.. Transcoding, Deskew and Lane-Aggregation are not required.

(1*)(2*)(3*)(4*): Refer to OIF2008.031.05, "OIF Carrier WG Requirements, High Speed Ethernet Transport over Optical Transport Networks"

Packet Transparent Mapping of 100GE&40GE

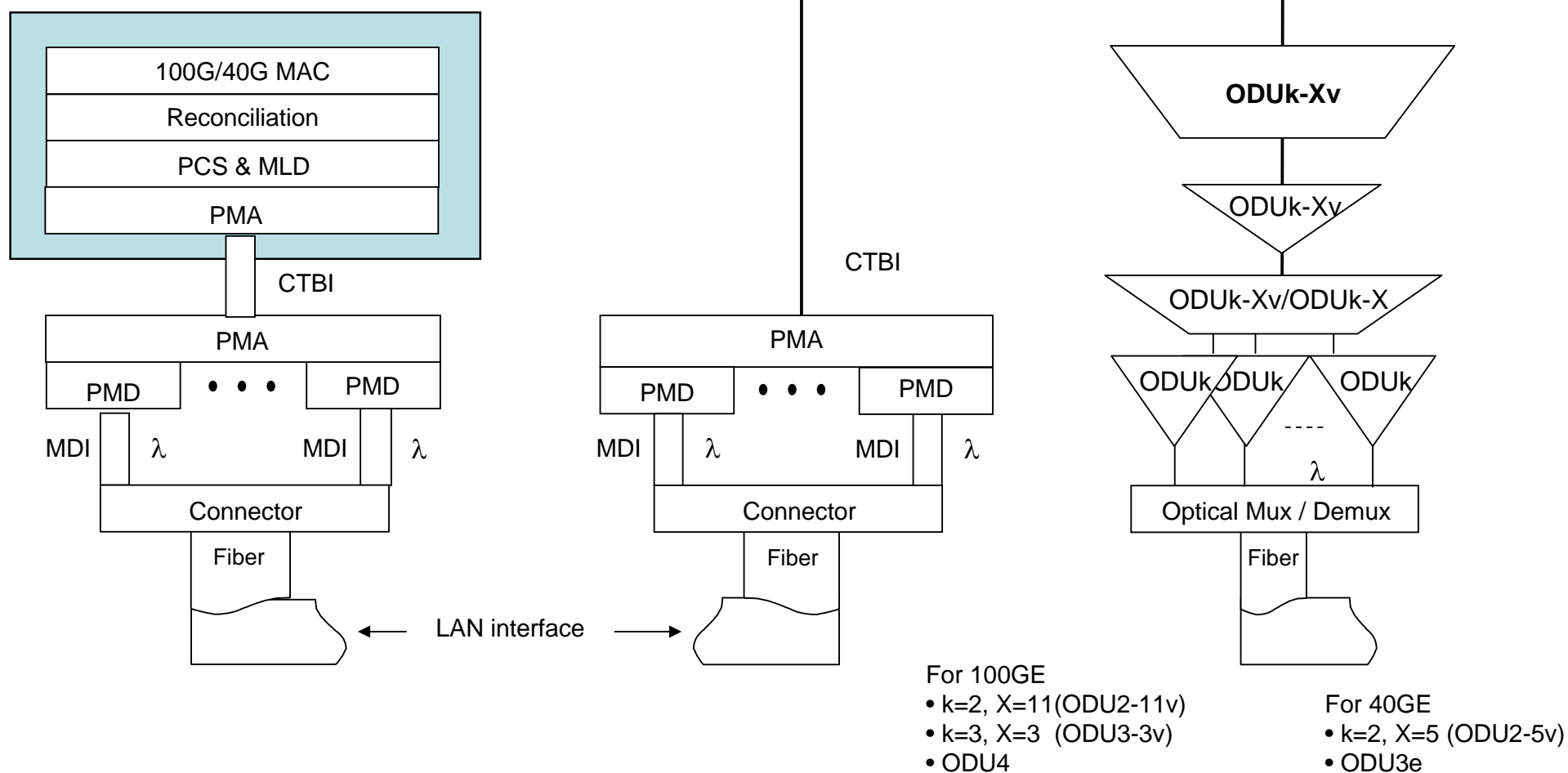


PCS Transparent Mapping of 100GE&40GE



Bit Transparent Mapping of 100GE&40GE

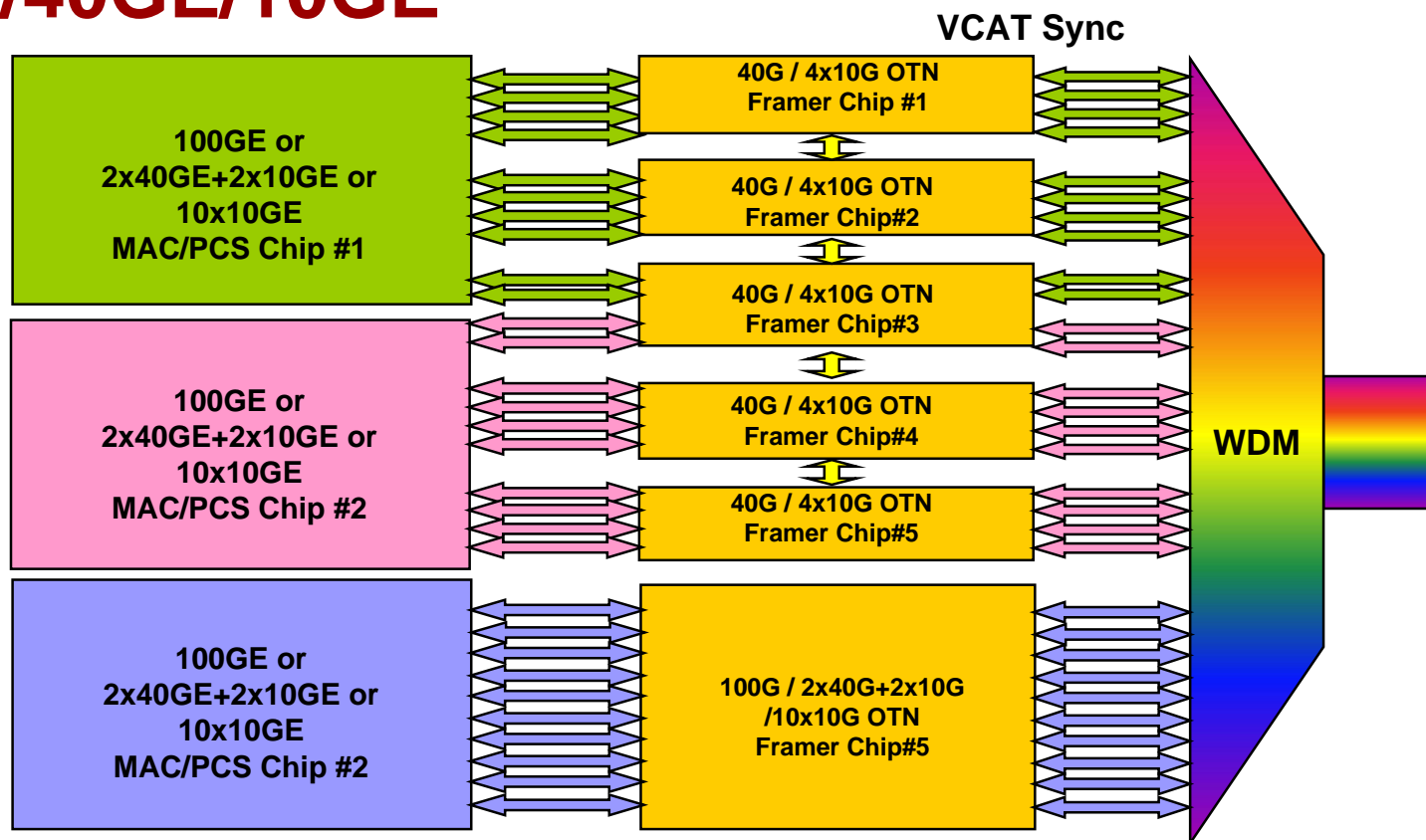
100GE/40GE MAC&PHY Chip



Bit Transparency and Lane-independent Transport

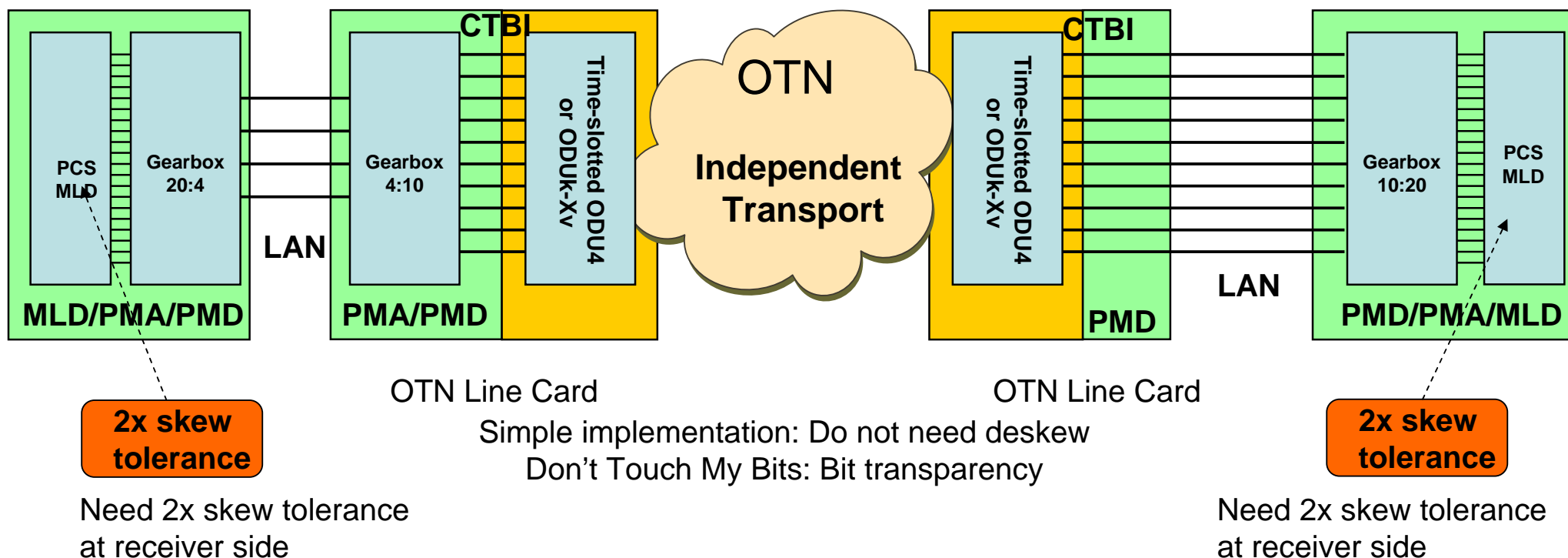
- **Consideration of Bit Transparency leads to Lane-independent transport model at CTBI interface for 100GE and 40GE.**
- **Lane-independent transport model:**
 - **Simple implementation and low complexity leading to low cost**
 - **Enabling a common OTN platform for supporting 10GE, 40GE and 100GE**
 - **Free to use different PMD at the ingress and Egress of OTN**
 - **A key feature of MLD,**
 - **Not the feature of lane-aggregate or Lane-independent transport model**
 - **Support 100GE bit transparency in time slotted ODU2-11v, ODU3-3v, ODU4**
 - **Support 40GE bit transparency in ODU3e, ODU2-5v**
 - **Compatible with 40GE codeword transparency based on 512/513b transcoding of 64/66b per lane in standard ODU3.**

Lane-Independent Common OTN Platform for 100GE/40GE/10GE



- Single MAC/PCS definition/Chip support of 100GE, 40GE, and 10GE should be considered.
- “Lane-Independent model” enables OTN system to compatibly implement 100GE, 40GE, and 10GE transport service over a common platform, thus reducing complexity.
- Enabling low cost multi-chip FPGA for early and quick implementation to support 100GE, 40GE and 10GE over OTN.

Lane-Independent Transport for MLD



- **No need to deskew the LAN virtual lanes at OTN ingress; No need to recover 64B/66B on each virtual lane in OTN node; 10 timeslots for 10 CTBI bit-streams. Applicable to serial 100GE (10 timeslots for 10 CTBI) for bit transparency transport**
- **Skew introduced by OTN domain will be compensated by VCAT**
 - No Multi-lane skew in ODU4
- **Free to use different PMD at the ingress and Egress of OTN**

Summary and Proposal

- ✓ Propose to include both Lane-Aggregate and Lane-Independent transport models to meet different requirements for multi-lane HSE over OTN, or treat Lane-Independent transport as an option for supporting bit transparency in addition to the PCS codeword transparency by the Lane-Aggregate transport model.
 - ✓ Lane-Aggregate transport is PCS codeword transparency oriented. It is an approach with broad support in the task force for the OTN support objective
 - ✓ Lane Independent transport is bit-transparency oriented. It is simpler to implement than the Lane-aggregate transport while supporting bit transparency for 100GE&40GE transport over a single OTN domain.
- ✓ Propose to Support a larger skew tolerance at the HSE Multi-lane Receiver side to allow Lane Independent transport over OTN

Thank You