Changes following revised compliance board specifications

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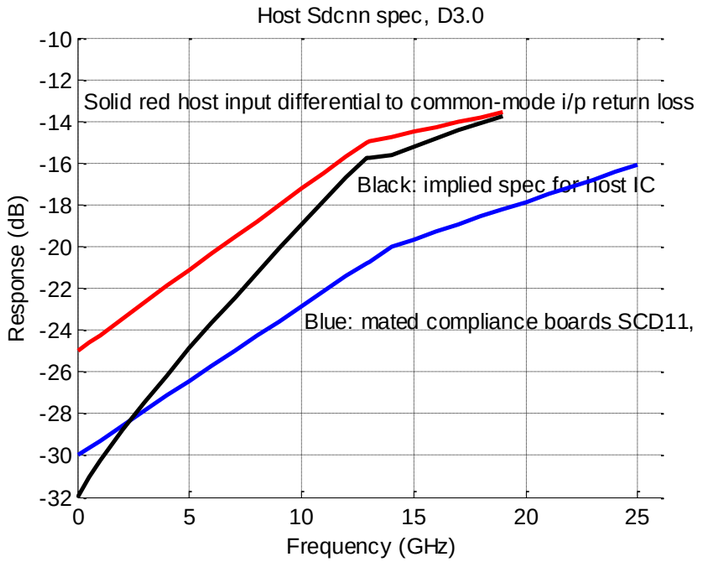
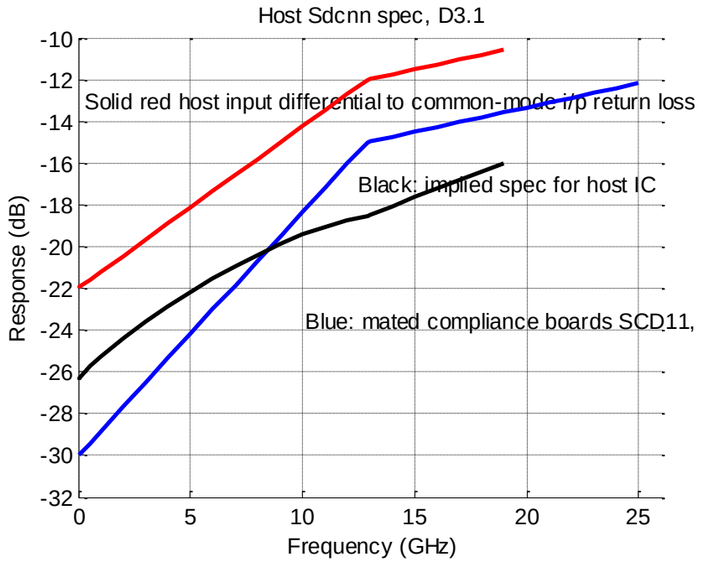
Effect on 100GBASE-CR4 host

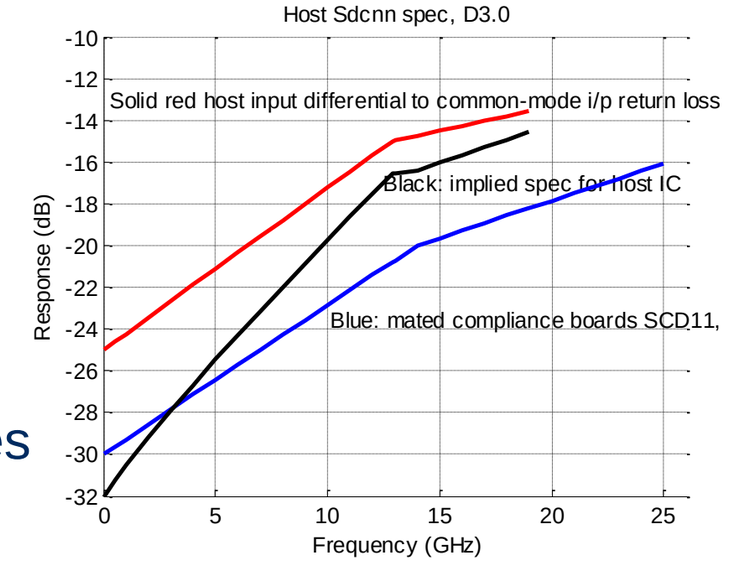
- These are "worst phase" calculations, allowing for compliance board loss
- Not including common-mode conversion insertion loss

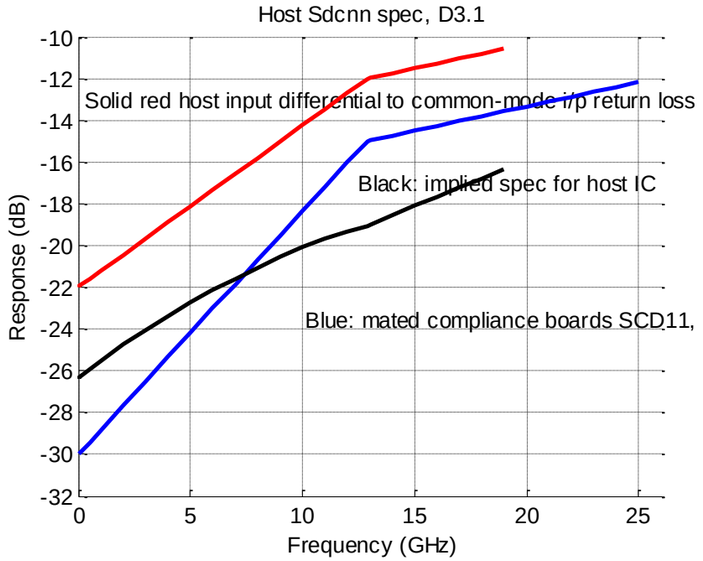
- Top: 1/2 dB connector loss
- Bottom: zero connector loss?
- Left: P802.3bj D3.0, right D3.1
- "Host IC" means at PCB/package interface

- IC must perform better above ~9 GHz
- But can perform worse at low frequencies





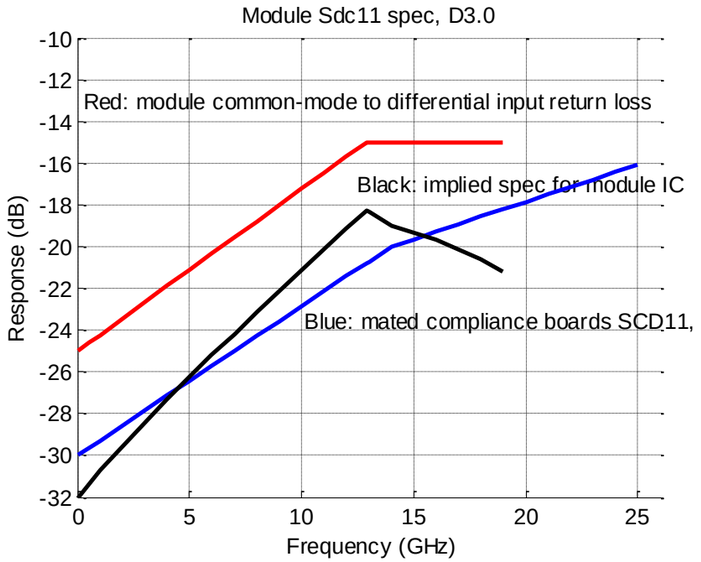


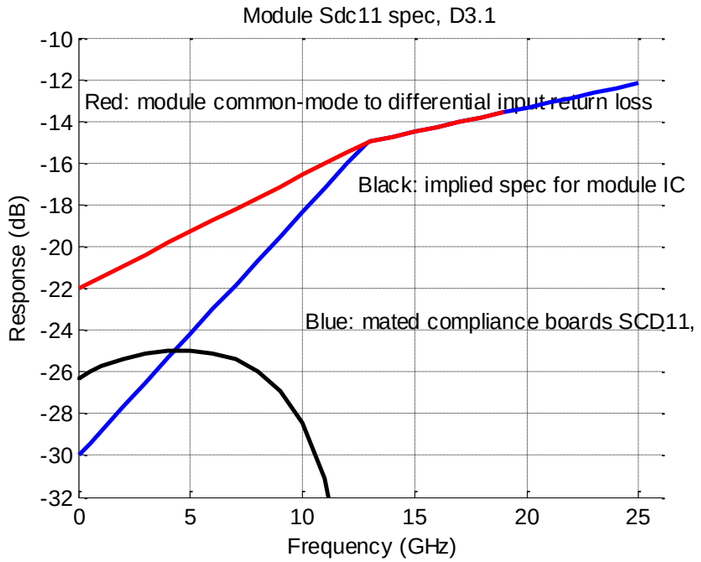


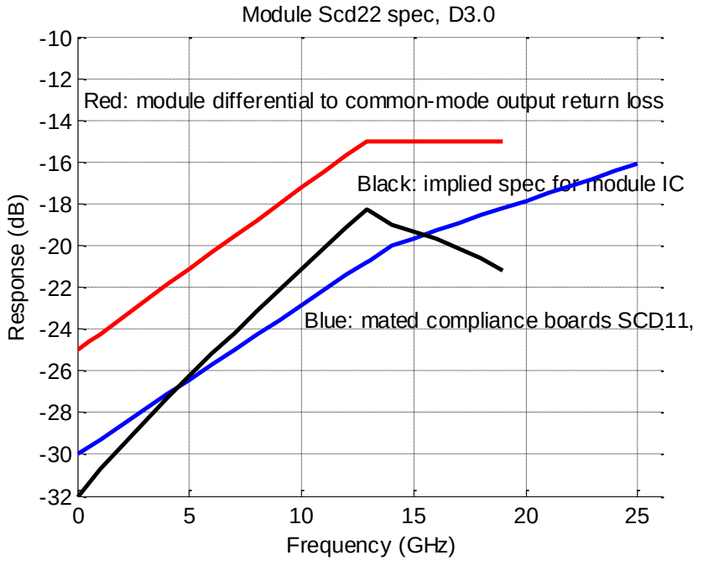
Effect on CAUI-4 module

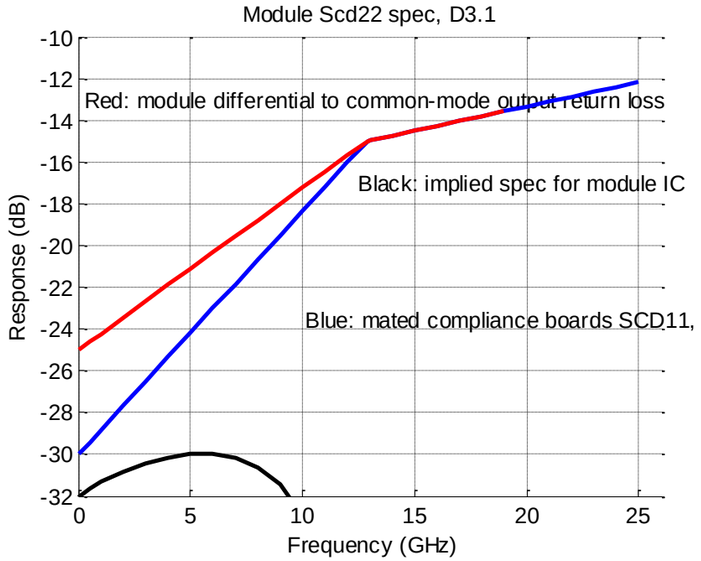
- Top: input
- Bottom: output
- Both with 1/2 dB connector loss
- Left: P802.3bj D3.0 / P802.3bm D2.0, right D3.1 / D2.1

- Mistake?









Thank You