IEEE P802.3bs
Baseline Summary

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Chair, IEEE P802.3bs 400 GbE Task Force

July 18, 2015
(Post July 2015 Plenary Summary)

Topic Matter	Motion	Reference Presentation
Architecture	• Motion #3, Jan 15: Move to adopt slides 4 and 8 from dambrosia_3bs_02b_0115 as baseline architecture.	http://www.ieee802.org/3/bs/public/15_01/dambrosia_3bs_02b_0115.pdf
RS / CDMII	• Motion #3, July 14: Move to adopt the baseline for the CDMII logical interface as shown in slide 5 of gustlin_3bs_03_0714.pdf.	http://www.ieee802.org/3/bs/public/14_07/gustlin_3bs_03_0714.pdf
PCS / PMA	• Motion #5, Jul 15: Move to adopt pages 6-22 from gustlin_3bs_02c_0715.pdf as the baseline for the 400GbE PCS and PMA.	http://www.ieee802.org/3/bs/public/15_07/gustlin_3bs_02c_0715.pdf
FEC	• Motion #3, Mar 15: Move to adopt RS(544,514,10) as the FEC in the 802.3bs 400GbE architecture	
Electrical Interfaces (C2C and C2M)	• Motion #4, Sept 14: Move to adopt 16 x 25Gb/s and 8 x 50Gb/s as the basis for the lane rates for any optional C2C and C2M electrical interfaces	
C2C / C2M 25G Electrical	• Motion #6, Sept 14: Move to adopt the P802.3bm C2C and C2M specifications with current values (except that the BER requirement is TBD) as a baseline draft for the 16 x 25Gb/s electrical interfaces	
C2C 50G Electrical	• Motion #4, Mar 15: Move to adopt li_3bs_01a_0315.pdf as the baseline proposal for CDAUI-8 chip-to-chip electrical I/O interface except for the differential return losses (on slide 11) for the TX and the RX shall be TBD .	http://www.ieee802.org/3/bs/public/15_03/li_3bs_01a_0315.pdf
C2M 50G Electrical	• Motion #5, Mar 15:Move to adopt brown_3bs_01a_0315.pdf as the baseline proposal for CDAUI-8 chip-to-module electrical I/O interface.	http://www.ieee802.org/3/bs/public/15_03/brown_3bs_01a_0315.pdf
C2C Informative Channel	• Motion #6, Jan 15: Move to adopt the following equation as the informative insertion loss equation for CDAUI-8 chip-to-chip electrical I/O interface IL <= { 1.083 + 2.543SQROOT(f) + 0.761f 0.01 <= f <= 28.05GHz} dB	
C2M Informative Channel	• Motion #8, Jan 15: Move to adopt the following equation as the informative insertion loss equation for CDAUI-8 chip-to-module electrical I/O interface IL <= { 1.076(0.075 + 0.537SQROOT(f) + 0.566f) 0.01 <= f <= 28.05GHz} dB	

See motion to note respective pages of proposal adopted, where appropriate.

EEE	• Motion #4, Jan 15: Move to adopt the EEE baseline proposed in marris_3bs_01_0115.pdf slide 7.	http://www.ieee802.org/3/bs/public/15_01/marris_3bs_01_0115.pdf
OTN	• Motion #5, Jan 15: Move to adopt slide 10 of trowbridge_3bs_01a_0115.pdf as the baseline for the OTN mapping reference point	http://www.ieee802.org/3/bs/public/15_01/trowbridge_3bs_01a_0115.pdf
100m MMF	• Motion #3, Nov 14: Move to adopt the proposal in slides 6 to 16 in king_3bs_02a_1114.pdf as the baseline proposal for the P802.3bs objective to "provide physical layer specifications which support link distances of at least 100 m of MMF" (400GBASE-SR16)*	http://www.ieee802.org/3/bs/public/14_11/king_3bs_02a_1114.pdf
500m SMF	• Motion #12, May 15: Move to adopt 4x100G PAM4 PSM4 as the modulation format for the 500m SMF (single mode fiber) PMD objective	
500m SMF	• Motion #3, Jul 15: Move to adopt a baseline for the 500m SMF proposal based on welch_3bs_01a_0715 as 400GBASE-DR4.	http://www.ieee802.org/3/bs/public/15_07/welch_3bs_01a_0715.pdf
2km SMF	• Motion #4, Jul 15: Move to adopt a baseline for the 2km SMF PMD objective based on the 2km proposal in slides 6-9 of cole_3bs_01a_0715	http://www.ieee802.org/3/bs/public/15_07/cole_3bs_01a_0715.pdf
10km SMF	▪ Motion #4, July 14: Move that 10km 400GbE SMF PMD will use a duplex fiber solution. ▪ Motion #6, May 15: Move to adopt 8 lambda x 50 Gb/s as the basis for the 10 km SMF PMD objective ▪ Motion #9, May 15: Move to adopt 8x50G PAM4 as the modulation format for the 10km SMF (single mode fiber) PMD objective ▪ Motion #11, May 15: Move to adopt a baseline for the 10km SMF PMD objective based on the 10km proposal in cole_3bs_01a_0515	http://www.ieee802.org/3/bs/public/15_05/cole_3bs_01a_0515.pdf

See motion to note respective pages of proposal adopted, where appropriate.

400GbE Architecture Baseline Proposal (Update)

IEEE P802.3bs 400 Gb/s Ethernet Task Force

January 2015

Pete Anslow - Ciena
John D'Ambrosia – Dell
Mark Gustlin – Xilinx
Adam Healey – Avago
David Law – HP
Gary Nicholl - Cisco
Dave Ofelt – Juniper
Steve Trowbridge - ALU

What Needs to be Supported in the Architecture?

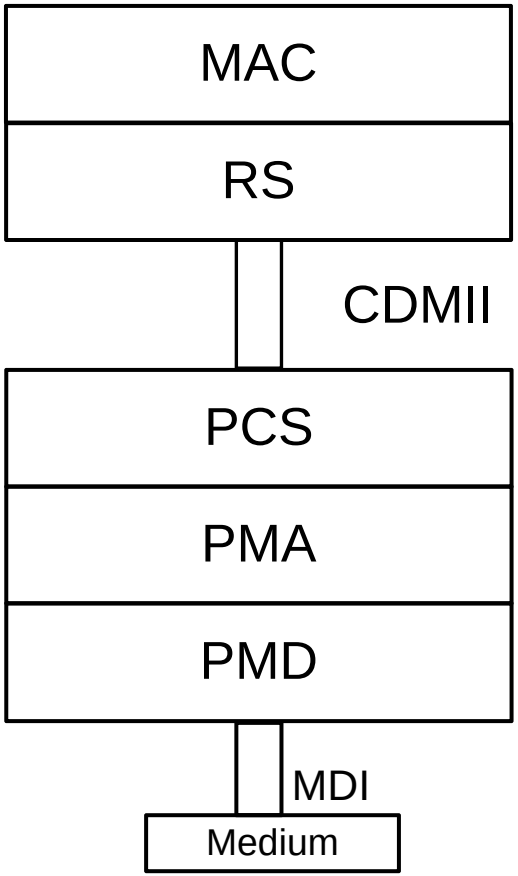
- The coding needs of the electrical interface may vary independently from the PMD interface
- The requirements for each interface can be different, both the FEC, modulation and number of lanes can change over time for each interface
- We need a single high level architecture which can support the evolving requirements of the interfaces over time
  - This does not mean it requires a complicated implementation
- A Media Independent interface needs to be specified to enable standardization of different PHYs today and future, “unknown”, PHYs tomorrow.
- We need an electrical interface between different devices, CDAUI (C2C & C2M)
- IEEE 802.3 supports two “levels” of implementers
  - The system implementer
  - The component implementer

Sublayer Functions (at a high level)

Sublayer	10GbE	100GbE	400GbE (proposed)
MAC	Framing, addressing, error detection	Framing, addressing, error detection	Framing, addressing, error detection
Extender	XGXS (PCS + PMA function)	N/A	CDXS (PCS + FEC function)
PCS	Coding (X: 8B/10B, R: 64B/66B), lane distribution, EEE	Coding (64B/66B), lane distribution, EEE	Coding, lane distribution, EEE, FEC
FEC	FEC, transcoding	FEC, transcoding, align and deskew	N/A
PMA	Serialization, clock and data recovery	Muxing, clock and data recovery, HOM	Muxing, clock and data recovery, HOM??
PMD	Physical interface driver	Physical interface driver	Physical interface driver

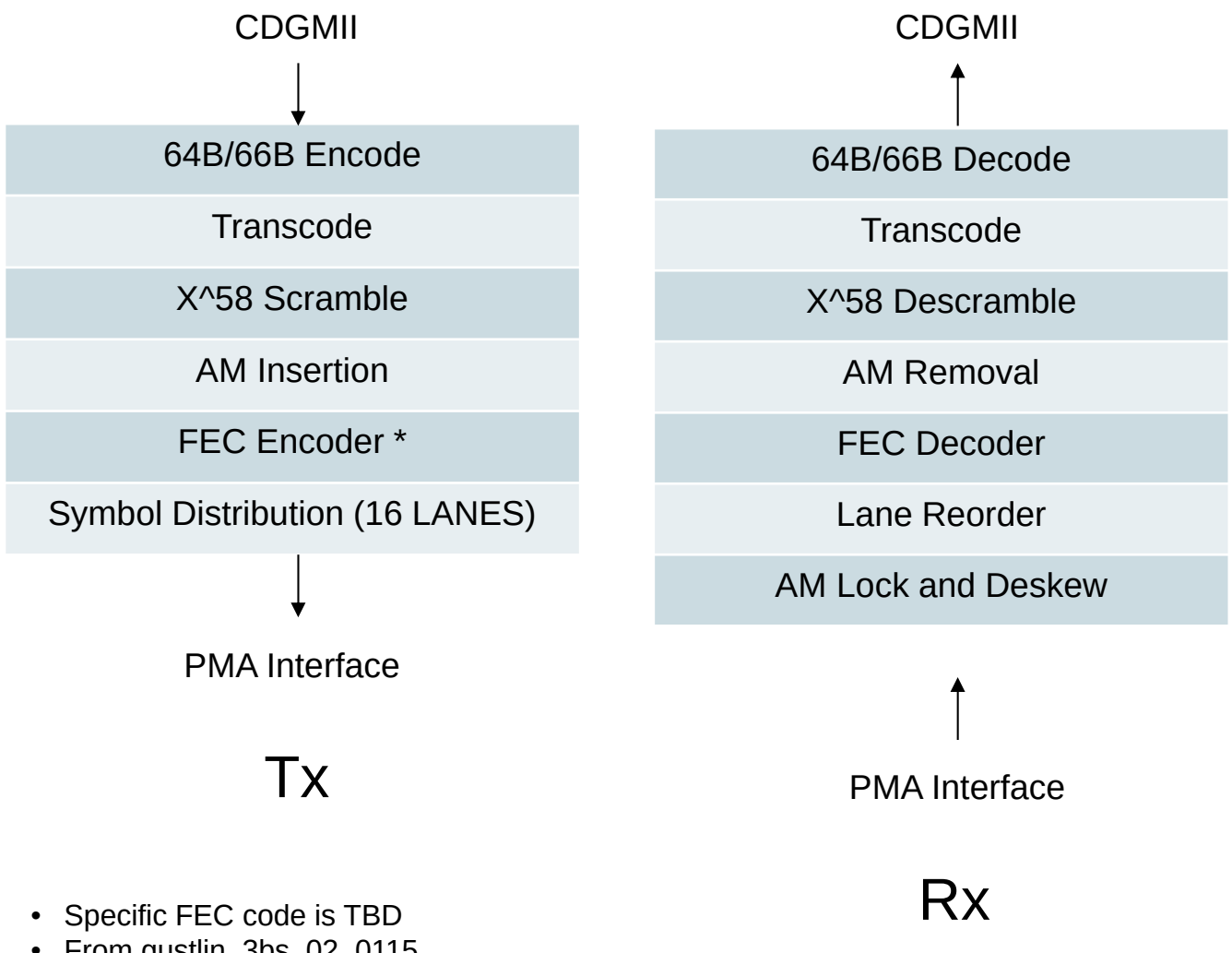
Note that there are variations with a single speed, not all are captured in this table

The 400GbE Basic Layer Diagram



- But…
  - To enable flexibility for future efforts, an extender sublayer for the CDMII is desirable, but there is no physical instantiation of the CDMII.
  - From a standardization perspective, it can leverage a CDAUI, which is a optional physical instantiation of the PMA service interface

PCS Block Diagrams



- Specific FEC code is TBD
- From gustlin_3bs_02_0115

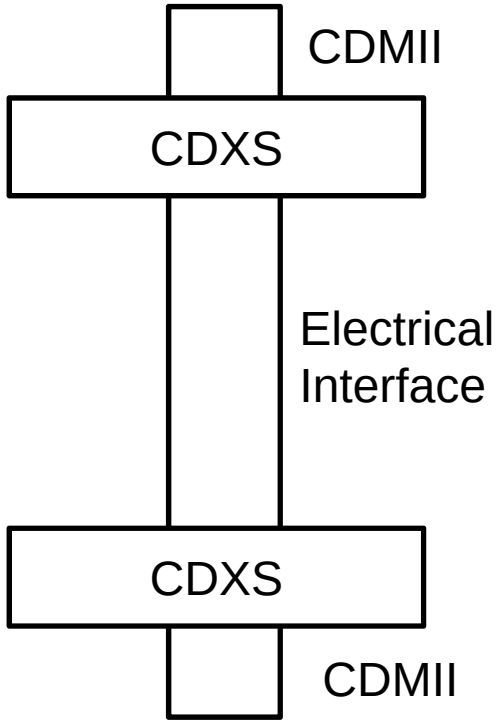
PMA

The following are the functions performed by the PMA sublayer

- Provide appropriate multiplexing
- Provide appropriate modulation (PAM4 for instance if required)
- Provide per input-lane clock and data recovery
- Provide clock generation
- Provide signal drivers
- Optionally provide local loopback to/from the PMA service interface
- Optionally provide remote loopback to/from the PMD service interface
- Optionally provide test-pattern generation and detection
- Tolerate Skew Variation

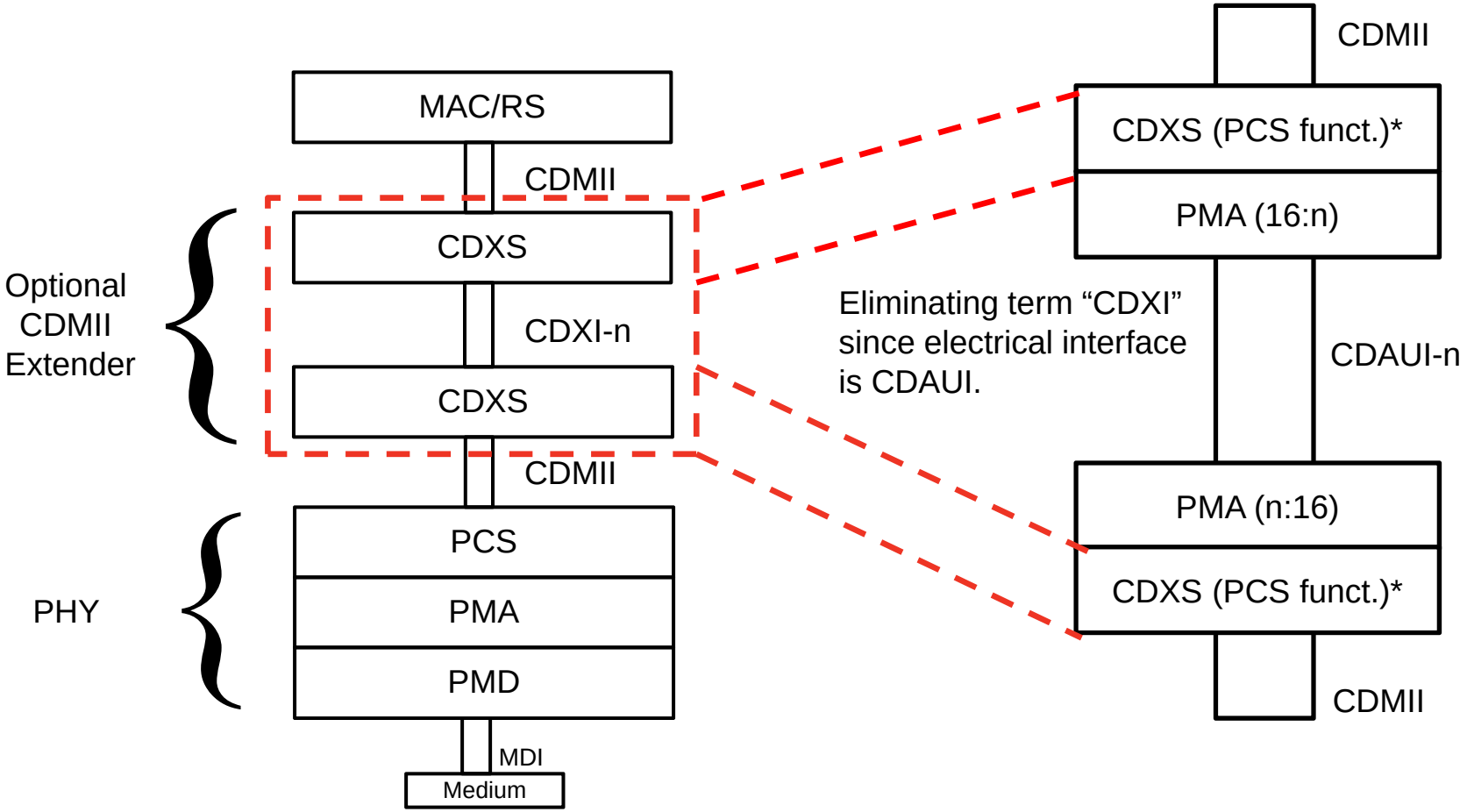
- From gustlin_3bs_02_0115

Comments on CDXS



- CDMII is the only media independent interface
- Different implementations or future PHYs may require changing FEC, which would require a return to CDMII (from a standardization perspective)
- The CDXS, as shown, is an extension of the CDMII.
- This allows support for new PCS / PMA functionality below the extended CDMII, if needed.
- The CDXS provides the coding / FEC of the electrical interface, not the coding / FEC of the PHY.

CDMII Extender Functional Concept

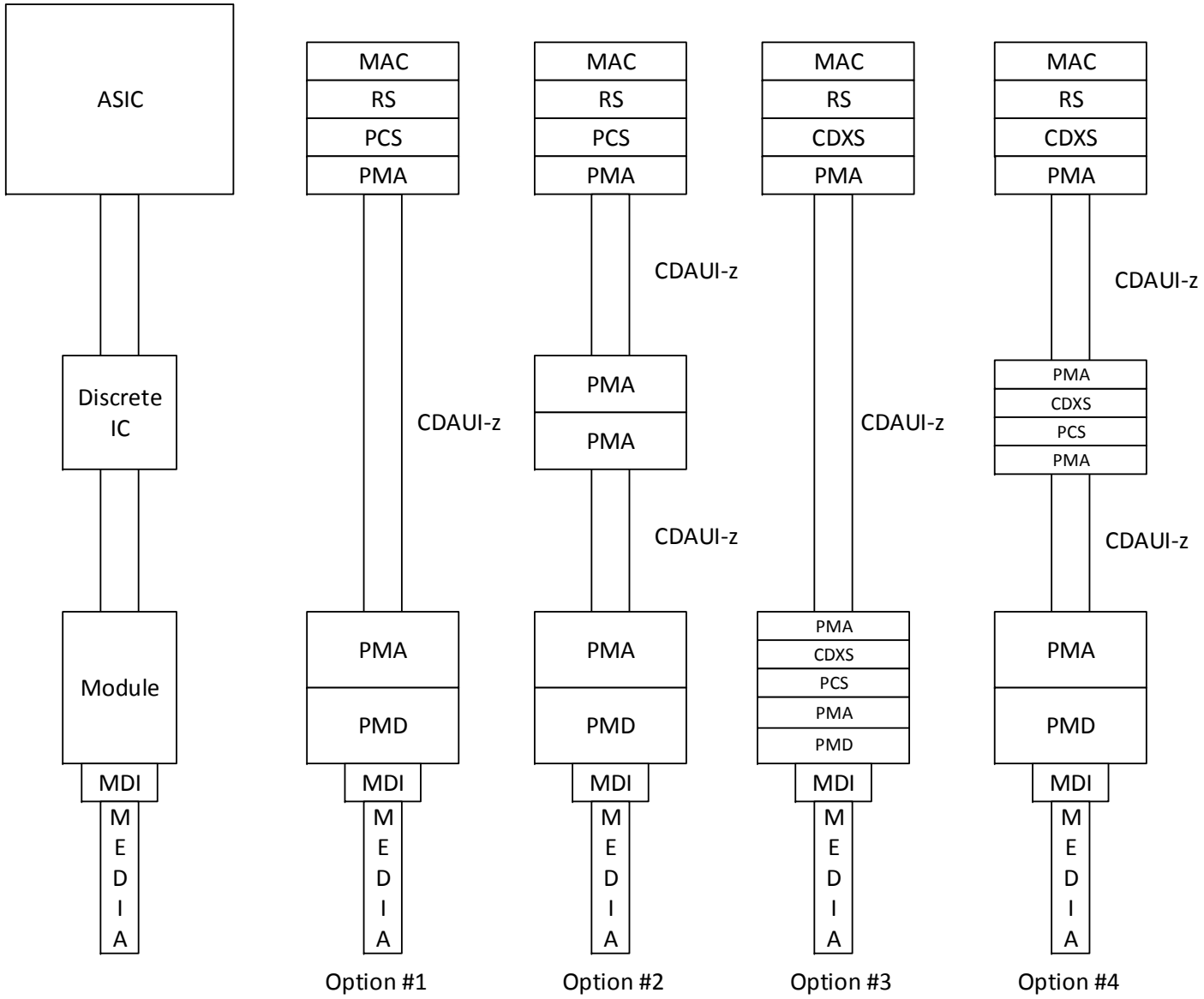


Initial Proposal

Updated Proposal

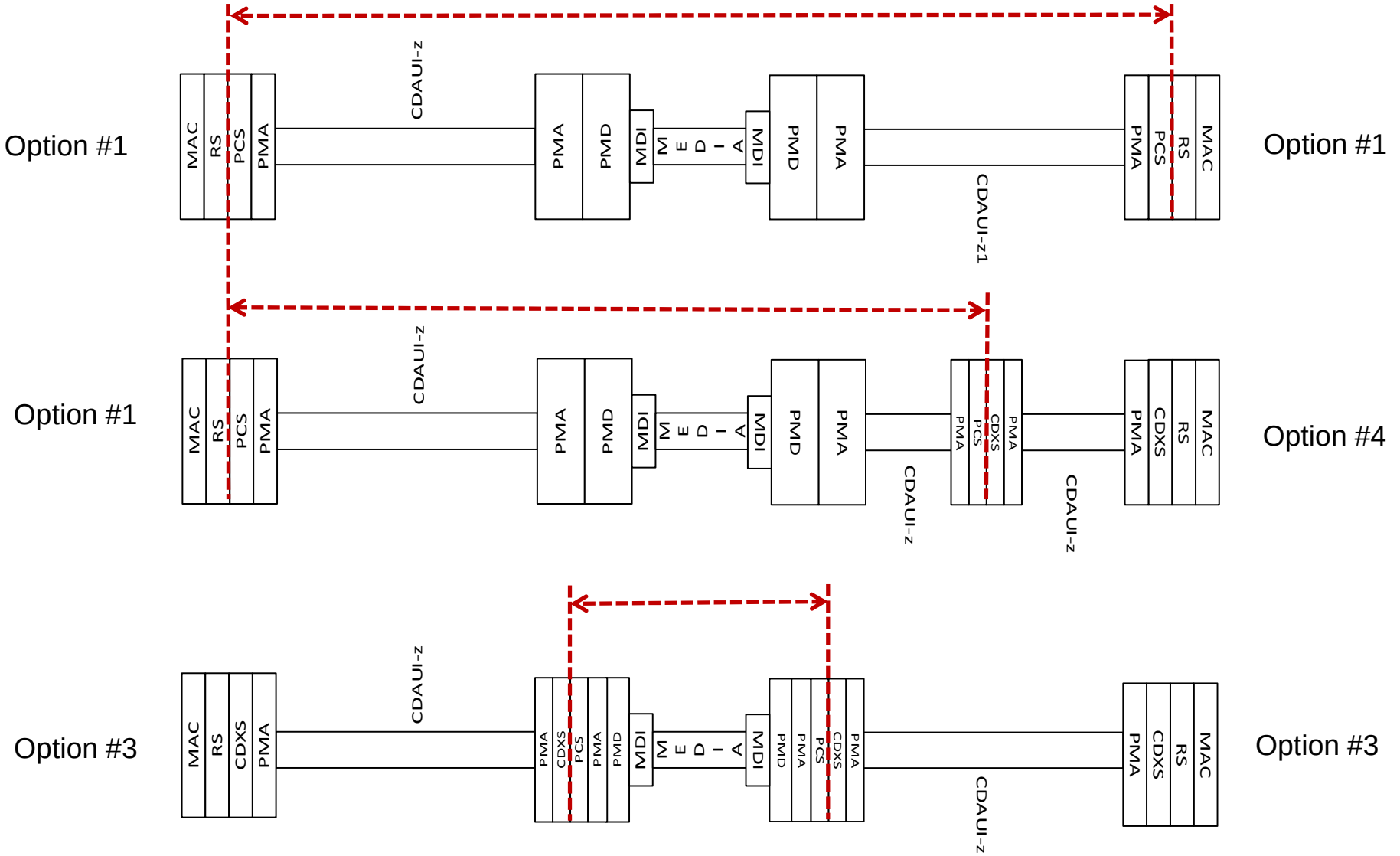
*** Note - Same as PCS (including FEC) to be defined.**

400GbE Example Implementations



"z" may be different for various interfaces cited for CDAUI

Leveraging the Proposed Architecture



Thanks!

400GbE MII Baseline Proposal

IEEE P802.3bs 400 Gb/s Ethernet Task Force

July 2014 San Diego

Mark Gustlin – Xilinx

Supporters

- John D’Ambrosia – Dell
- Arthur Marris – Cadence
- Dave Ofelt – Juniper
- Steve Trowbridge - ALU

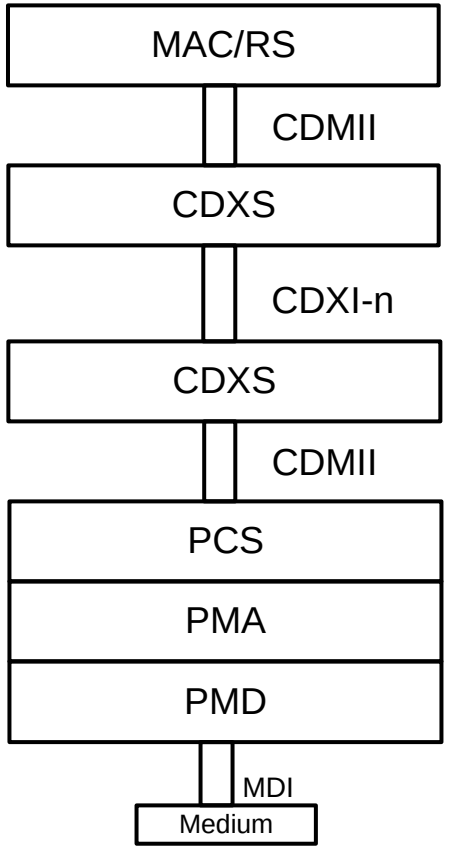
Proposed 400GbE Architecture

- The protocol stack diagram shows one possible implementation
- The CDMII connects the MAC/RS sublayer to the Extender sublayer or the PCS

CDMII is the 400 Gb/s Media Independent Interface

CDXS is the 400 Gb/s extender sublayer

CDXI is the interface between two extender sublayers



CDMII Interface

- Why define it?
  - Electrically it won't be directly instantiated, but in the proposed 400GbE architecture it can be extended with an extender sublayer (CDXS) and interface (CDXI-n)
  - Some will want it for RTL to RTL connections within devices
- Define it as a logical Interface only
  - Unless it is extended, then there is a physical instantiation via an extender sublayer

What is it?

- Base it directly on clause 81
- Same signal structure as shown below, just run faster, or in parallel

81.1.6 XLGMII/CGMII structure

The XLGMII/CGMII is composed of independent transmit and receive paths. Each direction uses 64 data signals (TXD<63:0> and RXD<63:0>), 8 control signals (TXC<7:0> and RXC<7:0>), and a clock (TX_CLK and RX_CLK). Figure 81–2 depicts a schematic view of the RS inputs and outputs.

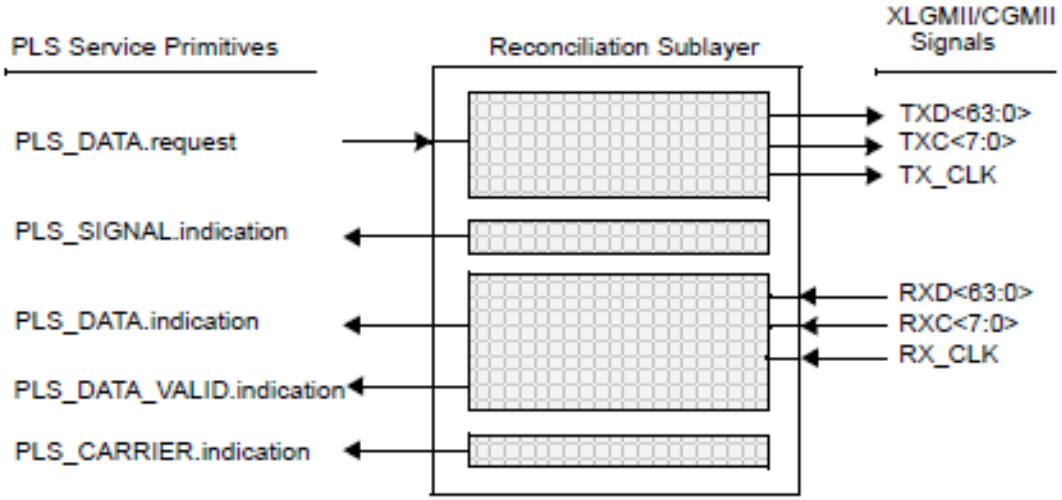


Figure 81–2—Reconciliation Sublayer (RS) inputs and outputs

Extender Sublayer (CDXS)

- The CDXS is the proposed extender sublayer to extend the CDMII
  - A typical instantiation is a high speed parallel SerDes interface
- It is optional, only used if the PCS does not cover both the electrical and optical interface needs
- The CDXS can contain PCS, FEC, and PMA functionality

Thanks!

400GbE PCS and PMA Baseline Proposals

IEEE P802.3bs 400 Gb/s Ethernet Task Force

July 2015 Hawaii

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Don Cober - Comira
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Piers Dawe – Mellanox
Ian Dedic - Socionext
Dan Dove – DNS
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Eric Fortin - ALU
Adam Healey – Avago
Scott Irwin – MoSys
Jonathan Ingham - Avago
Tom Issenhuth - Microsoft
Jonathan King - Finisar
Martin Langhammer - Altera
Scott Kipp – Brocade
Daniel Koehler – MorethanIP
Kenneth Jackson - Sumitomo
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Andy Moorwood – Ericsson
Ed Nakamoto - Spirent
Mark Nowell – Cisco
John Petrilla - Avago
Rick Rabinovich - ALE
Adee Ran – Intel
Sam Sambasivan – ATT
Omer Sella - Mellanox
Ted Sprague – Infinera
Steve Swanson - Corning
Jeff Twombly – Credo Semiconductor
Winston Way - Neophotonics
Brian Welch - Luxtera
Oded Wertheim - Mellanox

References

- This work is based on much of these preceding slide decks/work

http://www.ieee802.org/3/bs/public/15_03/wertheim_3bs_01a_0315.pdf
http://www.ieee802.org/3/bs/public/15_03/wang_t_3bs_01a_0315.pdf
http://www.ieee802.org/3/bs/public/15_03/trowbridge_3bs_01_0315.pdf
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http://www.ieee802.org/3/400GSG/public/13_07/ghiasi_400_01_0713.pdf
http://www.ieee802.org/3/400GSG/public/13_05/ghiasi_400_01a_0513.pdf

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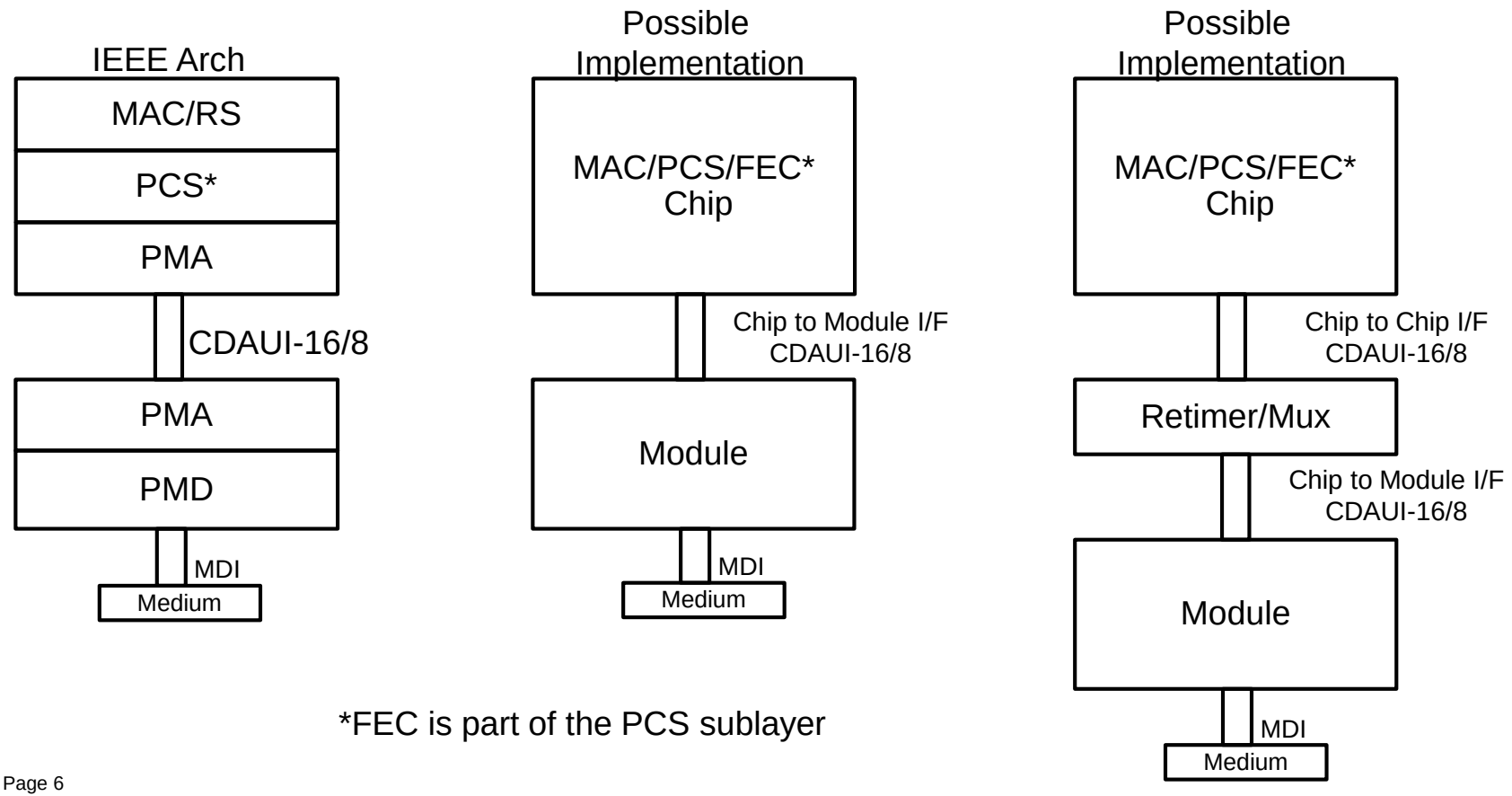
Introduction

- This looks at a baseline PCS and PMA proposal ~~based on a 1x400G FEC architecture~~

PCS Architecture

- Based on the adopted system architecture
- A single FEC is used, across up to 5 interfaces (in the PCS sublayer)
- CDMII is an optional interface that is not shown in these figures, but is already adopted and may be present in a given implementation



*FEC is part of the PCS sublayer

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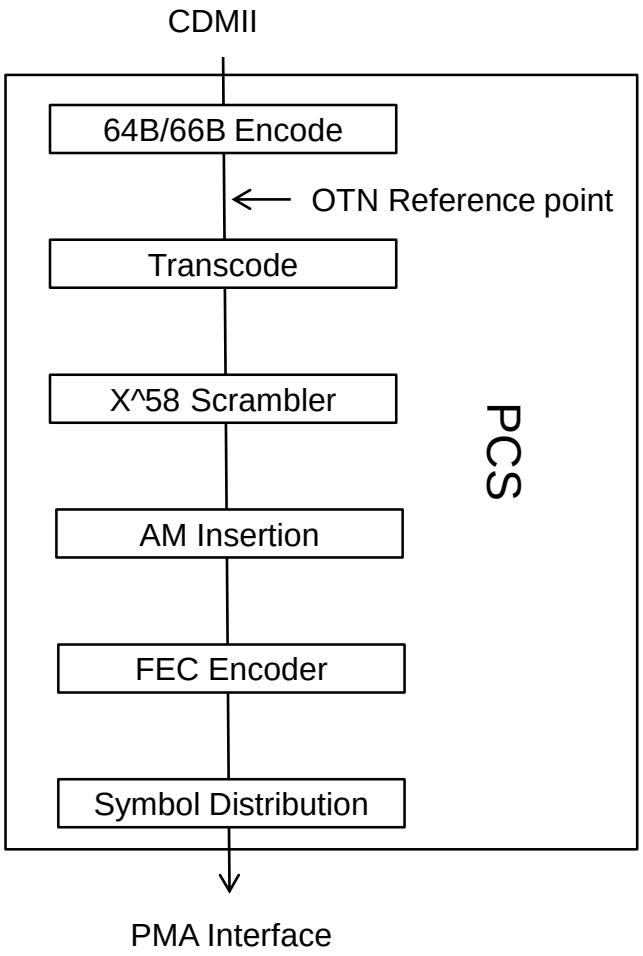
Proposed TX PCS Data Flow

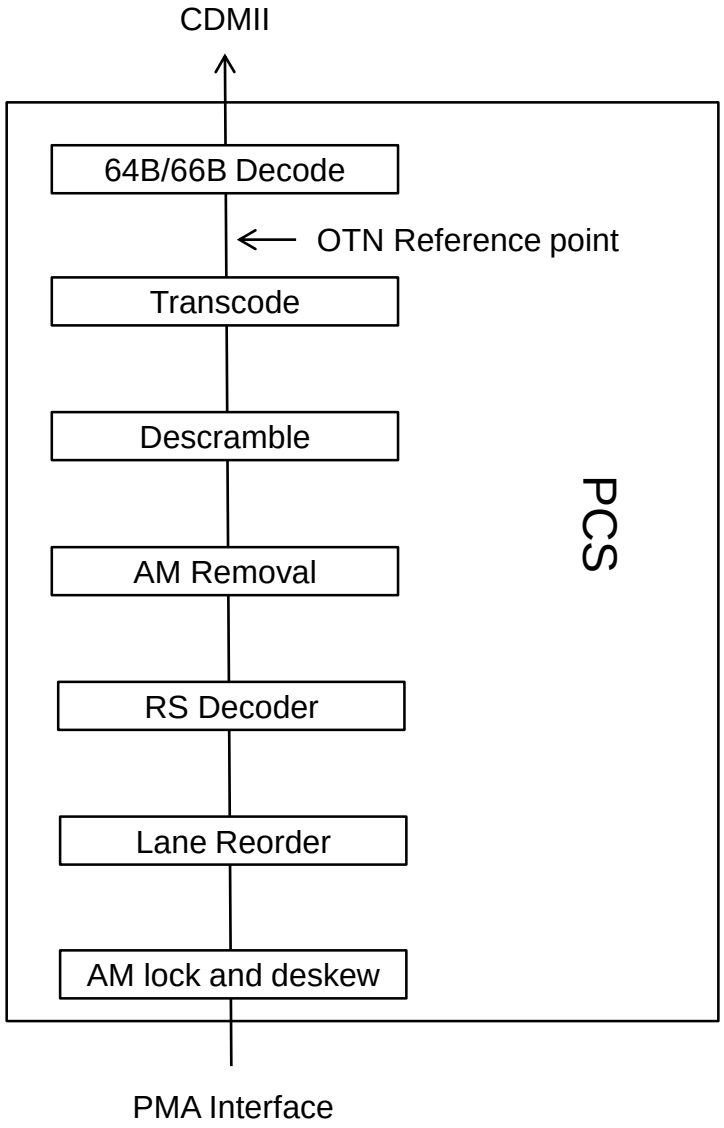
- 64B/66B encode based on clause 82
- Transcode to 256B/257B based on clause 91
- Scrambler is moved to after the Transcoding to simplify the flow
- FEC Encoder is RS(544,514,10), ~~in a 1x400G architecture~~
  - All FEC processing is as in clause 91, including error correction and detection modes
  - Method of forming PCS lanes from FEC codewords is TBD and dependent on further error analysis
- Location of the OTN reference point is as shown and adopted in the January meeting
- Support for any logical lane on any physical lane



Note: Updated and with more detail from what was adopted in dambrosia_3bs_02b_0115.pdf

Proposed RX PCS Data Flow

- Reverse of TX
- Allows for arbitrary lane arrival



Scrambling

- Re-use the X^58 self synchronous scrambler, but after the transcoding
- Run it across all payload information, but not the AMs
- Scrambling includes all 257 bits
  - Note that this is slightly different and simpler than 802.3bj

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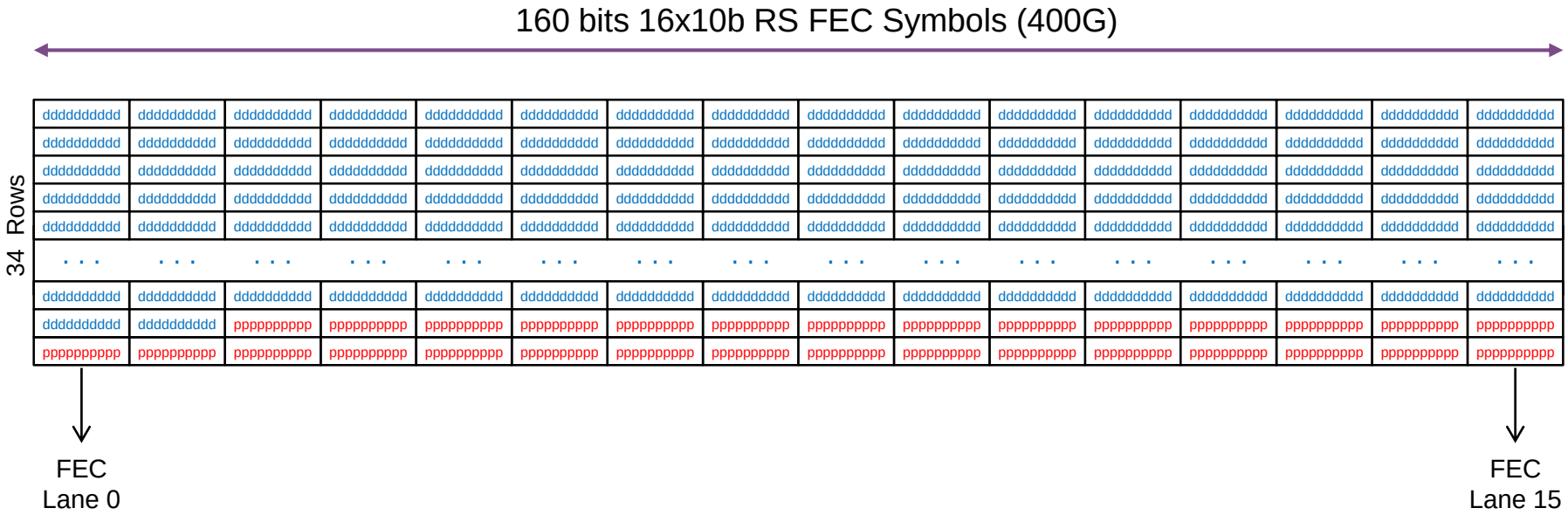
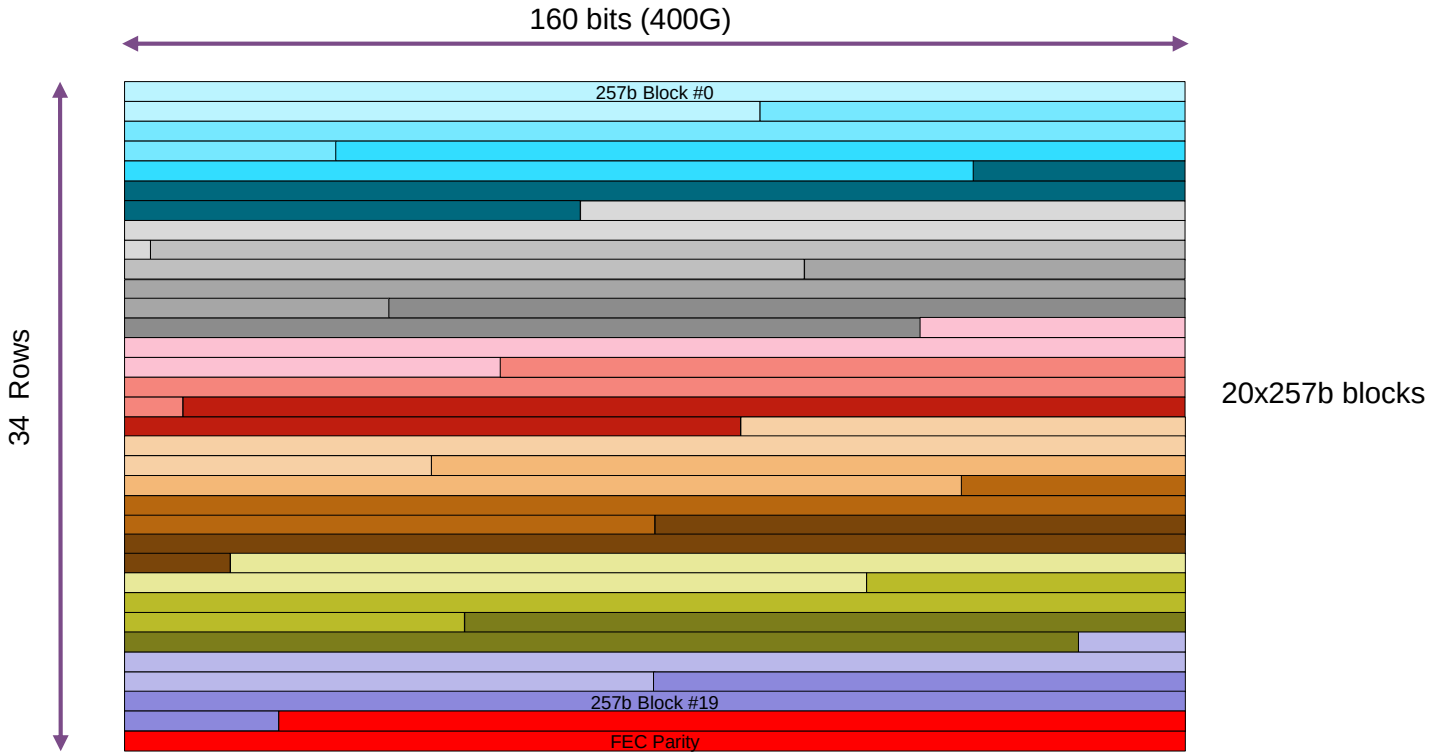
400GbE Data Distribution – 1x400G

- Below the RS-FEC sublayer, using 1x802.3bj KP4 FEC (400G single FEC instance), you would naturally have 16 FEC lanes
  - ddddddddddd = protected data (5140 bits total)
  - ppppppppppp = FEC Parity addition (300 bits total)
  - d + p = 5440 bits total



400GbE 257b Block Mapping

- This shows how the 257b blocks fit within the FEC block



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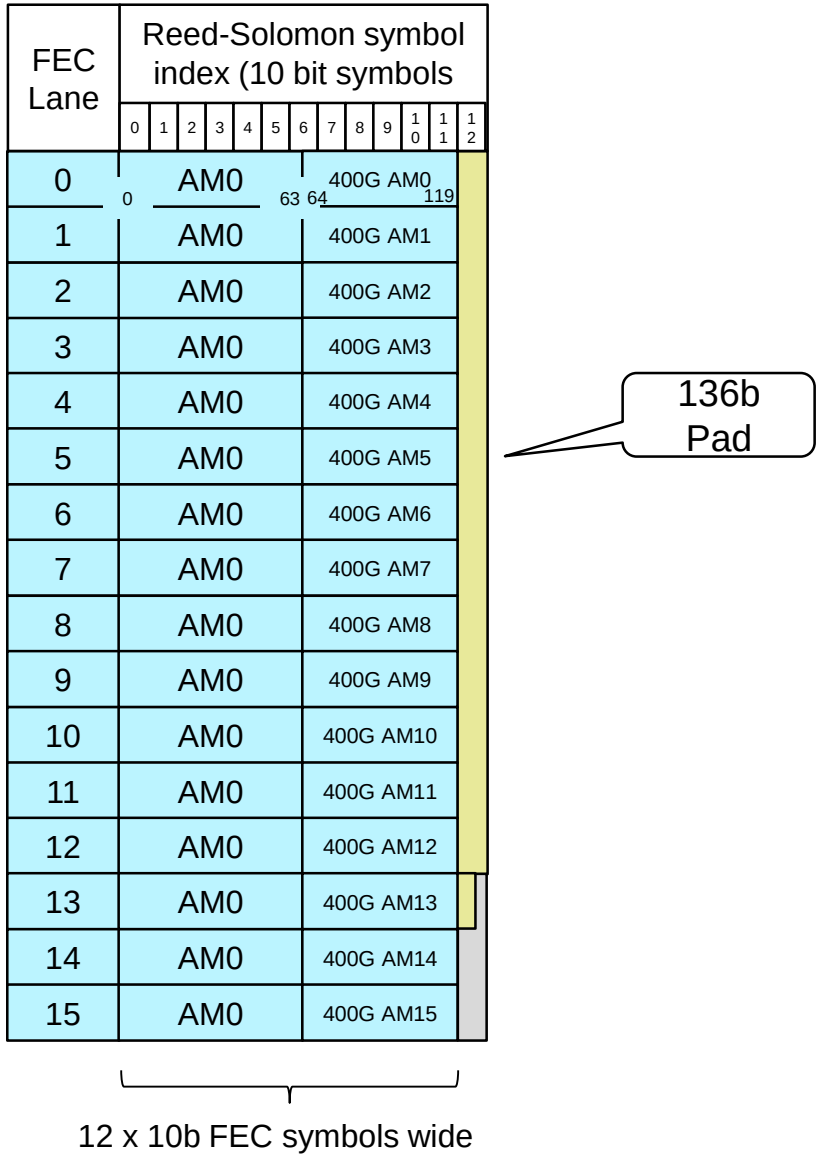
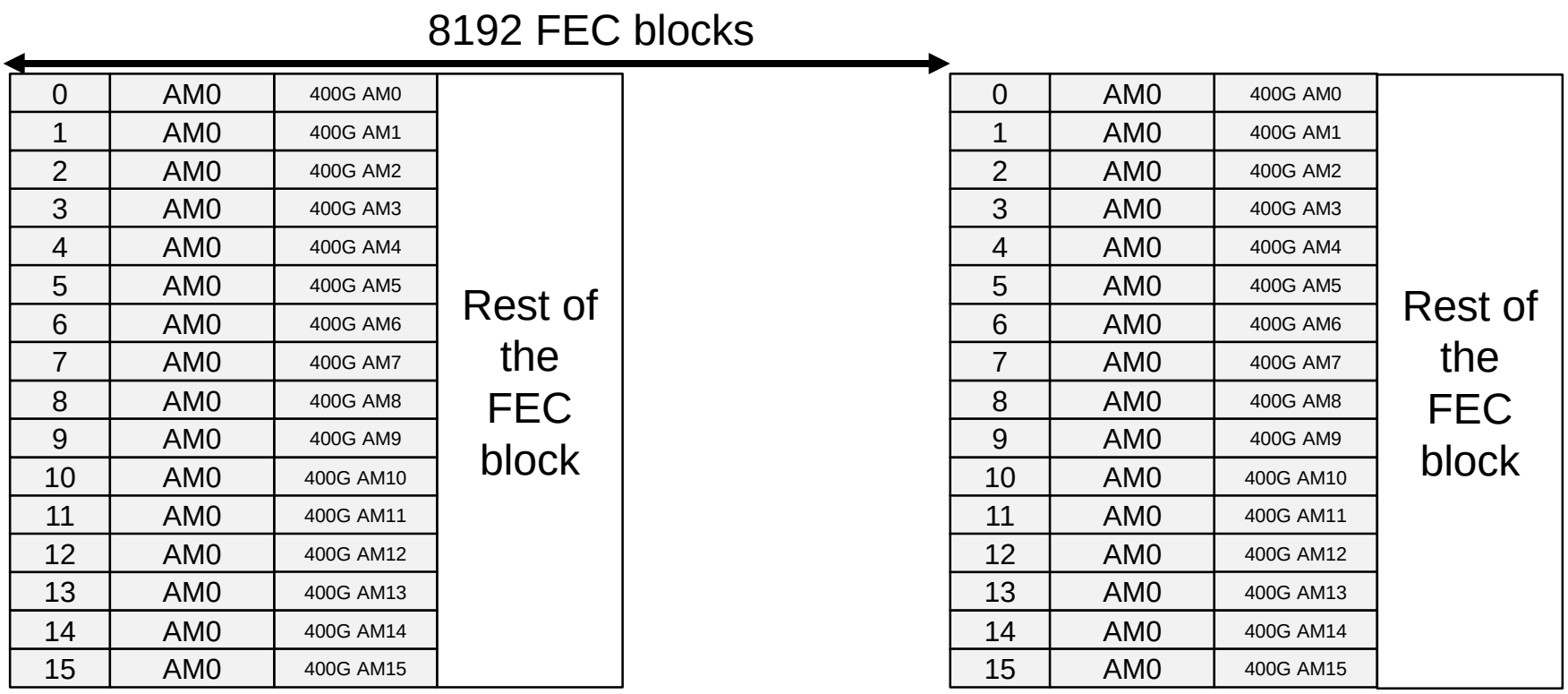
Proposed 400Gb/s AMs

- Re-use 100G AM0 from 802.3ba to allow common block lock between lanes of 100G and 400G, the rest is unique to 400GbE
- Have a 56b 400G unique AM per lane also
  - 56+64 = 120b, putting 120b on each FEC lane after RS symbol distribution requires 8x257b blocks
  - The pad allows us to fit evenly within 8x257b blocks to ease processing
  - Content of 400G AMx is TBD



400 Gb/s AM Distance

- AMs are always aligned to the beginning of an RS-FEC block
- Repetition distance is 8192 FEC blocks (2x 802.3bj)
  - This works out to a little less overhead than we have at 100GbE (~49PPM vs. ~61PPM)



Proposed 400Gb/s AM Detail

- Original AM0 contents: 0xC1, 0x68, 0x21, BIP3, 0x3E, 0x97, 0xDE, BIP7
  - Put what we originally had instead of the BIP fields back in the 802.3ba days
  - 0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B
- 400G AM0, AM1 etc. contents (56b)
  - Create a 28b unique AM field for each marker
  - 2nd 28b is just the bit inversion of the first 28b to keep balance
  - Anything else we need to add in/carry?
- What goes in the 136b pad?
  - Fill in with free running PRBS9 pattern which continues running from frame to frame. X^9+x^5+1

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PMA Functions

- The following are the functions performed by the PMA sublayer
  - Provide appropriate multiplexing
  - Provide appropriate modulation (NRZ/PAM4)
  - Provide appropriate coding as needed
    - Gray coding as appropriate (for the PAM4 electrical interface for instance)
  - Provide per input-lane clock and data recovery
  - Provide clock generation
  - Provide signal drivers when applicable
  - Optionally provide local loopback to/from the PMA service interface
  - Optionally provide remote loopback to/from the PMD service interface
  - Optionally provide test-pattern generation and detection
  - Tolerate Skew Variation
- Not required
  - Extra overhead such as block termination bits or framing for that termination

Note: Updated list from what was adopted in dambrosia_3bs_02b_0115.pdf

PMA Multiplexing

- The PMA will support bit muxing, without regard to skew or PMA lane identity
- Total skew is handled in the RX PCS
  - Skew budgets are TBD (variation and total skew)
  - Skew variation must be handled by PMA instances that do bit muxing, same as in the 802.3ba architecture

PMA Data Rate

- With KP4 FEC the per lane signaling rate is:
  - 544/514*257/256*25G = 26.5625G
  - When running 16 lanes
  - When running 8 lanes it is 53.125G per lane

- PLL multiplier from 156.25MHz is 170 for a 26.5625G lane
- This means that SR16 lanes will run 3% faster than the current SR4 lanes

Testing Concerns

- Propose to continue the use of scrambled idles as the PCS test pattern
  - Defined in clause 82.2.10 and 82.2.17

- Support PCS loopback, TX MII data is looped back to the RX MII and transmitted towards the PMA

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Work Items

- Hi BER, use FEC thresholds?
- Sublayer delay constraints are TBD, same with skew limitations
- Define 400G AM fields
- Precoding?
- Exact criteria for achieving AM lock

Conclusion

- This proposal implements the adopted RS(544,514,10) as the FEC in the 802.3bs 400GbE PCS ~~using a 1x400GbE architecture~~
- Additional PMA details are included, including a bit muxing architecture

Thanks!

Baseline Proposal for CDAUI-8 Chip-to-Chip (c2c)

For IEEE 802.3bs

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* Changes since *li_3bs_01_0115* shown in red

Purposes

- Present a PAM4 baseline specification proposal for CDAUI-8 c2c electrical interface in support of the 400 GbE to fulfill its objective of:

  Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

Technology Choice Highlights 1

- Channel target/requirement based on the equation of the following:
  - IL <= { 1.083 + 2.543SQROOT(f) + 0.761f 0.01 <= f <= 28.05GHz} dB

  as the informative insertion loss equation adopted by 802.3bs in Jan/2015 meeting
- Channel equalization based on a transceiver having TX FIR, RX CTLE and DFE

Technology Choice Highlights 2

- Raw BER of CDAUI-8 link to be < 1E-6; FEC brings link system BER to < 1E-15

Technology Choice Highlights 3

- Leverage the 100GBASE-KP4 (i.e., KP4) specification from 13.59 GBd to 26.5625 GBd, and is consistent with CEI-56G-MR specification draft[1]
- Gray-code proposed, FEC (capable of bringing raw BER from 1e-6 to < 1e-15) assumed. FEC and pre-coding (if needed) specifics be defined by the FEC ad hoc
- Reuse KP4 test patterns, TX and RX methodologies for specifying electrical characteristics and corresponding tests
- Reuse CAUI-4 TX and RX diff and CM RLs, compliance point definitions (i.e., TP0a and TP5a)
- Reuse CAUI-4 link adaptation method (i.e., CL 83D.3.3.2 and 45)
- Reuse/improve 802.3bj COM method channel compliance with PAM4 signaling

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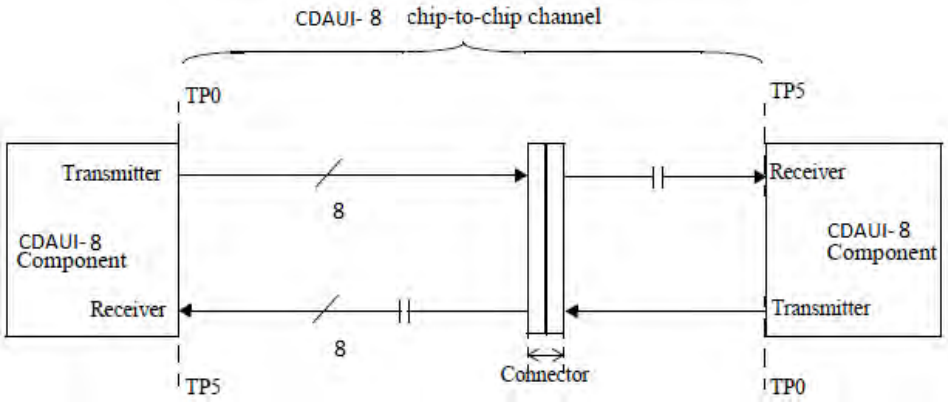
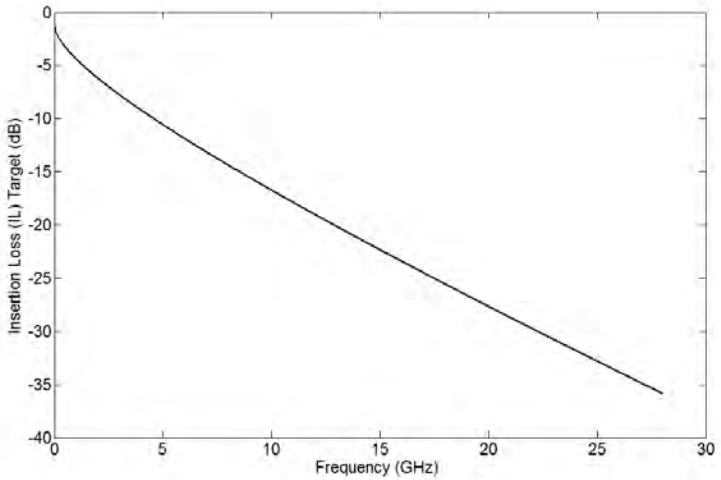
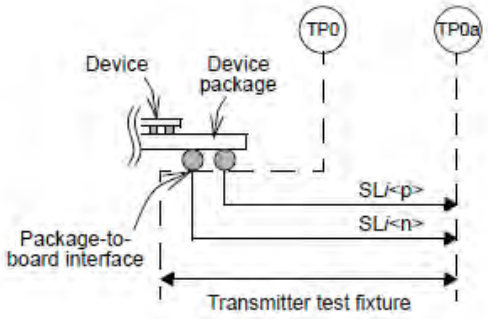
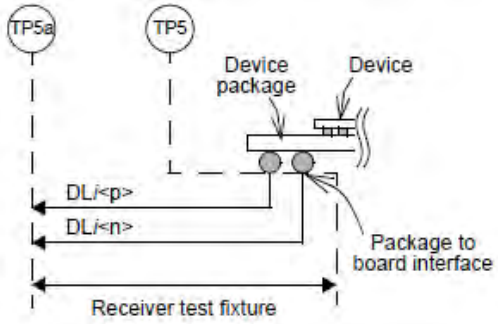
CDAUI-8 c2c Link Topology and IL Target



Informative target Max IL







- CDAUI-8 c2c compliance point definitions are the same as those defined in clause 83D.2 (CAUI-4)

CDAUI-8 c2c Functional Spec

- CDAUI-8 PMA functional spec will be largely base on reusing, extending/modifying Clauses 94.2.2 (TX), 94.2.3 (RX), including
  - FEC interface
    - KP4 FEC, i.e., RS(544, 514, 10)
  - Gray mapping
  - PAM4 encoding
  - Precoding
    - Pending, the need and specifics ought to be studied and determined in the FEC ad hoc

CDAUI-8 c2c Test Patterns

- CDAUI-8 PMA will reuse test patterns defined in clause 94.2.9, including:
  - JP03A test pattern
  - JP03B test pattern
  - Quaternary PRBS13 test pattern (with the termination block (i.e., 94.2.2.4) removed, this will need to be changed accordingly)
  - Transmitter linearity test pattern

CDAUI-8 c2c TX Spec

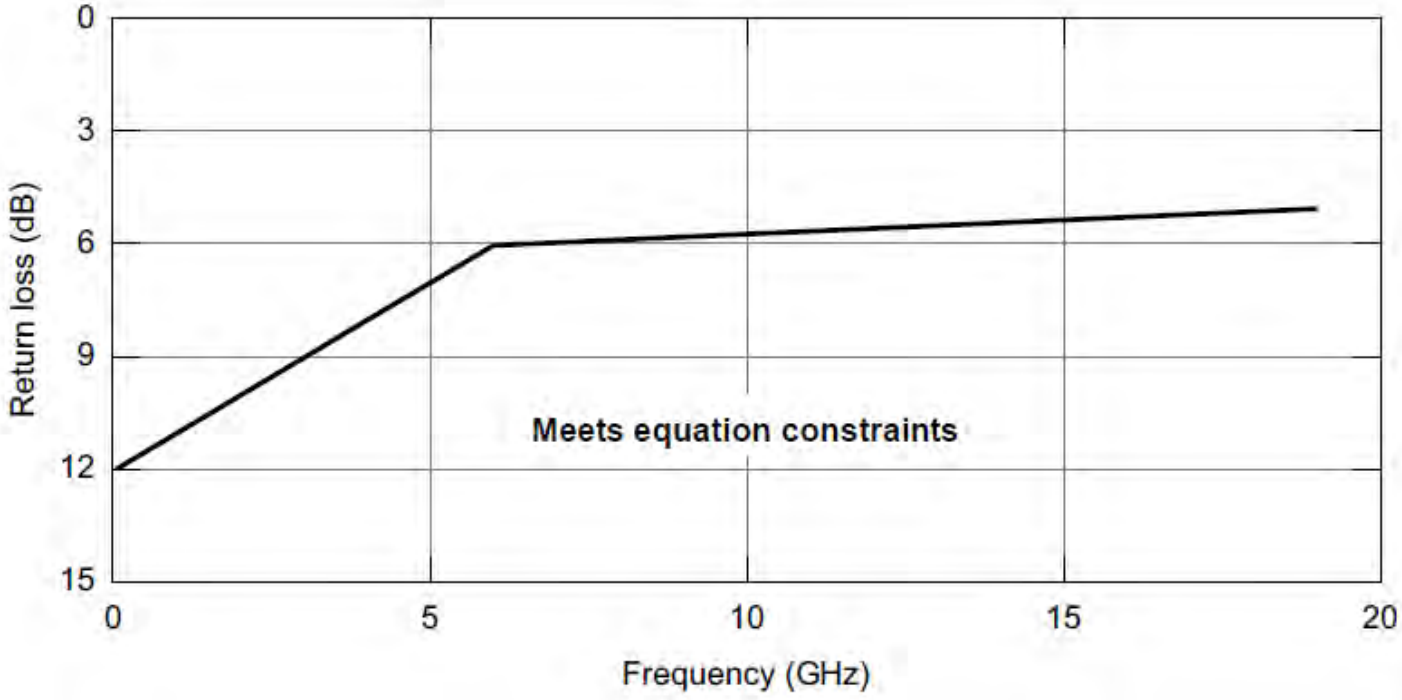
Parameter	Subclause reference	Value	Units
Signaling rate		26.5625	Gsym/s
Differential peak-to-peak output voltage (max.) Transmitter disabled Transmitter enabled		 30 1200	 mV mV
DC common-mode output voltage (max.)		1.9	V
DC common-mode output voltage (min.)		0	V
AC common-mode output voltage (RMS, max.)		30	mV
Differential output return loss (min.)		Eq. 17-4	dB
Common-mode output return loss (min.)		Eq. 17-5	dB
Output waveform Level separation mismatch ratio RLM(min) Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)		 0.92 0.6 0.4 0.80 × v_f 0.0083 0.05 1.54 4	 — V V V — — — —
Output jitter and linearity Clock random jitter, RMS (max.) Clock deterministic jitter, pp (max.) Even-odd jitter (max.) Signal-to-noise-and-distortion ratio (min.)		 0.01 0.04 0.019 31	 UI UI UI dB

- TX output waveform definition and test method will reuse clause 94.3.12.5
- TX output jitter definition and test method will reuse clause 94.3.12.6
- TX output noise and distortion definition and test method will reuse clause 94.3.12.7

* Updated to be aligned/consistent with *healey_3bs_01_0315*

CDAUI-8 c2c TX Diff RL Spec

$$RL_d(f) \geq \begin{cases} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB}$$



- Reuse Eq. (93-3) and Fig (93-7)

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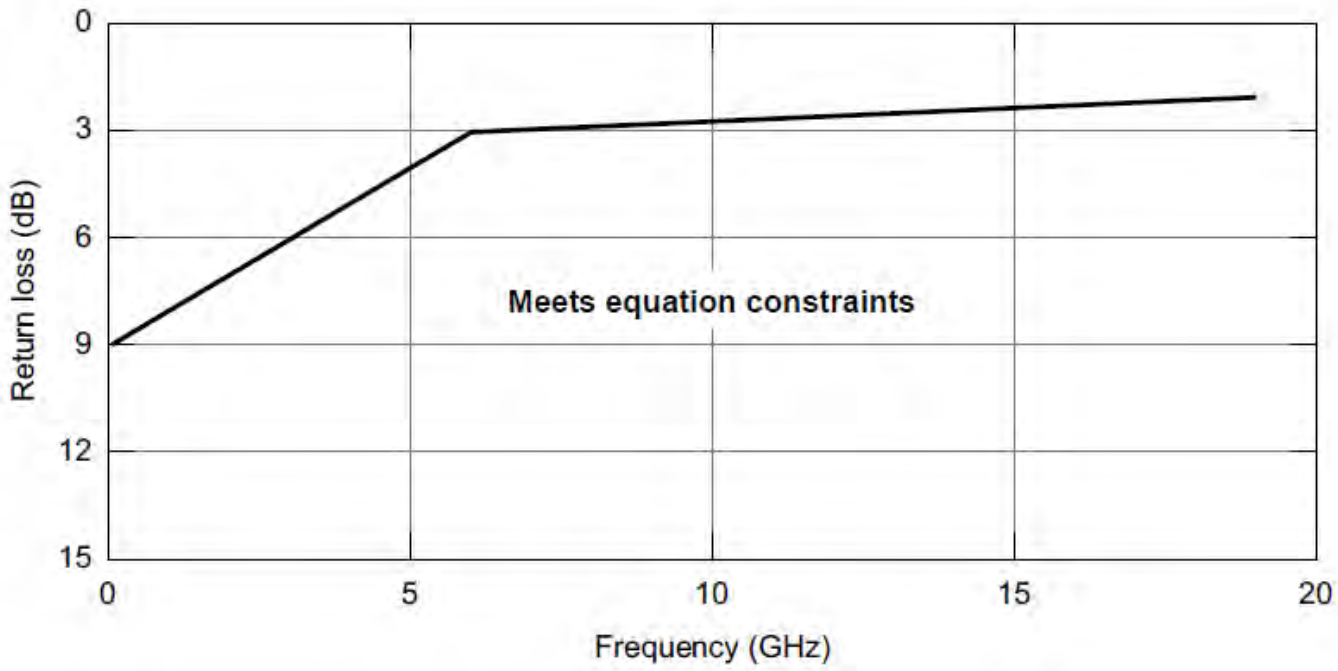
CDAUI-8 c2c TX CM RL Spec

$$RL_{cm}(f) \geq \begin{cases} 9.05 - f & 0.05 \leq f \leq 6 \\ 3.5 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB}$$



- Reuse Eq. (93-4) and Fig (93-8)

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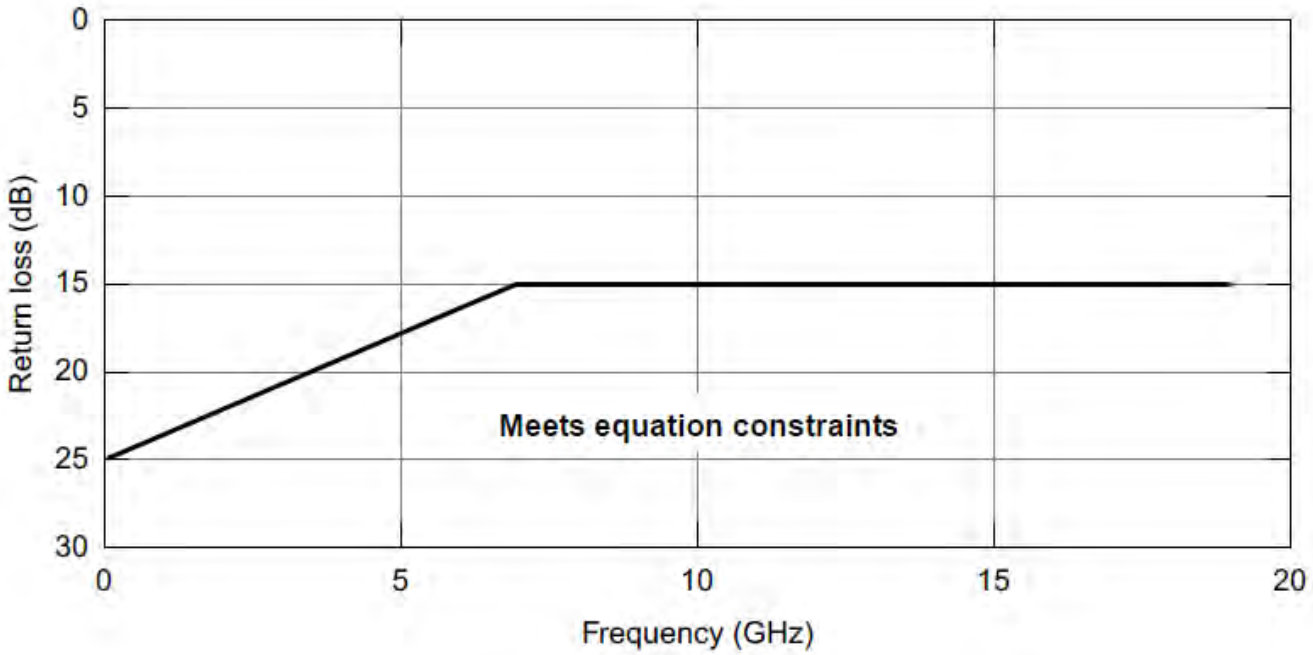
CDAUI-8 c2c RX Spec

Parameter	Symbol	Value	Units	Conditions
Differential Input Return Loss		Slide 11	dB	
Differential to Common-Mode Return Loss		Slide 14	dB	
Interference Tolerance		Slide 15	-	
Jitter Tolerance		Slide 16	-	

CDAUI-8 c2c RX D2C RL Spec

$$RL_{cd}(f) = \left\{ \begin{array}{ll} 25 - 1.44f & 0.05 \le f \le 6.95 \\ 15 & 6.95 < f \le 19 \end{array} \right\} \text{ dB}$$



- Reuse Eq. (93-5) and Fig (93-11)

CDAUI-8 c2c RX Interference Tolerance Parameters

Parameter	Test 1 values			Test 2 values			Units
	Min	Max	Target	Min	Max	Target	
Symbol error ratio[a]	—	10^{-5}		—	10^{-5}		—
Insertion loss at 13.2813 GHz [b]	19.5	20.5		9.5	10.5		dB
Coefficients of fitted insertion loss [c] a0 a1 a2 a4	 −1 0 0 0	 2 2.937 1.599 0.03		 −1 0 0 0	 1 0.817 0.801 0.01		 dB dB/GHz $^{1/2}$ dB/GHz dB/GHz ^{2}
RSS_DFE4 [d]	0.05	—		0.025	—		—
COM including effects of broad- band noise	—	—	2	—	—	2	dB

[a] The FEC symbol error ratio is measured in step 11 of the receiver interference tolerance method defined in 93C.2

[b] Measured between TPt and TP5 (see Figure 93C-4)

[c] Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with fmin = 0.05 GHz, and fmax = 26.5625. GHz, and maximum Δf = 0.01 GHz

[d] RSS_DFE4 is described in 93A.2.

- Largely re-use of Table 83D-5 and method in 94.3.13.3

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CDAUI-8 c2c RX Jitter Tolerance Parameters

Parameter	Case A values	Case B values	Units
Max Pre-FEC BER	1e-6	1e-6	
Jitter frequency	fb/849600	fb/8496	same as fb
Jitter Amplitude	5	0.05	UI

- Largely re-use method in 94.3.13.4
- fb is the BAUD rate

CDAUI-8 c2c Channel Spec: COM (I)*

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface	 C_d z_p z_R C_p	 TBD 12 30 TBD	 nF mm mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	TBD	Ω
Receiver 3 dB bandwidth	f_r	0.75 × f_b	
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.60	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –15 0 1	 dB dB dB
Continuous time filter, zero frequency	f_z	f_b / 4	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 4 f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V

* Updated to be aligned/consistent with *healey_3bs_01_0315*

CDAUI-8 c2c Channel Spec: COM (II)

Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.92	—
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit for n = 1 for n = 2 to N_b	$b_{max}(n)$	1 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	—

* Updated to be aligned/consistent with *healey_3bs_01_0315*

Summary

- A baseline proposal based PAM4 signaling for CDAUI-8 c2c electrical interface specification has been developed
  - Intent is to support existing CAUI-4 c2c channel and testing infrastructures
  - Reused/extended/modified from 100GBase-KP4 and CAUI-4 c2c specifications (i.e., clauses 94, 93A, and 83D)
  - Consistent with CEI-56G-MR adopted baseline specification in modulation and in general

References

[1] oif2014.245.01, www.oiforum.com

(That document was provided as an attachment to the October 28, 2014 liaison from OIF to IEEE 802.3. The liaison and its attachments can be found in the IEEE P802.3bs 400 Gb/s Ethernet Task Force private area)

Baseline Proposal for CDAUI-8 Chip-to-Module (c2m)

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Brian Welch, Luxtera
Helen Xu, Huawei
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* Changes since *brown_3bs_01a_0115* shown in red

Purpose

- Present a baseline specification proposal for CDAUI-8 c2m electrical interface in support of the 400 GbE Task Force to fulfill its objective of:

  Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

*

Technology Choice Highlights 1

- Channel target/requirement based on the following equation:

  IL <= { 1.076(0.075 + 0.537SQROOT(f) + 0.566f) 0.01 <= f <= 28.05GHz} dB

  as the informative insertion loss adopted by 802.3bs at the Jan/2015 Interim meeting

- Channel equalization based on a transceiver having autonomous Rx CTLE
  - Tx FIR or Rx DFE not specified in host or module transceivers. (Allowed, but not mandated.)

Technology Choice Highlights 2

- Raw BER of CDAUI-8 c2m link to be < 1e-6; FEC brings link system BER to < 1e-15

Technology Choice Highlights 3 *

- Leverage the CEI-56G-VSR-PAM4 draft specification[1] using one data rate:
  - 26.5625GBd
- Gray-code specified, FEC assumed but not specified
- Pre-coding not assumed since CTLE-only
- Reuse CAUI-4 c2m Tx and Rx methodologies for specifying electrical characteristics and corresponding tests
  - Diff and CM RLs and compliance point definitions
  - HCB/MCB method for channel compliance, adapted for PAM-4 signaling
  - Remove “recommended CTLE” mechanism

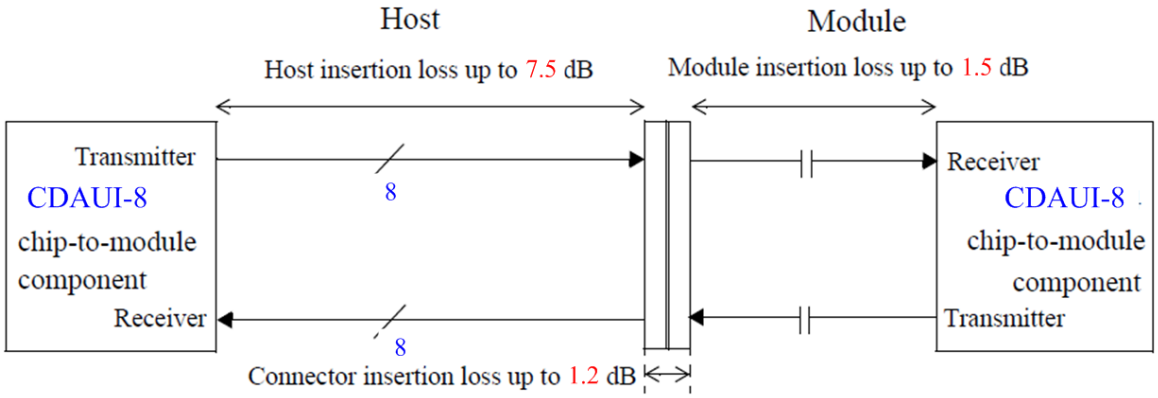
CDAUI-8 Chip-to-Module Link *

	CAUI-4 (83E.3.1 TP1a)	VSR 56G (15.3.2, TP1a)	CDAUI-8 Chip-Module Potential
Modulation	NRZ	PAM-4 (Gray coded)	PAM-4 (Gray coded)
Nominal Signaling Rate (each lane)	25.78125 Gb/s +/- 100 ppm	19.6 ≤ fb ≤ 30 GBd	26.5625 GBd +/- 100 ppm ~~28 GBd (TBD)[a] +/- 100 ppm~~
Unit Interval	38.787879 ps	33.33 ps - 51 ps	37.647059 ps ~~35.65 ps (TBD)[a]~~
Loss Budget, max[b]	10 dB	10.8 dB[c]	10.3 dB
Uncorrected BER	< 1e-15	< 1e-6	< 1e-6
Corrected BER	n/a	n/a	< 1e-15

~~[a] Two operating signaling rates, with choice of higher rate pending PMA FEC selection.~~

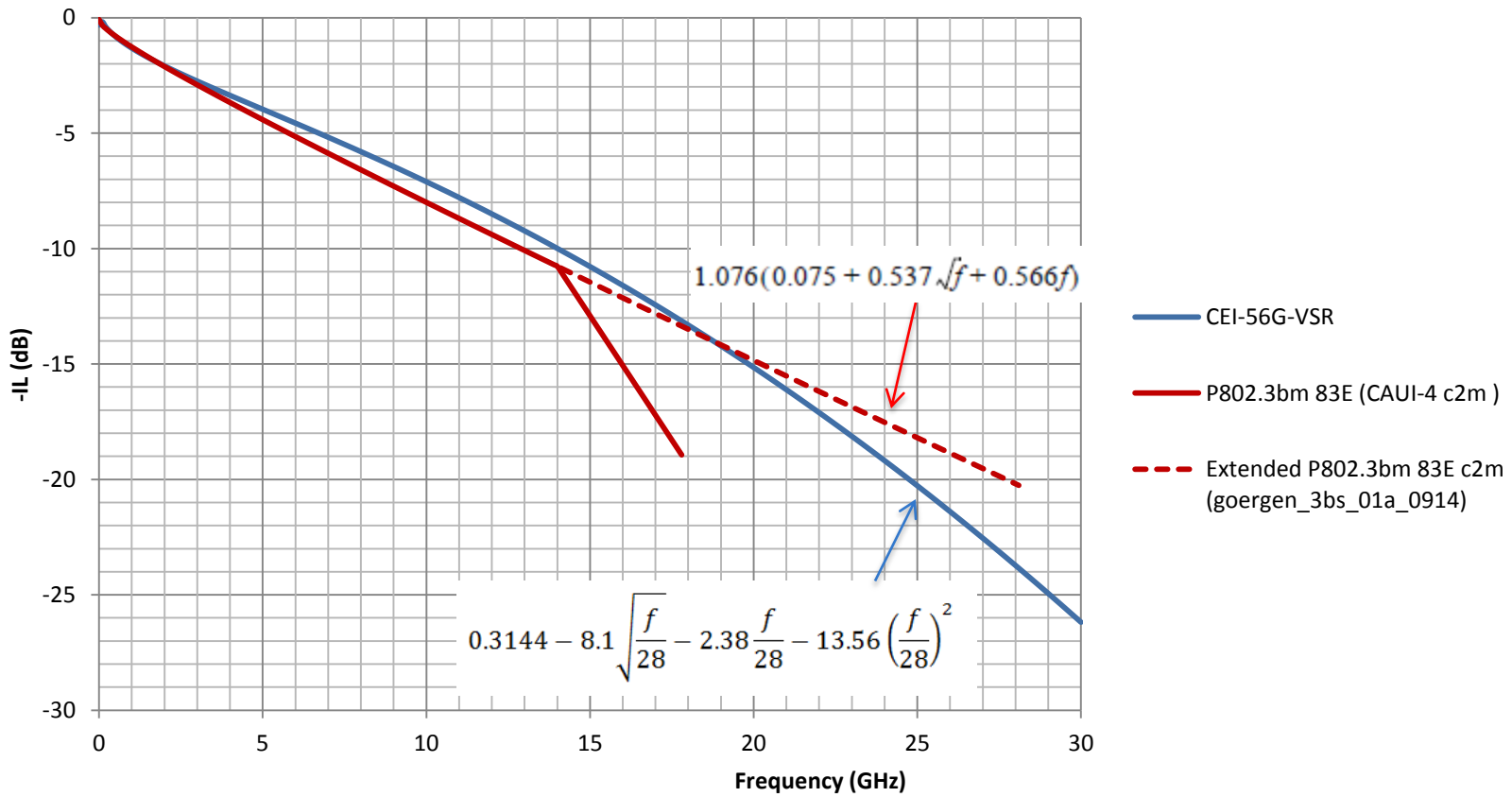
[b] At 1/2 symbol rate, comprising host PCB trace, module PCB trace, AC-coupling capacitors and one connector.

[c] Informative.



Chip-to-module insertion loss budget at 13.28 GHz

CDAUI-8 c2m PAM4 Channel Insertion Loss *



- Target IL curve is “extended CAUI-4 c2m” as adopted at Jan/2015 Interim
  - Loss at Nyquist (13.28GHz) = 10.27 dB
  - Working assumption: all IL curves shown are suitable for PAM4 signaling at 28GBd
  - Consider potential to operate over legacy CAUI-4 c2m channels

CDAUI-8 Host Transmitter

	CAUI-4 (83E.3.1 TP1a)	VSR 56G (15.3.2, TP1a)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak output voltage (max) with Tx enabled	900 mV	900 mV	900 mV
AC common-mode output voltage (max)	17.5 mVrms	17.5 mVrms	17.5 mVrms
Differential peak-to-peak output voltage (max) with Tx disabled	35 mV	-	35 mV
Differential termination mismatch (max)	10 %	10 %	10 %
Differential output return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Common-mode to differential output return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Common-mode output return loss (min)	-	2 dB	2 dB
DC common-mode output voltage (max)	2.8 V	2.8 V	2.8 V
DC common-mode output voltage (min)	-0.3 V	-0.3 V	-0.3 V
Eye Width (min)	0.46 UI at 1e-15	0.25 UI at 1e-6 applicable to all three PAM4 eyes	0.25 UI at 1e-6 applicable to all three PAM4 eyes
Output total jitter (max)	TJ: 0.54UIpp @ 1e-15 Measured using CTLE	TJ: 0.75UIpp @ 1e-6 Measured using CTLE	TJ: 0.75UIpp @ 1e-6 Measured using CTLE
Eye Height (min)	95 mV at 1e-15	50 mV at 1e-6 applicable to all three PAM4 eyes	50 mV at 1e-6 applicable to all three PAM4 eyes
Transition time (min, 20/80%)	10 ps	-	-

CDAUI-8 Module Receiver

	CAUI-4 (83E.3.1 TP1)	VSR 56G (15.3.2, TP1)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak input voltage tolerance (min)	900 mV	900 mV	900 mV
Single-ended voltage tolerance range (min)	-0.4 to 3.3 V	-	-
DC common-mode input voltage (max)	2.85 V	2.85 V	2.85 V
DC common-mode input voltage (min)	-0.35 V	-0.35 V	-0.35 V
Differential termination mismatch (max)	10 %	10 %	10 %
Differential input return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Differential to common mode input return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Module stressed input test	83E.3.4.1	15.3.10.2.1	Same as VSR

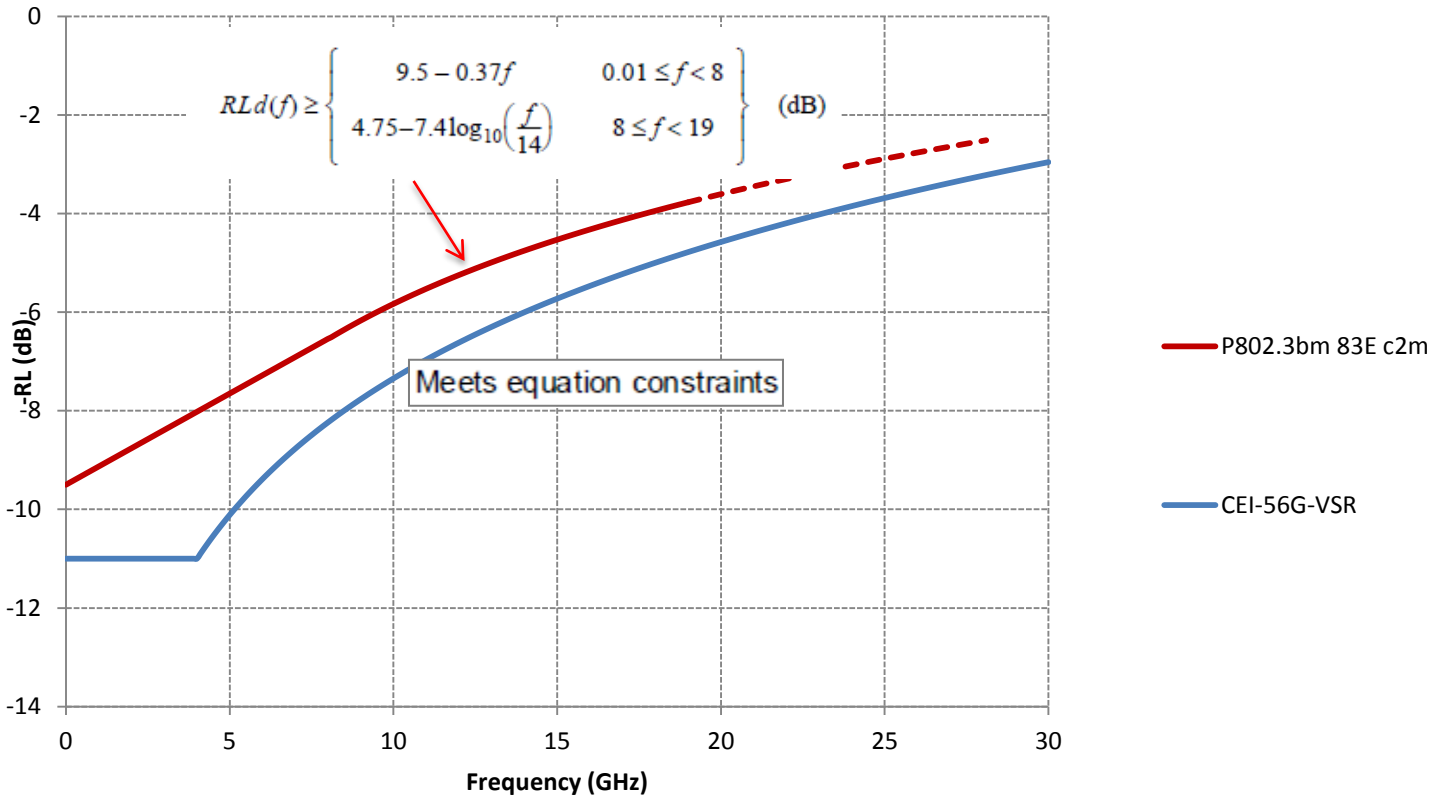
CDAUI-8 Module Transmitter

	CAUI-4 (83E.3.2 TP4)	VSR 56G (15.3.3, TP4)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak output voltage (max) with Tx enabled	900 mV	900 mV	900 mV
AC common-mode output voltage (max)	17.5 mVrms	17.5 mVrms	17.5 mVrms
Differential termination mismatch (max)	10 %	10 %	10 %
Differential output return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Common-mode to differential mode output return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Common-mode output return loss (min)	-	2 dB	2 dB
DC common-mode output voltage (max)	2.85 V	2.85 V	2.85 V
DC common-mode output voltage (min)	-0.35 V	-0.35 V	-0.35 V
Vertical Eye Closure (max)	5.5 dB	5.8 dB	5.8dB
Eye Width (min)	0.57 UI at 1e-15	0.4 UI at 1e-6 applicable to all three PAM4 eyes	0.4 UI at 1e-6 applicable to all three PAM4 eyes
Output total jitter (max)	TJ: 0.43UIpp @ 1e-15 Measured using CTLE	TJ: 0.6UIpp @ 1e-6 Measured using CTLE	TJ: 0.6UIpp @ 1e-6 Measured using CTLE
Eye Height (min)	228 mV at 1e-15	120 mV at 1e-6 applicable to all three PAM4 eyes	120 mV at 1e-6 applicable to all three PAM4 eyes
Transition time (min, 20/80%)	12 ps	-	-

CDAUI-8 Host Receiver

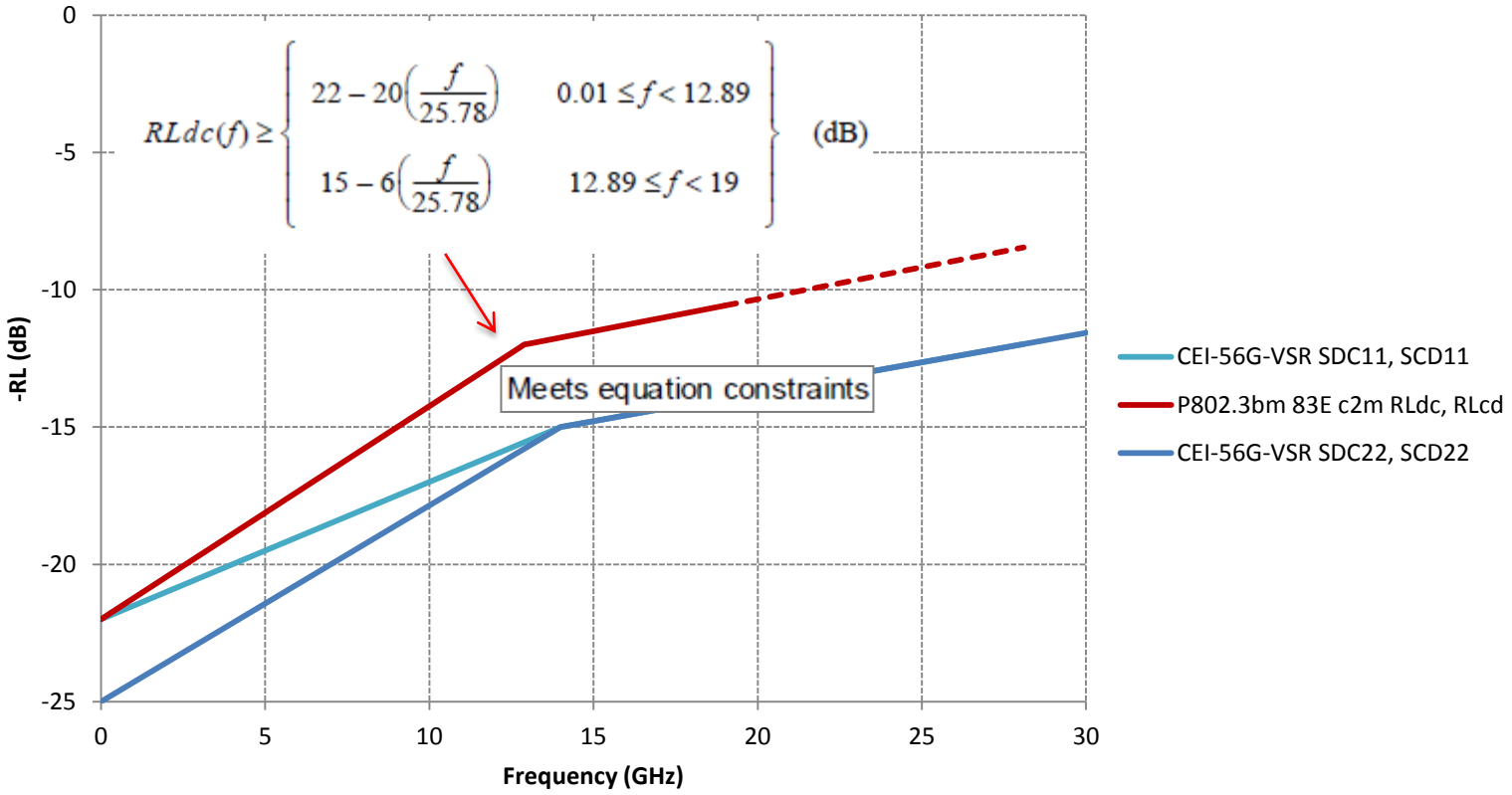
	CAUI-4 (83E.3.2 TP4a)	VSR 56G (15.3.2, TP4a)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak input voltage tolerance (min)	900 mV	900 mV	900 mV
DC common-mode input voltage (max)	2.8 V	2.8 V	2.8 V
DC common-mode input voltage (min)	-0.3 V	-0.3 V	-0.3 V
Differential termination mismatch (max)	10 %	10 %	10 %
Differential input return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Differential to common-mode input return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Host stressed input test	83E.3.3.2	15.3.10.2.1	Same as VSR
Jitter tolerance	-	-	-

CDAUI-8 c2m Tx & Rx Differential Return Loss Spec



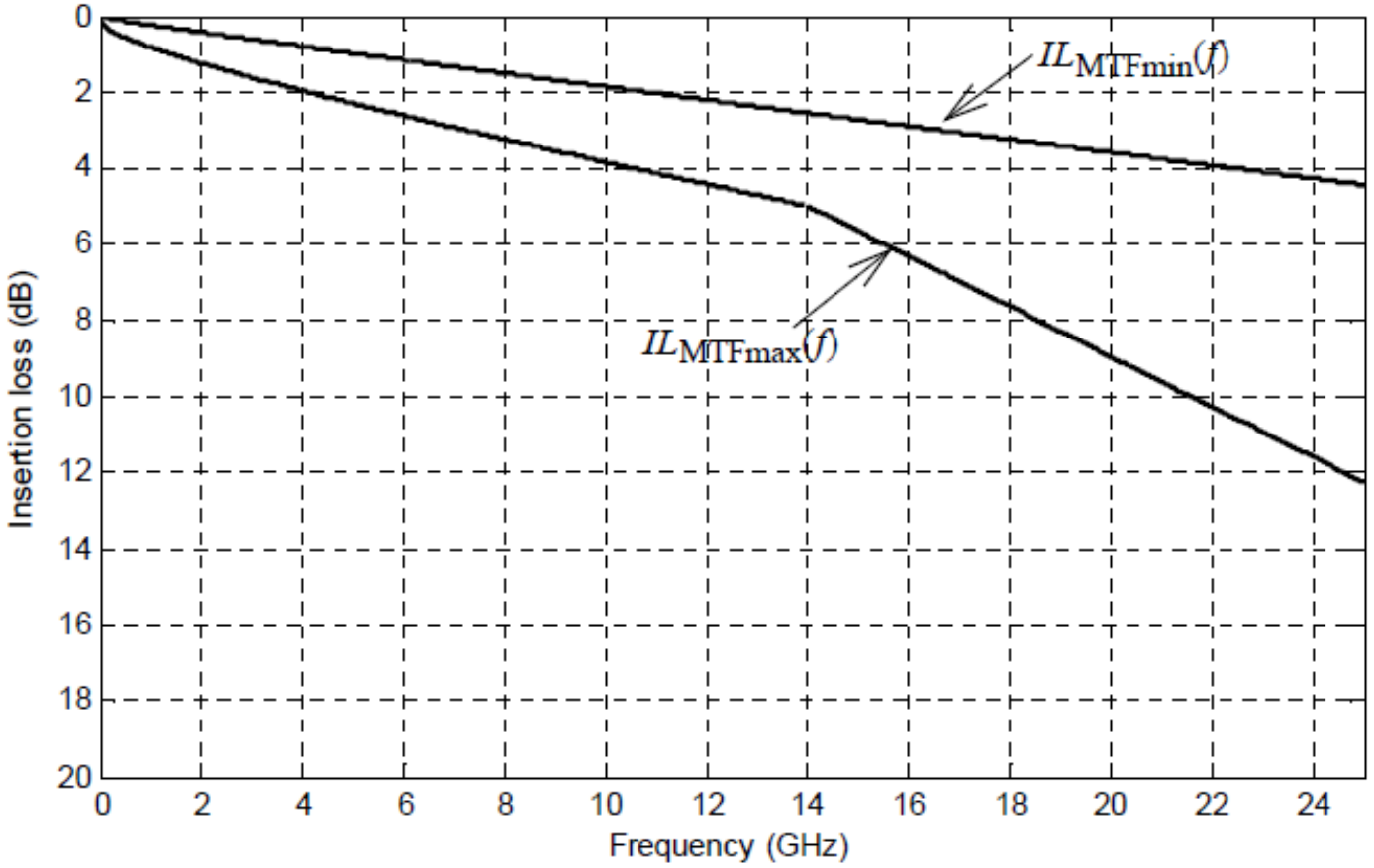
- Same as Annex 83E (CAUI-4 c2m)

CDAUI-8 c2m Tx Common-Mode to Differential & Rx Differential to Common-Mode Return Loss Specs



- Same as Annex 83E (CAUI-4 c2m)

Compliance Boards

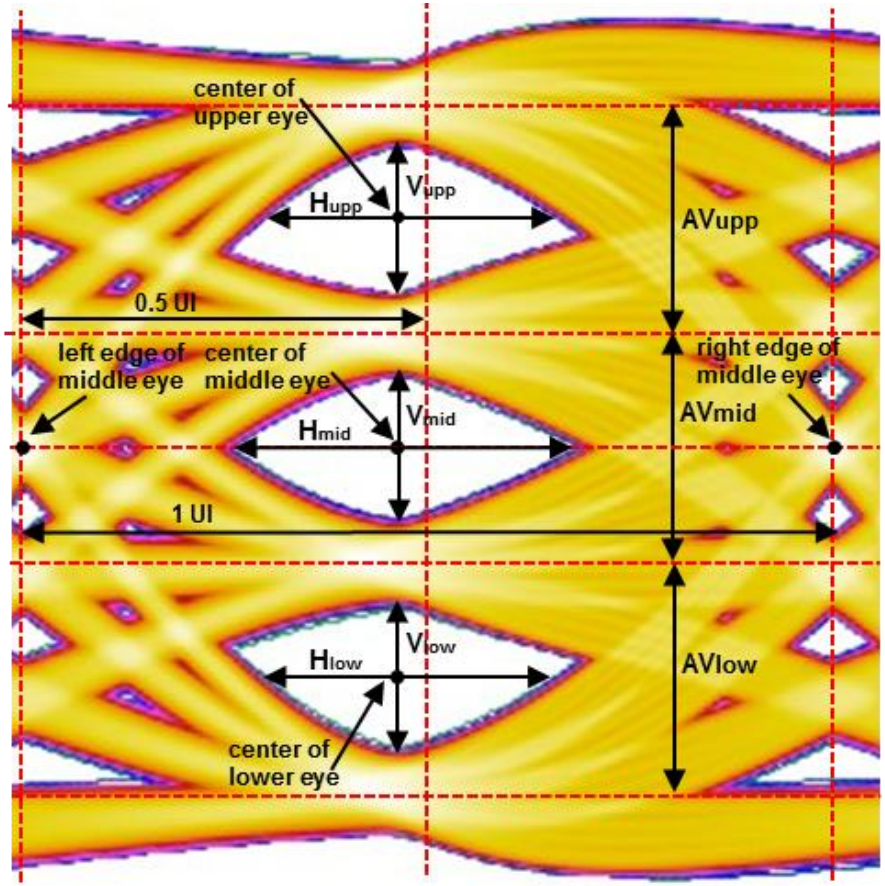


- Same as CR4 (Cl. 92)
  - No new compliance boards required

CDAUI-8 c2m Test Patterns

- CDAUI-8 PMA can reuse test pattern defined in clause 94.2.9:
  - Quaternary PRBS13 test pattern (if the termination block (i.e., 94.2.2.4) is removed, this will need to be changed accordingly)
  - Other KP4 test patterns (JP03A, JP03B) not required

CDAUI-8 c2m PAM4 Jitter and Eye Height Parameters



See Appendix for measurement procedure

Module Stressed Receiver Test *

- Same test configuration as Annex 83E
  - Modified for PAM4 testing consistent with 56G-VSR-PAM4
  - CRU and SIJT corner frequencies pending further study

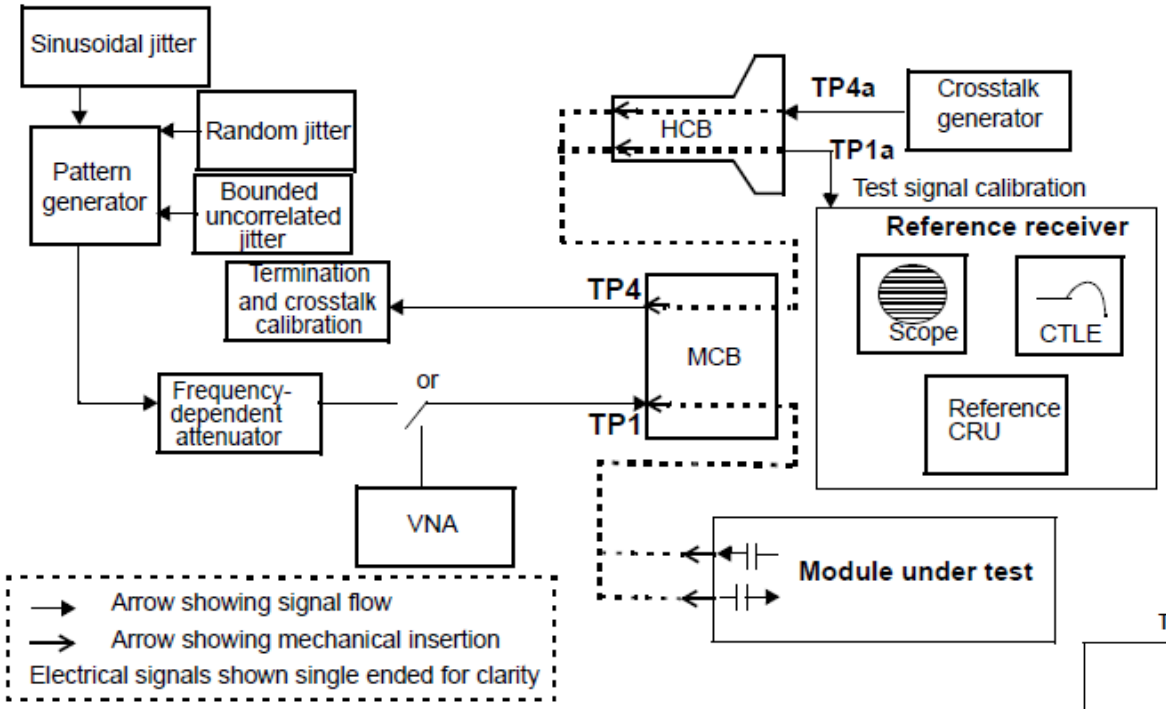


Figure 83E–15—Example module stressed input test

Table 15-7. Sinusoidal jitter frequency for TP4 and TP1 testing

Frequency Range (Hz)	Sinusoidal jitter, Peak to peak (UI)
f<fb/849600	*Not Specified*
fb/849600 < f ≤ fb/8496	*5*fb/(849600*f)*
fb/8496 < f ≤ 10xLB	*0.05*
NOTES:LB = Receiver Loop Bandwidth	

Host Stressed Receiver Test

*

- Same test configuration as Annex 83E
  - Modified for PAM4 testing consistent with 56G-VSR-PAM4
  - CRU and SIJT corner frequencies pending further study

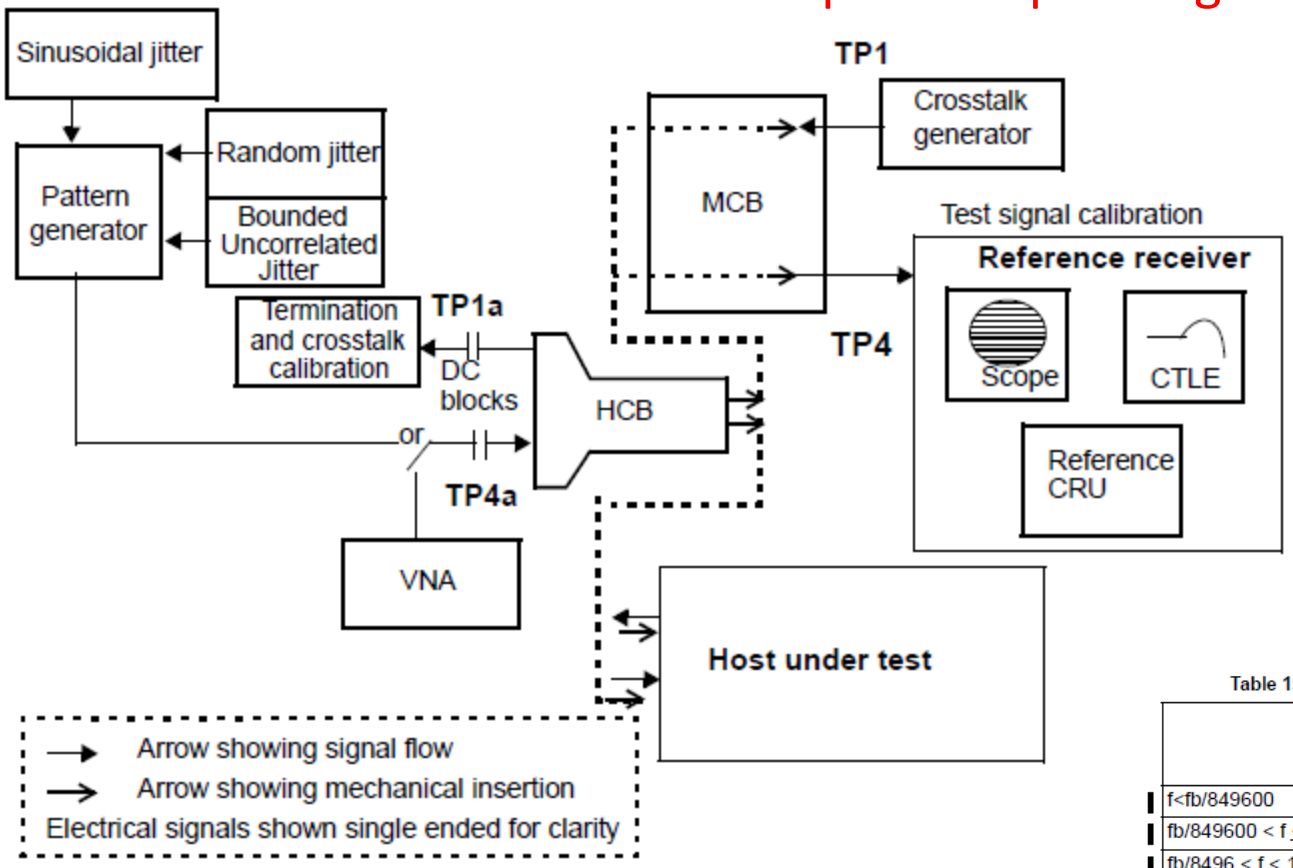


Figure 83E–14—Example host stressed input test

Table 15-7. Sinusoidal jitter frequency for TP4 and TP1 testing

Frequency Range (Hz)	Sinusoidal jitter, Peak to peak (UI)
f<fb/849600	*Not Specified*
fb/849600 < f ≤ fb/8496	*5*fb/(849600*f)*
fb/8496 < f ≤ 10xLB	*0.05*
NOTES:LB = Receiver Loop Bandwidth	

Host / Module Output Waveform Test *

- Same test configuration as Annex 83E
  - Modified for PAM4 testing consistent with 56G-VSR-PAM4
  - CRU corner frequency pending further study

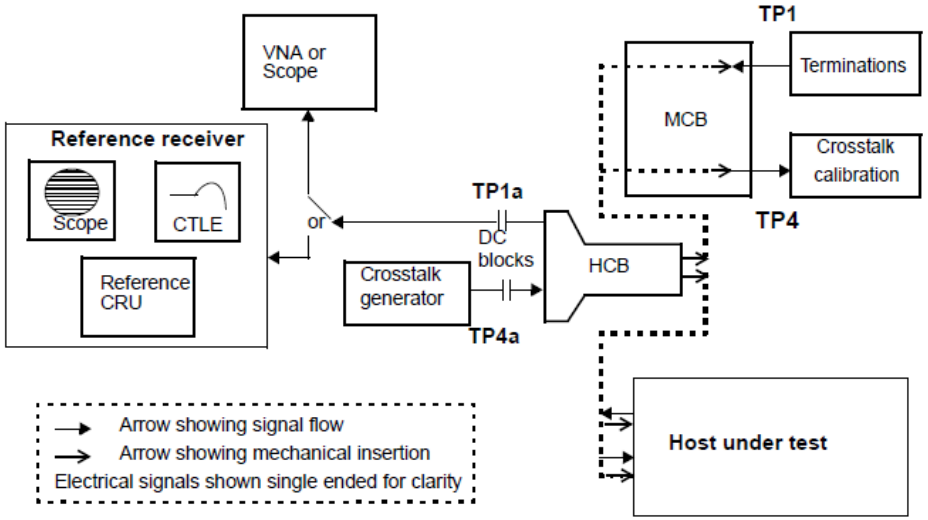


Figure 83E–9—Example host output test configuration

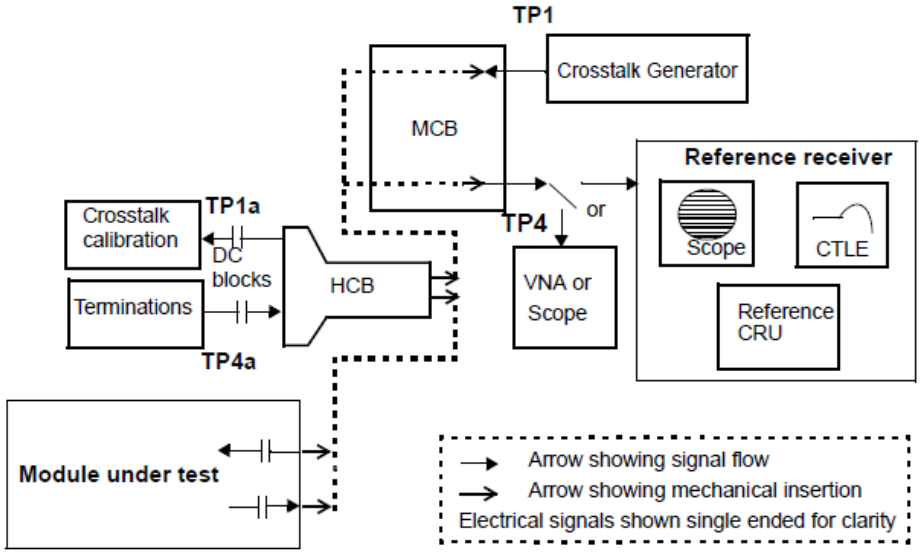


Figure 83E–11—Example module output test configuration

Summary

- Baseline proposal using PAM4 signaling for a CDAUI-8 c2m electrical interface specification:
  - Supports CAUI-4 c2m channel
  - Reuses test infrastructures and setup in Annex 83E
  - Is consistent with CEI-56G-VSR draft baseline specification
    - Straightforward to extend/modify Annex 83E specification for PAM4 signaling

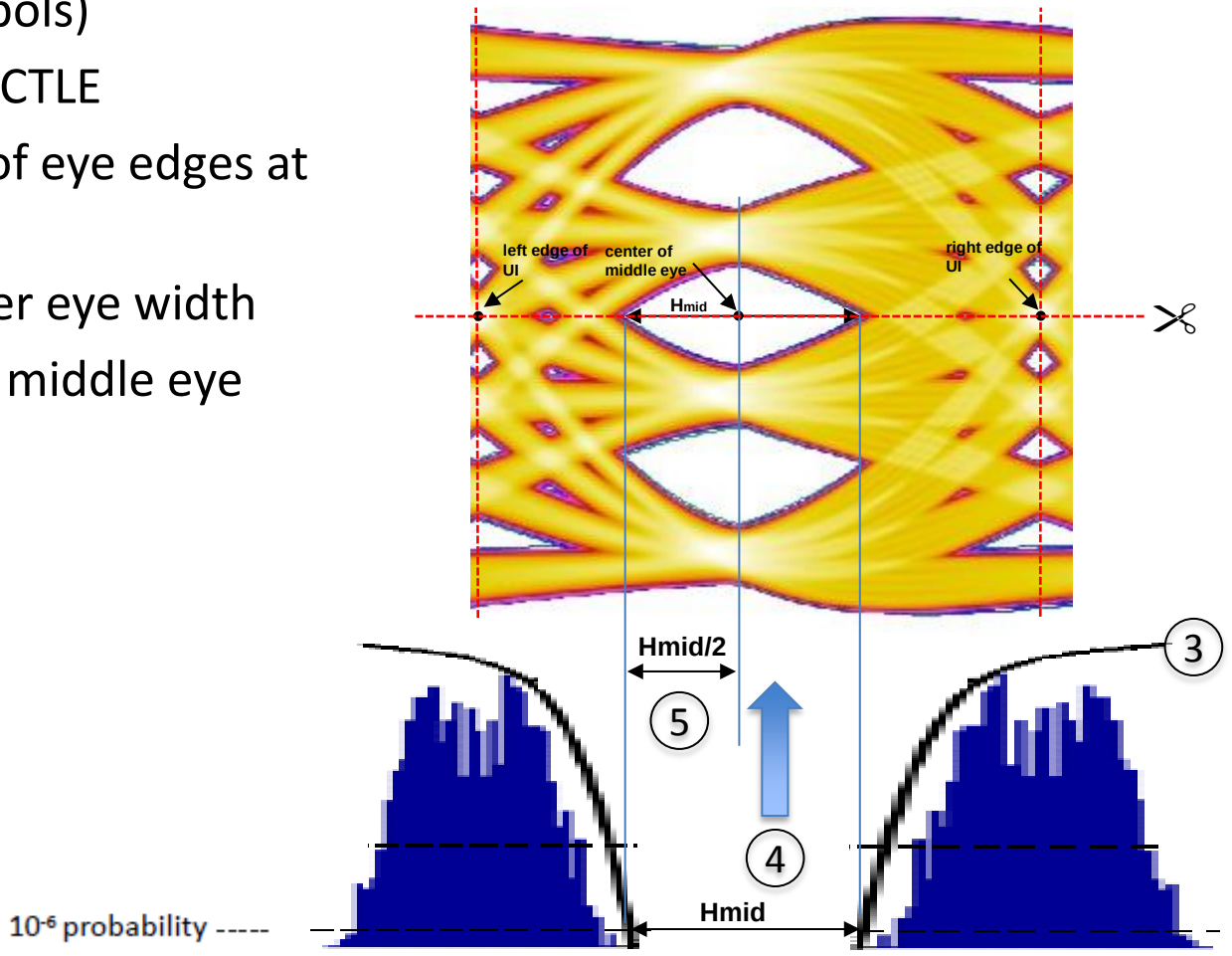
References

[1] oif.2014.230.01, www.oiforum.com (This document was provided as an attachment to the October 28, 2014 liaison from OIF to IEEE 802.3. The liaison and its attachments can be found in the IEEE P802.3bs 400 Gb/s Ethernet Task Force private area)

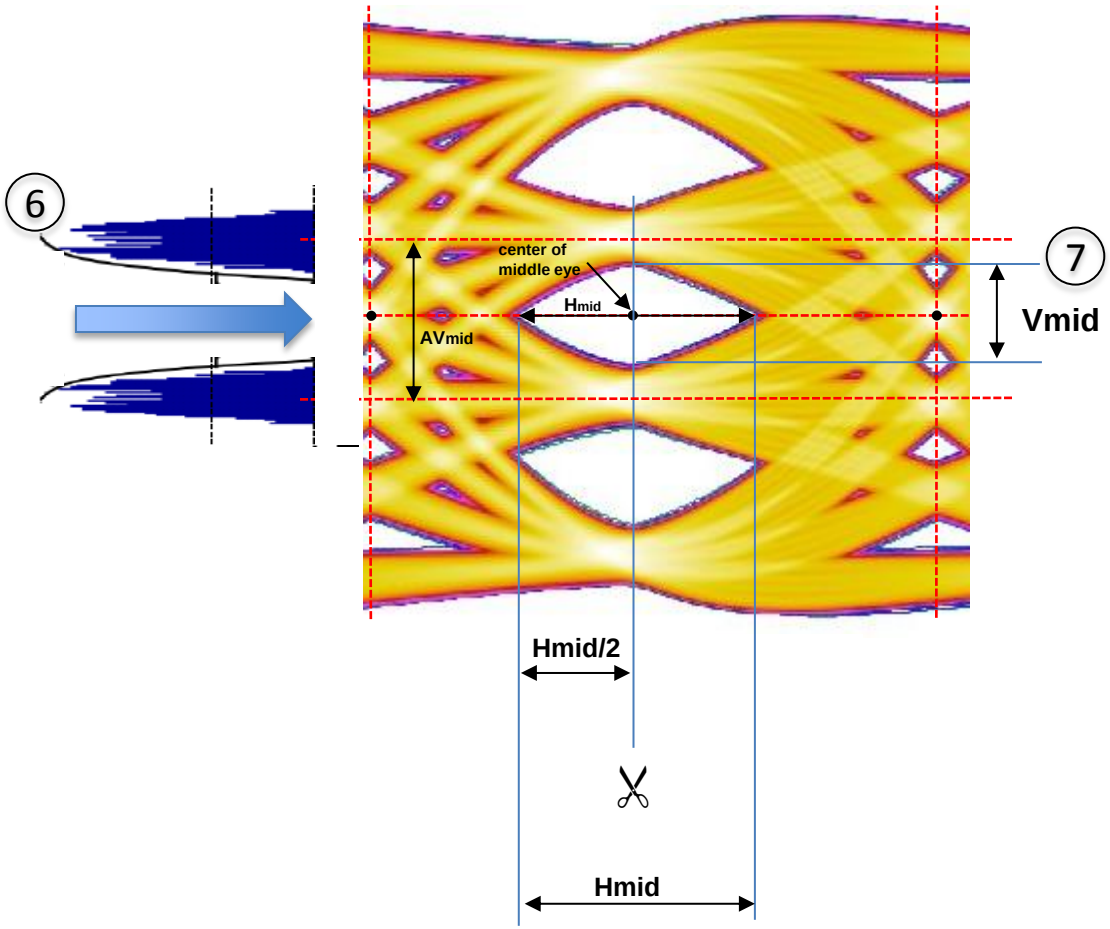
Appendix

Extracting PAM4 Eye Width and Height

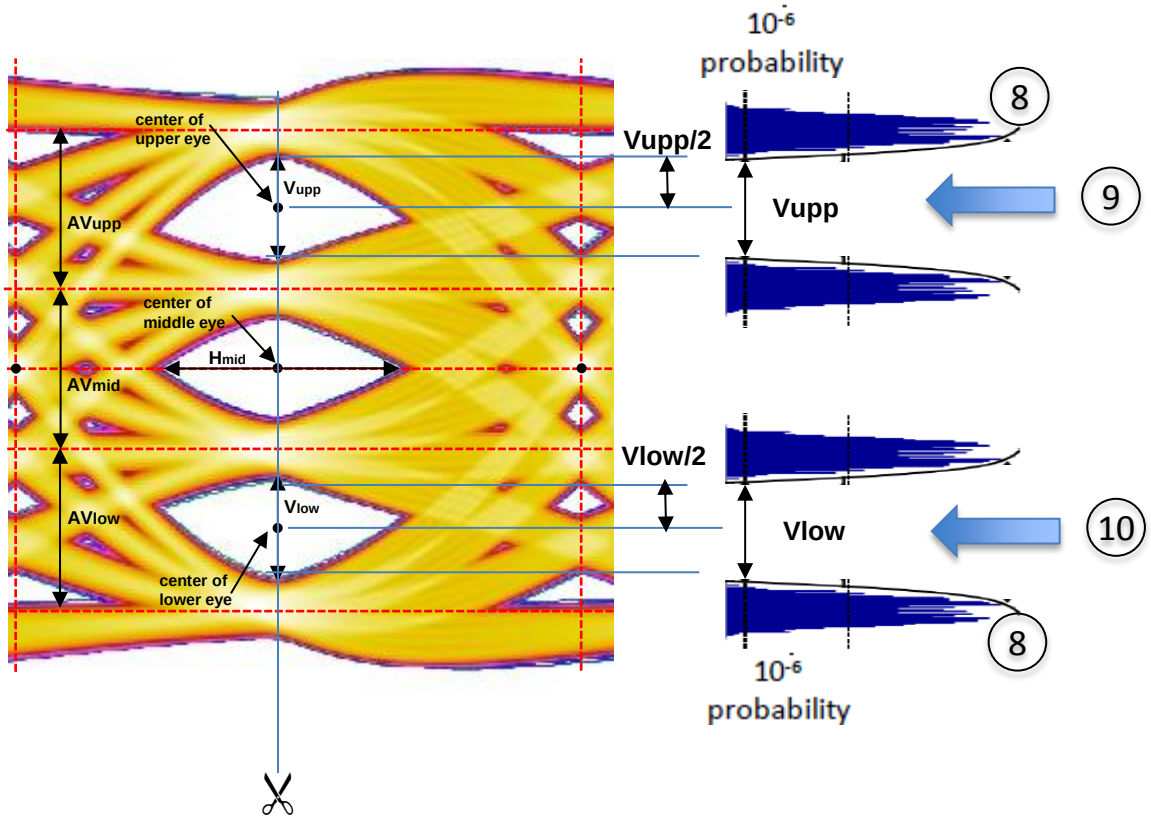
- Reuse Annex 83E.4.2 method to:
  1. Capture QPRBS13 pattern (> 4 million symbols)
  2. Apply reference CTLE
  3. Construct CDFs of eye edges at zero crossing
  4. Hmid = 1e-6 inner eye width
  5. Locate center of middle eye at Hmid/2



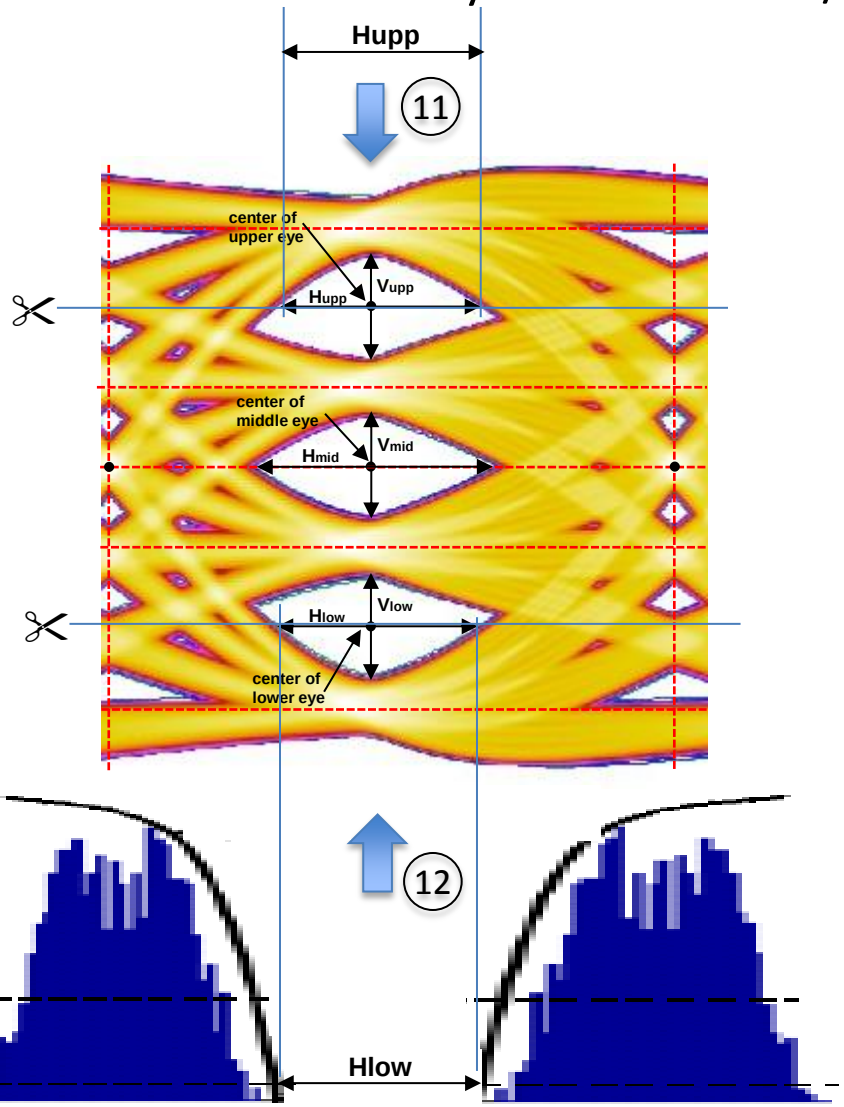
- Reuse Annex 83E.4.2 method to:
  6. Construct CDFs of signal voltages of middle eye sampled at Hmid/2
  7. Vmid = 1e-6 inner eye height



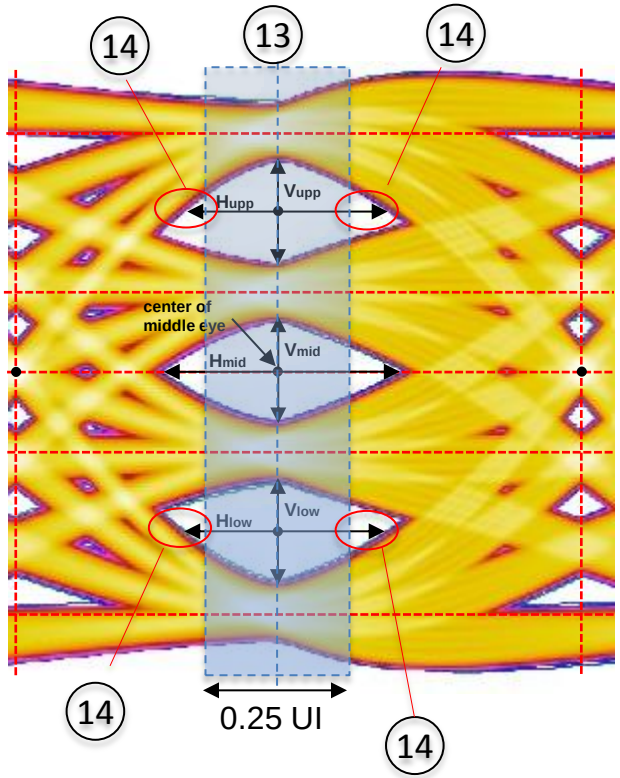
- Extract upper and lower eye heights
  8. Construct CDFs of signal voltages of upper and lower eyes at Hmid/2
  9. Vup = 1e-6 inner height of upper eye at Hmid/2
  10. Vlow = 1e-6 inner height of lower eye at Hmid/2



- Extract upper and lower eye widths
  11. Hupp = 1e-6 inner width of upper eye sliced at Vupp/2
  12. Hlow = 1e-6 inner width of lower eye sliced at Vlow/2



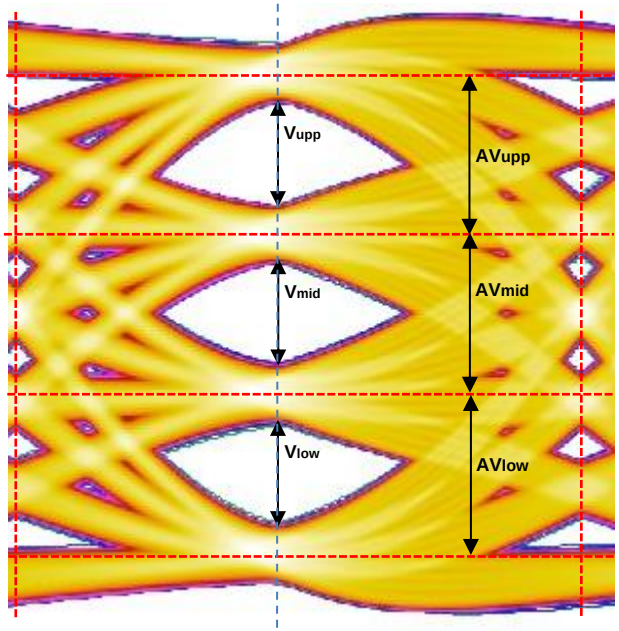
- Check upper and lower eye alignment to middle eye
  13. Apply 0.25UI-wide mask centered on middle eye
  14. 1e-6 horizontal openings of upper and lower eyes must extend outside this mask, measured at ½ inner eye height



- Module Output VEC Measurement

15. Calculate VEC as 20log[min(AVupp/Vupp, AVmid/Vmid, AVlow/Vlow)]

*



Energy Efficient Ethernet (EEE) for 802.3bs

Arthur Marris - Cadence

Supporters

- Mark Gustlin – Xilinx
- Andre Szczepanek – Inphi
- Dave Ofelt – Juniper
- Gary Nicholl - Cisco

Key features of Energy Efficient Ethernet (EEE)

- If a system has nothing to transmit it can power down its transmit path after it has indicated its intention to do so.
- The partner device can also power down its receive path when it detects that the path is going to be powered down.
- The link stays up while in low power mode and no frames are dropped.
- EEE is asymmetric. One direction can be powered up while the other is powered down.

How does EEE work?

- The client (i.e. system) requests Low Power Idle (LPI) from the reconciliation sublayer (RS).
- The RS then signals LPI on the MII (media independent interface).
- The transmit PCS (physical coding sublayer) encodes the LPI signal using a special symbol.
- The receive PCS decodes the LPI symbol and signals LPI on the receive MII.
- When the client ceases requesting LPI the RS continues inhibiting transmission for a fixed period to allow time for the local transmit path and remote receive path to recover from their low power modes.

What is “Fast Wake” mode of operation?

- In Fast Wake mode of operation the transmit and receive path remain active and continuously transmit and receive LPI when it is requested by the client. (However Clause 82 BIP is not calculated)
- Fast Wake is compulsory for 40G and 100G PHYs that support EEE.
- Fast Wake is controlled by LLDP (Link Layer Discovery Protocol) rather than AN (auto-negotiation)
- Fast Wake is suitable for optical PHYs that unable to power up and down quickly and do not support AN.

What is “Deep Sleep” mode of operation?

- In Deep Sleep mode the transmit path stops transmitting but periodically sends refresh indication while LPI is requested.
- In Deep Sleep mode the receiver checks for the occurrence of refresh indication and will assert link failure if refresh does not appear.
- Deep Sleep mode requires the receive PMA and PCS to resume operation within a determined time period.
- In Deep Sleep mode the transmit and receive PCS generate tx_quiet and rx_quiet signals to allow the PHY to periodically power down its transmit and receive path.
- Clause 83 defines a mechanism for sending the tx_quiet signal over the CAUI/XLAUI interface and for synthesizing the rx_quiet signal.
- As only optical PHYs are included in the 802.3bs objectives, none of the PHYs specified in 802.3bs will support Deep Sleep operation, however the architecture should not preclude support for Deep Sleep in the future.

What should be done for 802.3bs?

- Adopt Fast Wake mode of operation for the 802.3bs PHY types.
- Add these PHY types to “Table 78-1 Clauses associated with each PHY or interface type” and indicate that they do not support deep sleep with the “b” suffix.
- The CDMII will need to be able to signal LPI and the RS will need to include a transmit LPI state machine to defer transmission for the wake time period after de-assertion of LPI.
- The PCS will need to be able to encode and decode LPI.

Further considerations for supporting EEE in 802.3bs

- Consider whether the receive PCS should have a “RX_FW” state that it goes into when receiving LPI from its link partner. In this state it could disable error checking.
- When specifying the CDAUI electrical interface consider defining a mechanism for transmitting alert and quiet signalling similar to how it is done in 83.5.11.1 to allow for future support of Deep Sleep, and also consider generation of an energy detect signal.
- To support Deep Sleep mode the PCS needs to achieve synchronization and alignment quickly. This will most likely be done through the use of “rapid alignment markers” so make sure the architecture does not preclude their use in the future.
- If Deep Sleep is supported in the future then the CDXI may need to be powered down. In this case it would be necessary to preserve the MII signalling of LPI to the PCS in the transmit direction and LPI to the MAC in the receive direction until the interface powers up. Also it will be necessary for the CDXI to power up quickly.

Summary

- 802.3bs will use EEE fast wake functionality which requires the CDMII to signal LPI and the PCS to encode and decode it
- To allow for future support of deep sleep functionality consideration needs to be given to how the PCS and electrical interfaces can resume operation quickly after power down

OTN Support Proposal
P802.3bs 400 Gb/s Ethernet Task Force

Steve Trowbridge

Alcatel-Lucent

Supporters

- Pete Anslow (Ciena)
- Gary Nicholl (Cisco)
- Tongtong Wang (Huawei)
- Xinyan Wang (Huawei)
- David Ofelt (Juniper)
- Andre Szczepanek (Inphi)

Key Elements of OTN Support

- See "OTN Support: What is it and why is it important?", July 2013
  - A new rate of Ethernet (e.g., 400 Gb/s) fits into the corresponding rate OTN transport signal
  - All Ethernet PHYs of a given rate are mapped the same way and can be interconnected over the OTN (e.g., same PCS for all 100 Gb/s PHYs gives a single canonical format ("characteristic information" in ITU-T terminology) that can be mapped
  - Optical modules for Ethernet can be reused for OTN IrDI/client interfaces at the corresponding rate

A new rate of Ethernet (e.g., 400 Gb/s) fits into the corresponding rate OTN transport signal

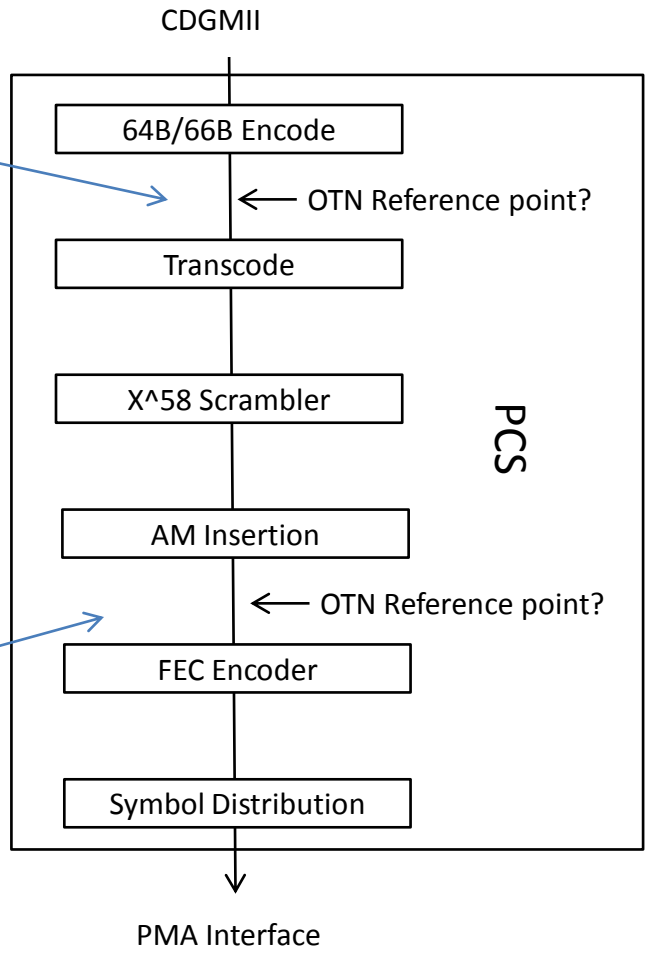
- Assumption – the OTN mapper/demapper will terminate and regenerate any Ethernet FEC code, correcting errors at the OTN ingress since the FEC is chosen to correct single-link errors but not double-link errors
- Assumption – the OTN mapper/demapper may trans-decode/trans-encode back to 64B/66B to avoid MTTFPA reduction for OTN transported signal
- Based on these assumptions, the encoded data rate of the OTN-mapped 400 Gb/s Ethernet would be no more than 400 Gb/s x 66 / 64 = 412.5 Gb/s ±100ppm. Since the 400 Gb/s OTN container would presumably be designed to also transport four “lower order” ODU4s, there should be no concern that it is large enough to carry 400 Gb/s Ethernet based on the assumption that the canonical form is near this rate.
- Any Ethernet bits in excess of this rate are likely to be part of a FEC that is not carried over OTN

All PMDs of a given rate are mapped in the same way into OTN:

Candidate Locations for the OTN Reference point

Option B

Option A



OTN Reference Point Option A

- Pro
  - Most similar to what ITU-T chose for mapping of 40GbE into OPU3 and 100GbE into OPU4 based on 802.3ba assumption that all PMDs of a given rate used exactly the same logical lane striping
  - Capable of carrying end-to-end information in the alignment markers if all PMDs are striped the same
- Con
  - Even if all P802.3bs PMDs use the same logical lane striping, if all future 400GbE PMDs are not striped in the same way, requires re-striping into the canonical format before mapping into OTN
  - Relies on OTN FEC for satisfactory MTTFPA

OTN Reference Point Option B

- Pro
  - High certainty to be a common format regardless of whether all 400GbE PMDs (P802.3bs and future) use the same logical lane striping
  - No need to convert between logical lane formats in OTN mapper/demapper
  - Robust MTTFPA regardless of what ITU-T does with FEC
- Con
  - Can't carry end-to-end information in alignment markers. But note that there doesn't seem to be a compelling reason to support BIP inside of FEC-enabled Ethernet PMDs
  - Higher bit-rate to map as 64B/66B rather than mapping the transcoded signal.

Straw Polls relevant to OTN support

- Straw Poll #1 - I support FEC for optical PMDs
  - **FEC mandatory – 69**
  - FEC optional – 7
  - Some PMDs may not need FEC – 0
  - Mandatory for some, optional for others – 10
  - Need more information – 10
- Straw Poll #9 - If all PMDs developed in P802.3bs include mandatory FEC and FEC error statistics are available, do we also require BIP?
  - Y: 4; **N: 24; A: 69**
- Straw Poll #10 – If BIP is required, should it be:
  - Segment by segment (optimized for fault isolation) – 2
  - End to end (optimized for service assurance) – 6
  - **Need more information – 35**
  - **Not required/don't care - 33**

Observations

- Strong majority believe that all optical PMDs developed by P802.3bs will have mandatory FEC
- Most think that if all optical PMDs have mandatory FEC, that BIP is not necessary, i.e., you get a better view of link quality from FEC corrected errors
  - Note that any BIP inside of a FEC exhibits a “cliff” behavior, going from zero errors to quite a lot the instant the error ratio exceeds the correction capability of the FEC. In addtion, this information is available from the FEC uncorrected codewords counter
- For those who still think there would be BIP, the number who express an opinion on how it is used (fault isolation or service assurance) is statistically insignificant
- For those who still think they need more information, please study slides 5-12 of trowbridge_3bs_01_0714.pdf and ask questions!

OTN Reference Point Proposal

- Propose that the OTN reference point for 400GbE is a logically serial stream of 64B/66B blocks, unstriped, without lane alignment markers (Option B). An implication of this choice is that there is no BIP carried end-to-end (note that a segment BIP for a particular lane striping and FEC would still be possible).
- Any idle insertion/deletion to provide room for striping overhead must occur between the CDGMII and the OTN reference point. No idle insertion/deletion should occur between the OTN reference point and the PMD. Assuming 16K frequency of lane markers (regardless of the lane count or lane rate), the effective rate of this logical interface is the *nominal MAC rate x 66/64 x (1-1/16384)* so that any physical instantiation has room to insert lane markers as needed without idle insert/delete elsewhere in the stack

Module Reuse

- Module reuse was facilitated by the fact that nothing below a CAUI chip-to-module interface cared about the or manipulated the bit values on the lanes – as long as OTN was striped into the same number of logical lanes as Ethernet, everything would work
- The following likely can be preserved: no idle insertion/deletion occurs below a CDAUI chip-to-module interface
- The following are possibly not be precluded by the 400GbE architecture:
  - Logical to physical lane multiplexing in a module may be on a block or FEC symbol basis rather than a bit basis
  - One (possibly Ethernet Frame Format dependent) FEC code may be replaced with another)

Options for Module Reuse

- Option I: Preserve the 802.3ba rule that no sublayers below a CDAUI care about bit values or manipulate the bit values on logical lanes (bit multiplexing only). Any FEC is done on the host board above a CDAUI. OTN may use a different FEC than Ethernet if it needs a stronger FEC to compensate for the higher bit-rate
- Option II (most general, described in Norfolk) encode the OTN frame as 66B blocks (all data) and use whatever striping and FEC encoding mechanisms are used for Ethernet. OTN and Ethernet use the same FEC
- Option III (potentially very complex) Allow OTN to use a different (stronger) FEC than Ethernet but do not require bit multiplexing of logical lanes. This would constrain that OTN and Ethernet choose FEC (or pairs of FECs, if not all 400GbE PMDs use the same FEC) with the same symbol size and that the marking to discover the FEC symbol alignment is common between OTN and Ethernet

Option II Amplification

- Use the fact that the OTN reference point, as proposed, is a logically serial stream of 64B/66B blocks.
- Note that before this reference stream can be physically instantiated, it must be striped over multiple physical or logical lanes
- Maintain the principle, as in 802.3ba, that idle insertion/deletion is not done below this reference point.

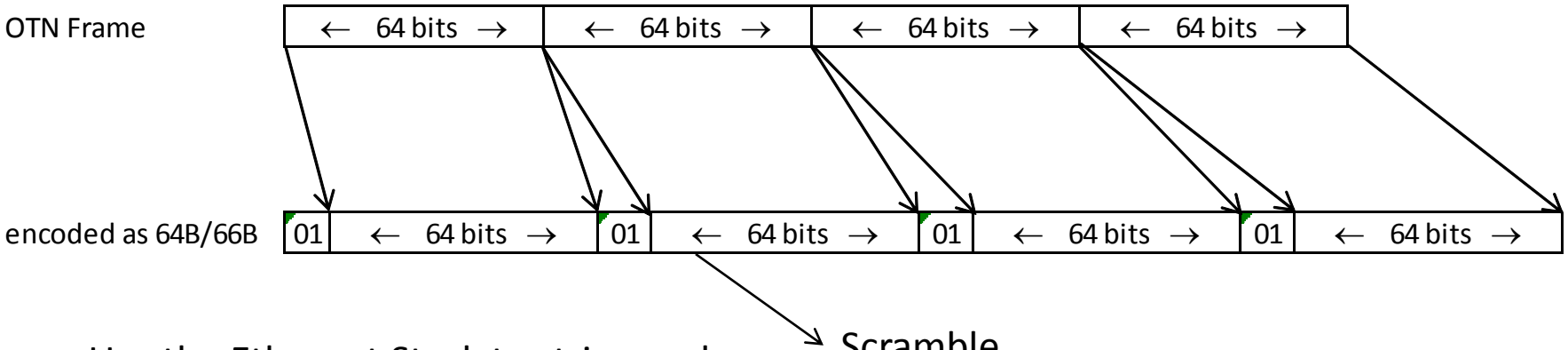
Option II Example

- Example physical instantiation could be something like gustlin_400_02a_1113.pdf, produced by transcoding 64B/66B to 256B/257B, striping first into 100G groups, striping within each 100G group into 4 logical lanes on 10-bit symbol boundaries, inserting alignment markers on each lane, and applying an RS(528,514) code based on 10-bit symbols with alignment markers appearing in the first of each of 4096 Reed Solomon code blocks (essentially 4 instances of P802.3bj 100G FEC)

Option II Implications for OTN

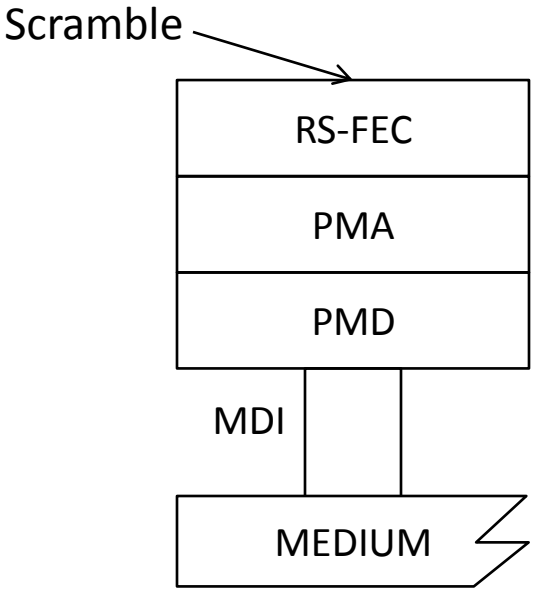
- Likely only possible if the same FEC code can be used for OTN applications as for Ethernet applications at about 6% higher bit-rate
- Would need to make OTN look like 66B blocks. Easiest way to do this and not lose any information in transcoding is to insert a “01” sync header after every 64 bits (all data)
- Since this is just part of the logical frame format, this doesn’t waste as many bits as it appears. 8 sync header bits are added to every 256 data bits in the “logical” frame format, but 7 of those bits are immediately recovered in 256B/257B transcoding and reused for the FEC code. So 0.39% net is added to the OTN frame to make it look like 66B blocks, then 2.724% overhead RS FEC added

Option II - Illustration of turning OTN frame into 64B/66B blocks



Use the Ethernet Stack to stripe and FEC encode the OTN frame when carrying over an Ethernet Module for an OTN IrDI or client interface

Could be OTN frame aligned as an OTUC4 frame without FEC is exactly 7648×64 bits, but not essential with scrambling



Option II: OTN Bit-rates using this scheme

	Working Assumption Bit-Rate
OTUC4 bit-rate without FEC	422.904 Gb/s
64B/66B encoded	436.120 Gb/s
256B/257B transcoded	424.556 Gb/s
Insert Lane Markers	424.582 Gb/s
Add RS(528,514) FEC	436.146 Gb/s
Logical Lane Rate (well within CEI-28G)	27.259 Gb/s
Ethernet Nominal Bit-rate	412.5 Gb/s
400G OTN Increase in bit-rate	5.73 %

100G OTN Increase in bit-rate	8.42 %

Smaller increase for 400G than for 100G, mainly due to RS(528,514) FEC rather than RS(255,239) FEC. Proportion remains the same even for Ethernet PMDs that use a higher overhead FEC

Option II – Recommended module reuse mechanism for OTN

- There is an Ethernet sublayer reference point such as the that is logically equivalent to a serial stream of 64B/66B blocks (the same as the recommended OTN reference point)
- No idle insertion/deletion occurs below the that reference point, and hence the rest of the stack can deal with a constant-bit-rate (CBR) bitstream that is effectively an infinite-length packet.
- Note that any logical to physical lane interleaving that works for Ethernet also works for OTN since they are encoded the same way
- The link parameters and FEC coding gain have sufficient margin to meet the error performance target when running at approximately 5.73% higher bit-rate than necessary for 400G Ethernet

THANKS!

400 Gb/s 100 m MMF reach objective draft baseline proposal

MMF ad hoc

IEEE P802.3bs, San Antonio, TX, Nov 2014

Outline

- Baseline proposal of a retimed PMD to address the 802.3bs objective to ‘Provide physical layer specifications which support link distances of at least 100 m over MMF’
  - 16 lane parallel, short wavelength based PMD for 400GBASE-SR16.
  - Leveraging 100GBASE-SR4 technology, compatible with 16 x 25 Gb/s electrical interface, and breakout applications.
  - Assumed use of 100GBASE-SR4 FEC, or similar strength FEC (to be defined in 802.3bs), to enable 100 m reach.
  - Architecture, parameters and specifications for optical interfaces, and the proposed MDI, follow.

Supporters and contributors

- John Abbott, Corning
- Piers Dawe, Mellanox
- Mike Dudek, QLogic
- Ali Ghiasi, Ghiasi Quantum LLC
- Mark Gustlin, Xilinx
- Jack Jewell, Commscope
- Jonathan King, Finisar
- Scott Kipp, Brocade
- Paul Kolesar, Commscope
- Brett Lane, Panduit
- Robert Lingle Jr., OFS
- Valerie Maguire, Siemon
- Slobodan Milijevic, Microsemi
- John Petrilla, Avago technologies
- Rick Pimpinella, Panduit
- Rick Rabinovich, Alcatel-Lucent Enterprise
- Steve Swanson, Corning
- Mike Zhang, Siemon

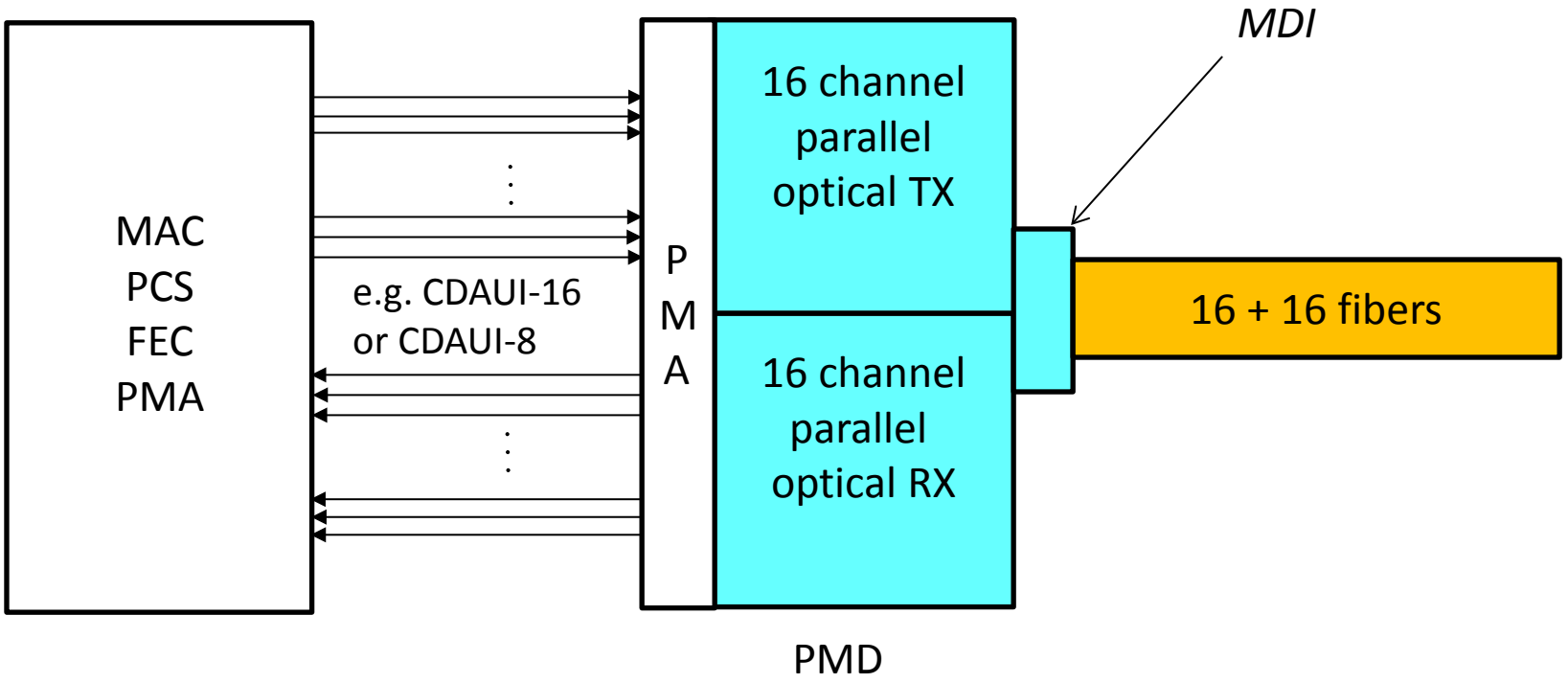
and a very nice letter of support
from the CDFP MSA

Motivation

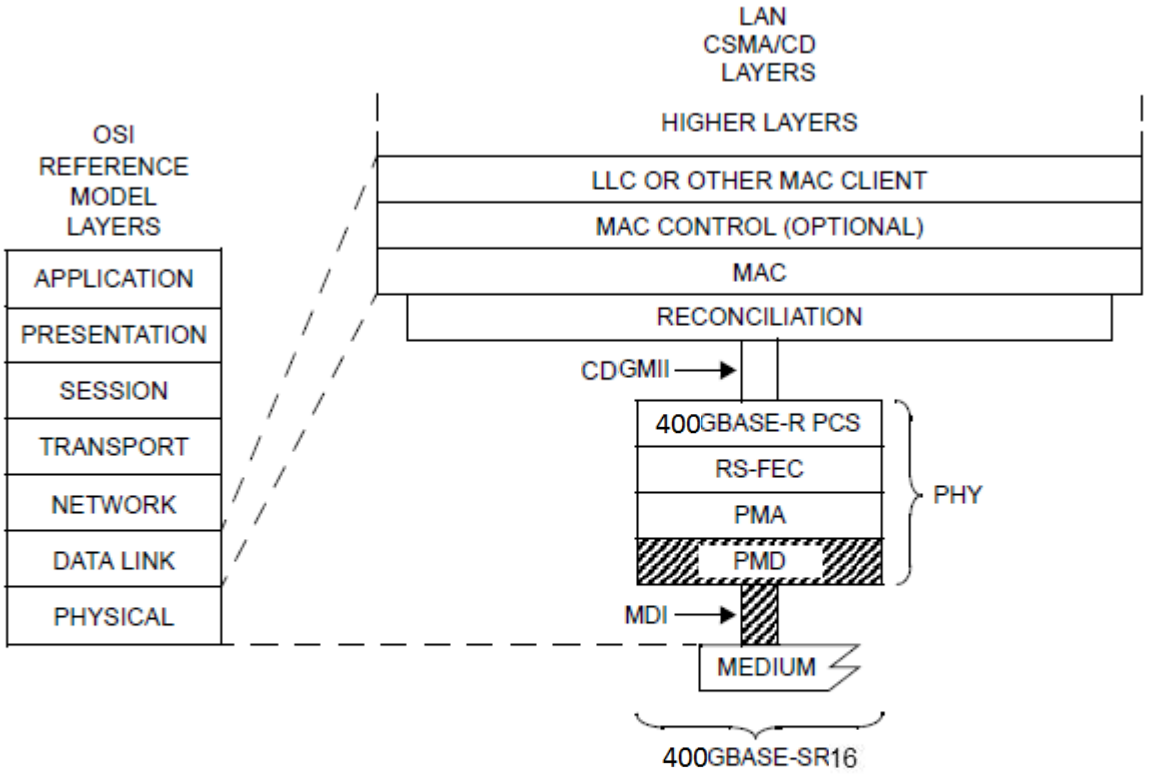
- 16 parallel links operating at 25.78125 GBd utilize low cost, high performing multimode fiber compatible optics and electronics
  - Leverages 100GBASE-SR4 technology
  - FEC supported retimed interface enables a lowest power, lowest cost, 100m solution today
  - Uses existing, viable semiconductor technologies and uncooled VCSELs
- The 16 optical lanes can directly map the 16 electrical lanes of CDAUI-16, without requiring multiplexing, translation, or de-skewing inside the module.
- Compatible with ‘break out’ application
- This proposal is supported by multiple vendors and users, and is economically feasible and competitive compared to other alternatives.

Proposal

- 16 parallel lanes @ 25.78125 GBd for 100GBASE-SR16 over 100 m OM4 fiber.
  - Exact signaling rate is determined by project's choice of FEC.
- 850 nm sources, re-use of 100GBASE-SR4 specifications.
  - Assumes PMD target BER (prior to error correction) around $5x10^{-5}$, similar to 100GBASE-SR4.



Position in 802.3 architecture

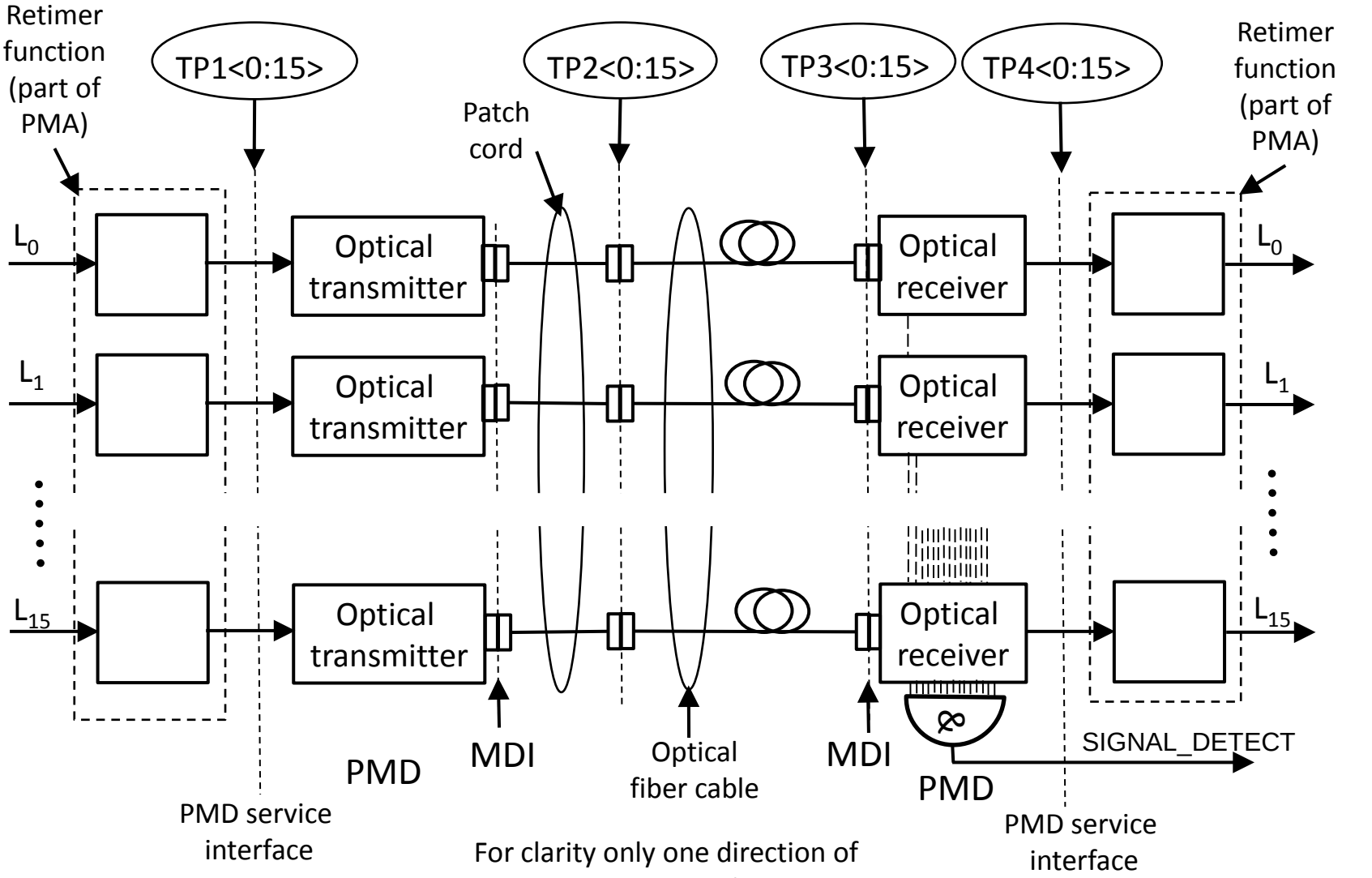


CDGMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
SR = PMD FOR MULTIMODE FIBER

Editor's note: The RS-FEC layer may be merged into 400GBASE-R PCS layer, depending on the choice of architecture by the Task Force.

Block diagram for 400GBASE-SR16 transmit/receive path



PMD Optical specifications

- Transmitter characteristics (each lane) at TP2 follow 100GBASE-SR4, Clause 95, Table 95-6.
- Receiver characteristics (each lane) at TP3 follow 100GBASE-SR4, Clause 95, Table 95-7.
- Illustrative link power budget follows 100GBASE-SR4, Clause 95, Table 95-8.
  - Current status of these tables shown on next 3 slides

Transmitter characteristics (each lane) at TP2: follow 100GBASE-SR4, Clause 95, Table 95-6 (D3.2 illustrated below)

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
RMS spectral width[a] (max)	0.6	nm
Average launch power, each lane (max)	2.4	dBm
Average launch power, each lane (min)	–9	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Optical Modulation Amplitude (OMA), each lane (min)[b]	–7	dBm
Launch power in OMA minus TDEC (min)	–7.9	dBm
Transmitter and dispersion eye closure (TDEC), each lane (max)	4.9	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio (min)	2	dB
Optical return loss tolerance (max)	12	dB
Encircled flux[c]	≥ 86% at 19 μm ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 1.5×10^{-3} hits per sample	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}	

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDEC < 0.9 dB, the OMA (min) must exceed this value.
[c]If measured into type A1a.2 or type A1a.3 50 μm fiber in accordance with IEC 61280-1-4.

Receiver characteristics (each lane) at TP3: follow 100GBASE-SR4, Clause 95, Table 95-7 (D3.2 illustrated below)

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–10.9	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	–5.6	dBm
Conditions of stressed receiver sensitivity test:[d]		
Stressed eye closure (SEC), lane under test	4.9	dB
Stressed eye J2 Jitter, lane under test	0.39	UI
Stressed eye J4 Jitter, lane under test	0.53	UI
OMA of each aggressor lane	3	dBm
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.
[d]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

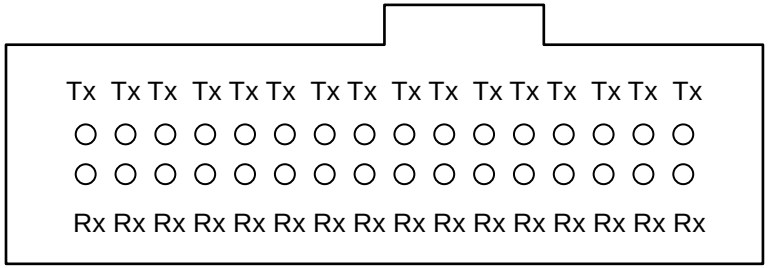
Illustrative link power budget: follow 100GBASE-SR4, Clause 95, Table 8 (D3.2 illustrated below)

Parameter	OM3	OM4	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700	MHz.km
Power budget (for max TDEC)	8.2		dB
Operating distance	0.5 to 70	0.5 to 100	m
Channel insertion loss[b]	1.8	1.9	dB
Allocation for penalties[c] (for max TDEC)	6.3		dB
Additional insertion loss allowed	0.1	0	dB

[a]per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 95–5 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 95.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

Medium Dependent Interface (MDI) for 400GBASE-SR16 and lane assignments

- Similar to the MDI defined for 100GBASE-SR10 (Clause 86.10.3.3, Recommended Option A), but using MPO-16, a 16-wide version of the 100G-SR10 MDI.
- Transmitters occupy the top row and receivers occupy the bottom row for better heat dissipation



400GBASE-SR16 optical lane assignments for the MDI receptacle when viewed looking into the receptacle with keyway feature on top.

  - The following 4 slides show draft text and figures which describe the MDI and lane assignments, using clause 86 and 95 content as basis, with modifications for 400GBASE-SR16 and MPO-16

MDI (1 of 4)

xx.m.n Medium Dependent Interface (MDI)

The 400GBASE-SR16 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure xx-a). The 400GBASE-SR16 PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure xx-b. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;
b) PMD with receptacle.

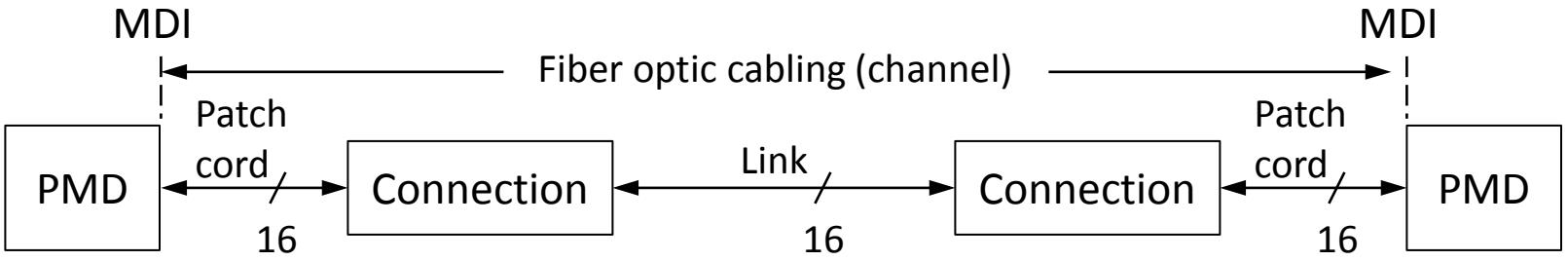


Figure xx-a – Fiber optic cabling model

Editor's note: Figure xx-a may be placed in a preceding subclause

MDI (2 of 4)

xx.m.n.1 Optical lane assignments

The sixteen transmit and sixteen receive optical lanes of 400GBASE-SR16 shall occupy the positions depicted in Figure xx-b viewed looking into the MDI receptacle with the connector keyway feature on top. The interface contains 32 active lanes within 32 total positions. The transmit optical lanes occupy the top row. The receive optical lanes occupy the bottom row. See clause xx.m.n.2 for MDI optical connector requirements.

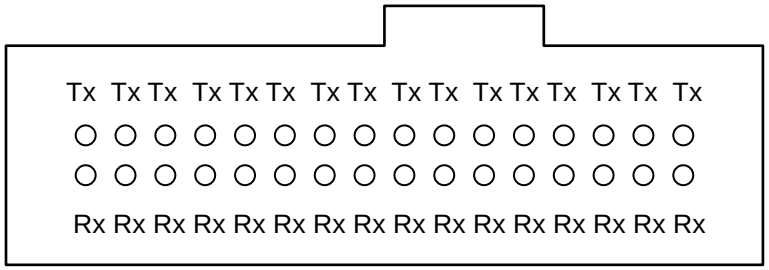


Figure xx-b -- 400GBASE-SR16 optical lane assignments
viewed looking into the MDI receptacle with keyway feature on top.

MDI (3 of 4)

xx.m.n.2 Medium Dependent Interface (MDI) requirements

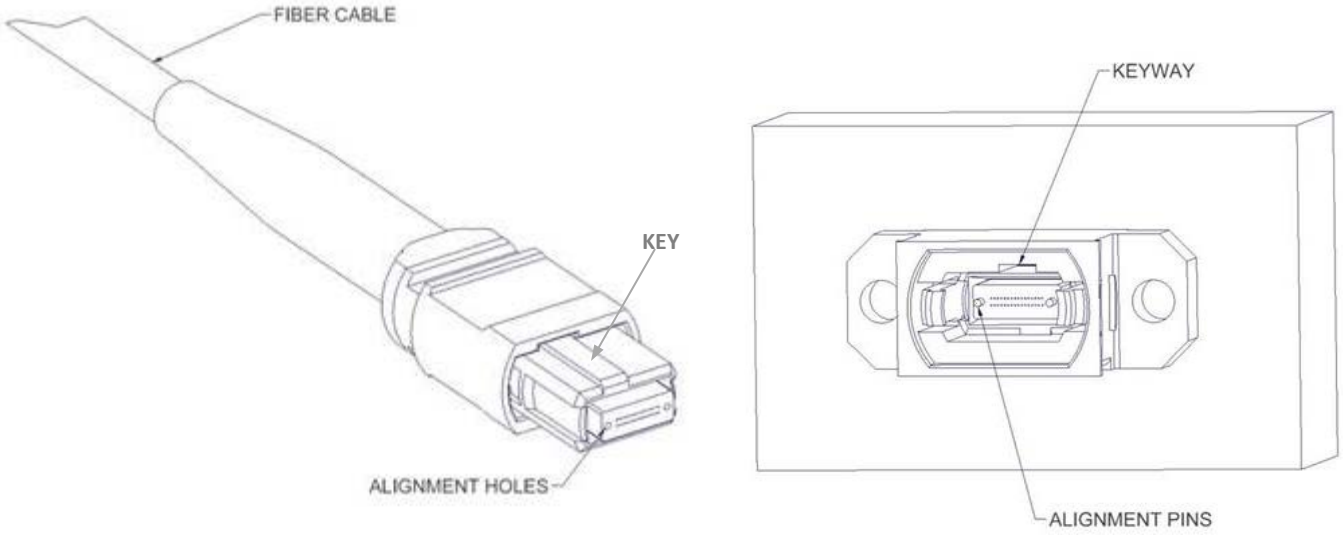
The MDI adapter or receptacle shall meet the dimensional specifications of ANSI/TIA-604-18 adapter designation FOCIS 18A-k-0. The plug terminating the optical fiber cabling shall meet the dimensional specifications of ANSI/TIA-604-18 female plug connector flat interface designation FOCIS 18P-2x16-1-0-2-2. The MDI shall optically mate with the plug on the optical fiber cabling. Figure xx-c shows an MPO-16 female plug connector with flat interface, and an MDI.

The MDI connection shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2.

NOTE— Transmitter compliance testing is performed at TP2 as defined in xx.k.j, not at the MDI.

Editor's note: ANSI/TIA-604-18 presently entering third ballot.
IEC has not yet initiated ballot on the equivalent connector.

MDI (4 of 4)



MPO-16 female plug connector flat interface

MDI

Figure xx-c – MPO-16 female plug connector flat interface and MDI

Editor's note: Figure is in public domain so may be used "as is". It is also acceptable redrawn in a form like Figure 86-8 with keying adjustment.

Further work

- The PMD target BER is likely to deviate from $5x10^{-5}$, so some fine tuning of parameters may be required.
  - The project's choice of FEC will determine the pre-FEC BER target, and may also affect the exact signaling rate.
- Confirm skew budget

400G-PSM4: A Proposal for the 500m Objective using 100 Gb/s per Lane Signaling

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Jeff Twombly (Credo)
Ralf-Peter Braun (Deutsche Telekom)

400G-PSM4

- Proposal: A 4x100 Gb/s parallel SMF interconnect to satisfy the 500m objective.
- Lane Speed: 100 Gb/s per lane using 50 GBaud-PAM4 optical signaling
- Single wavelength solution

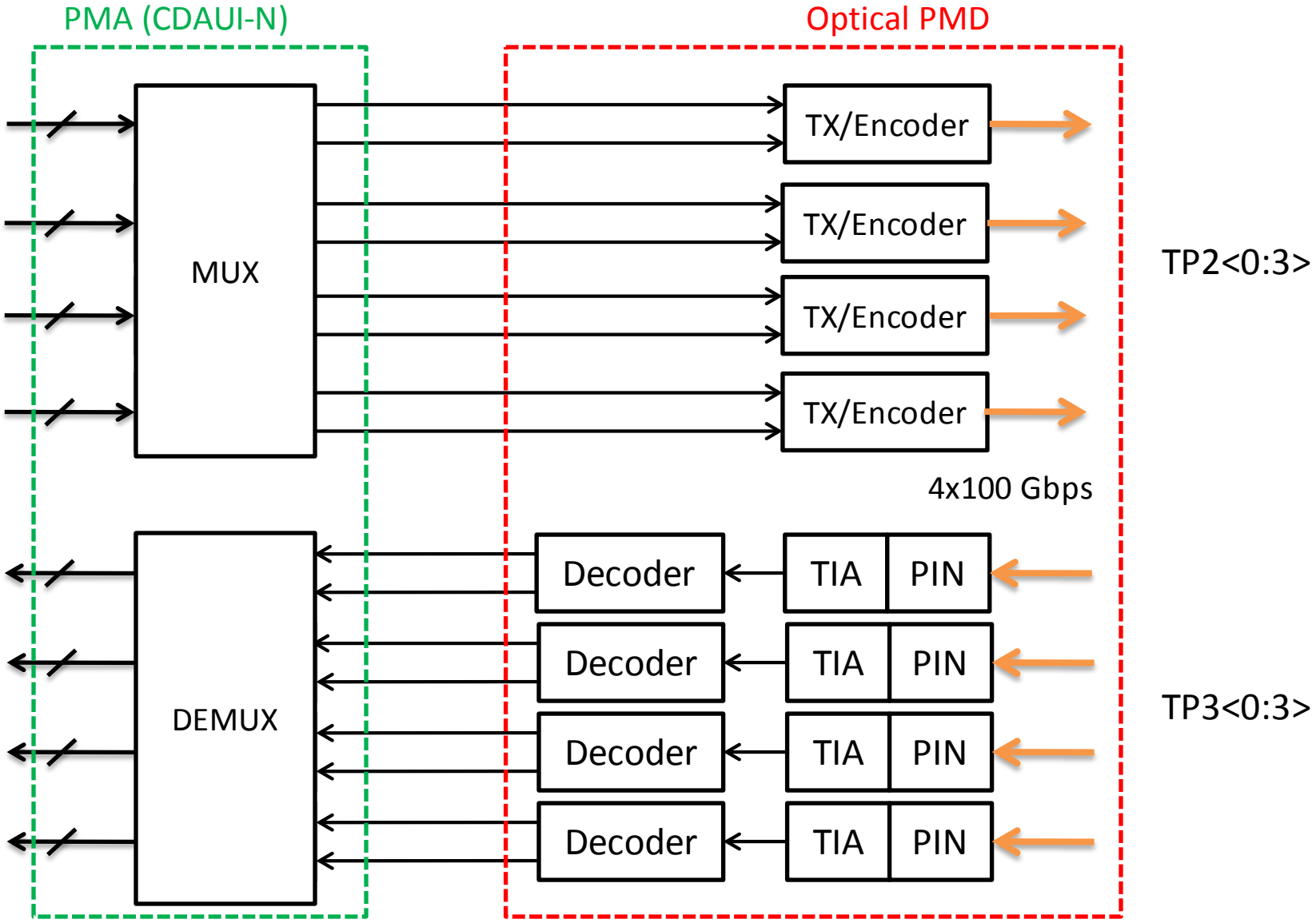
Updates Since Last Meeting

- Went to a "flat" specification
  - Single value OMA and Sensitivity across 13nm optical window
  - "Contoured" specification moved to Appendix
- Reduced TDP max from 3.5 dB to 2.5 dB
  - OMA max reduced to **4.2**dB (consistent with TDP max reduction)
- BER revised from 2.3e-4 to 2.0e-4
- Relabeled illustrative link budget slide
- Revisions from welch_3bs_01_0715 in **Purple**.

Motivations for Changes

- Several requests for “Flat” specification:
  - Makes spec easier to understand
  - Simplifies testing
  - Still provides ample wavelength tolerance for uncooled operation
    - Same width as a “CWDM laser”
- TDP value had been a holdover from 100G specification
  - Requests received to reduce for 400G
  - Relaxes receiver design (eye shape and max power)

400G-PSM4 Block Diagram



400G-PSM4 : Link Parameters

	400G-PSM4
Reach, min (m)	500
Signaling rate, each lane (Range)	53.125 ± 100 ppm GBd
Encoding type	PAM4
Wavelength(s)	1304.5 to 1317.5 nm
Operating BER[Ғ]	2.0e-4
Channel insertion loss, max (dB)[†]	3.0
Allocation for penalties, at max TDP (dB)[‡]	3.0
Power margin, at min TDP (dB)[ҒҒ]	9.25
Maximum discrete reflectance (dB)	-35

Ғ The exact operating BER will be determined by the final FEC and PMA definition

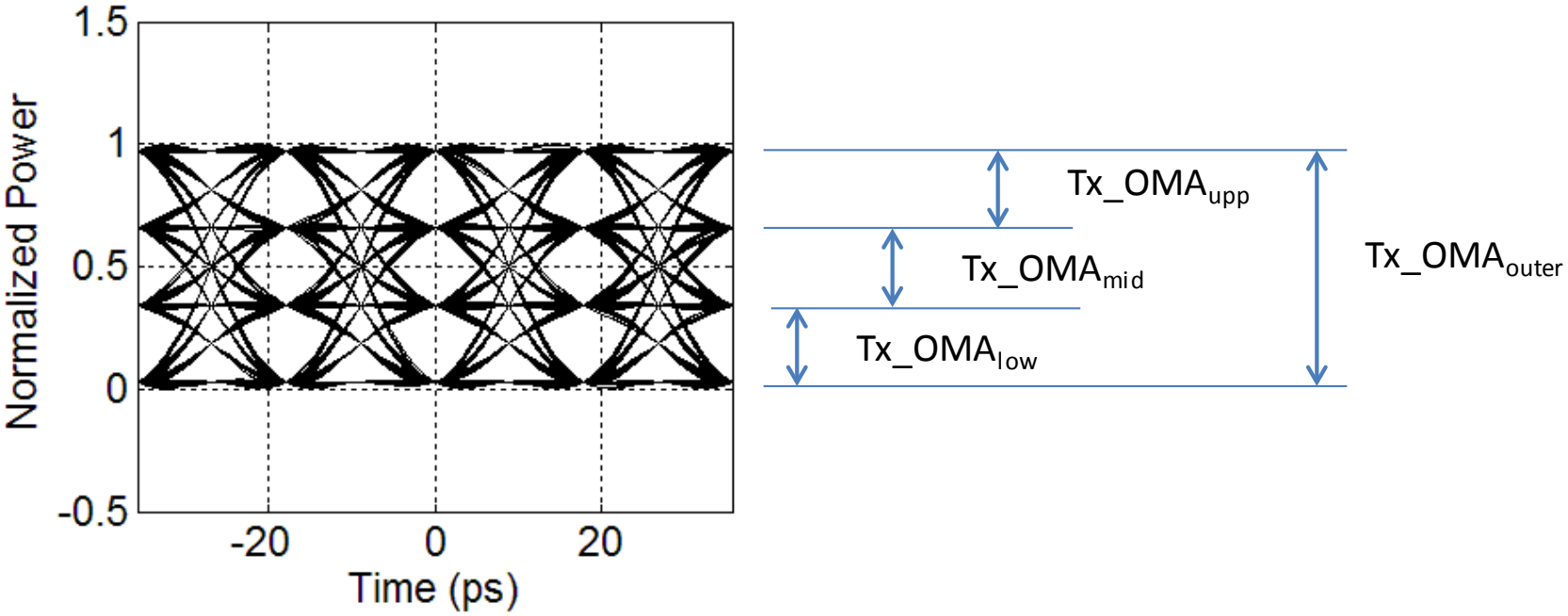
† From http://www.ieee802.org/3/bs/public/14_05/kolesar_3bs_01_0514.pdf

‡ Sum of Max TDP (2.5 dB) and MPI penalty (0.5 dB)

ҒҒ Power Margin, at min TDP = Modulation Penalty + Channel Loss + MPI + TDP Min + Unallocated Margin

All Parameters Subject to Change in Task Force Review

Transmitter Specifications



- Max OMA and ER specified based on outer Tx_OMA_{outer}
- Sensitivity and link budget based on inner $Tx\_OMA_{low/mid/upp}$
  - Spec applies to minimum of 3 inner eye transitions

400G-PSM4: Transmitter Specifications (TP2)

	400G-PSM4
Signaling rate, each lane (Range)	53.125 ± 100 ppm GBd
Encoding type	PAM4
Wavelength(s)	1304.5 to 1317.5 nm
OMA_{outer}, each lane, max (dBm)	**4.2**
OMA_{outer}, each lane, min (dBm)	0†
$OMA_{low/mid/upp}$, each lane, min (dBm)	-4.8†
Launch Power in $OMA_{low/mid/upp}$ – TDP, each lane (min) (dBm)	**-5.6**
Transmitter and dispersion penalty, (TDP) each lane (max) (dBm)	2.5
ER_{outer}, each lane, min (dB)	5.0
Average launch power, each lane max (dBm)	4.0
Average launch power, each lane min (dBm)	-2.1‡
Transmitter RIN_{ave}, max (dB/Hz)	-142
Transmitter reflectance, max (dB)	-20
Transmitter Eye Mask	TBD

All Parameters Subject to Change in Task Force Review

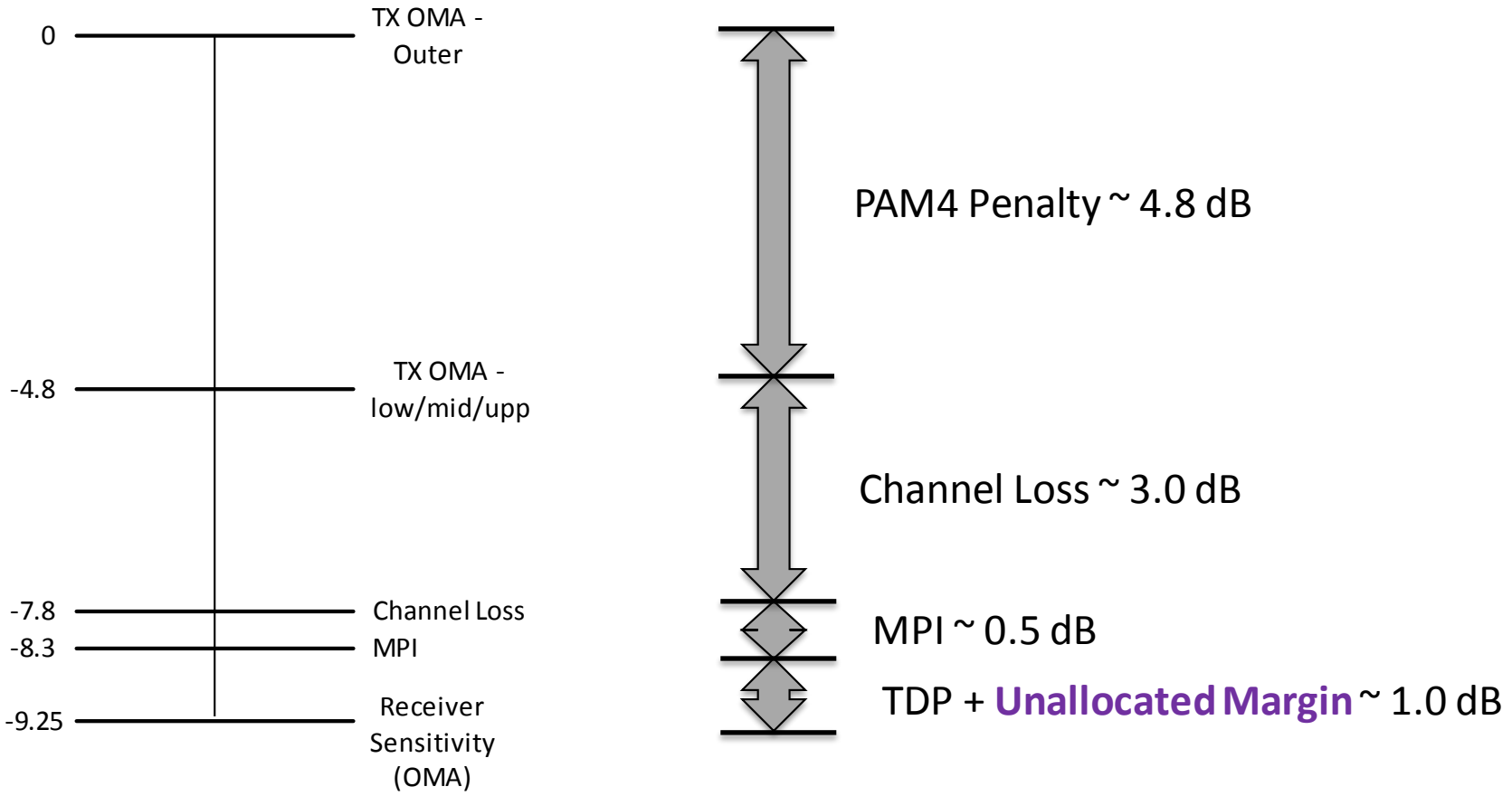
† Even with TDP < 0.8, OMA values must meet or exceed the stated minimums
‡ Assuming Min OMA with ER of 10

400G-PSM4: Receiver Specifications (TP3)

	400G-PSM4
Signaling rate, each lane (Range)	53.125 ± 100 ppm GBd
Encoding type	PAM4
Wavelength(s)	1304.5 to 1317.5 nm
Receiver sensitivity (OMA), each lane max (dBm)†	-9.25
Average receive power, each lane max (dBm)	4.0
Average receive power, each lane min (dBm)	-5.1
Damage threshold (dBm)	6.5
Receiver reflectance, max (dB)	-26
Stressed receiver sensitivity (OMA), each lane max (dBm)	TBD
Conditions of stressed receiver sensitivity test:	
Vertical eye closure penalty, each lane (dB)	TBD
Stressed eye J2 Jitter, each lane (UI)	TBD
Stressed eye J4 Jitter, each lane (UI)	TBD
Stressed eye mask definition	TBD

† Received sensitivity reported in 'NRZ mode' and uncorrected BER, equivalent to sensitivity for any sub-eye low/mid/upp
All Parameters Subject to Change in Task Force Review

400G-PSM4 Link Budget (at TDP = 0.8 dB)



† Received sensitivity reported in 'NRZ mode' and uncorrected BER, equivalent to sensitivity for any sub-eye low/mid/upp
All Parameters Subject to Change in Task Force Review

400G-PSM4

- Proposal: A 4x100 Gb/s parallel SMF interconnect to satisfy the 500m objective.
- Lane Speed: 100 Gb/s per lane using 50 GBaud-PAM4 optical signaling
- Single wavelength solution

Appendix

PSM4 with “contoured” TX/RX specifications

400G-PSM4: Transmitter Specifications (TP2)

	400G-PSM4
Signaling rate, each lane (Range)	53.125 ± 100 ppm GBd
Encoding type	PAM4
Wavelength(s)	1297 to 1323 nm
OMA_{outer}, each lane, max (dBm)	$MAX(3.8+(\lambda-1310)^2/70,4.3)$
OMA_{outer}, each lane, min (dBm)	$MAX(-1.3+(\lambda-1310)^2/70,-0.8)+MAX(TDP,0.8)$
$OMA_{low/mid/upp}$, each lane, min (dBm)	$MAX(-6.07+(\lambda-1310)^2/70,-5.57)+MAX(TDP,0.8)$
ER_{outer}, each lane, min (dB)	5.0
Average launch power, each lane max (dBm)	4.0
Average launch power, each lane min (dBm)	$MAX(-3.4+(\lambda-1310)^2/70,-2.9)+0.8$
TDP, each lane, max (dB)	2.5
Transmitter RIN_{ave}, max (dB/Hz)	-142
Transmitter reflectance, max (dB)	-20
Transmitter Eye Mask	TBD

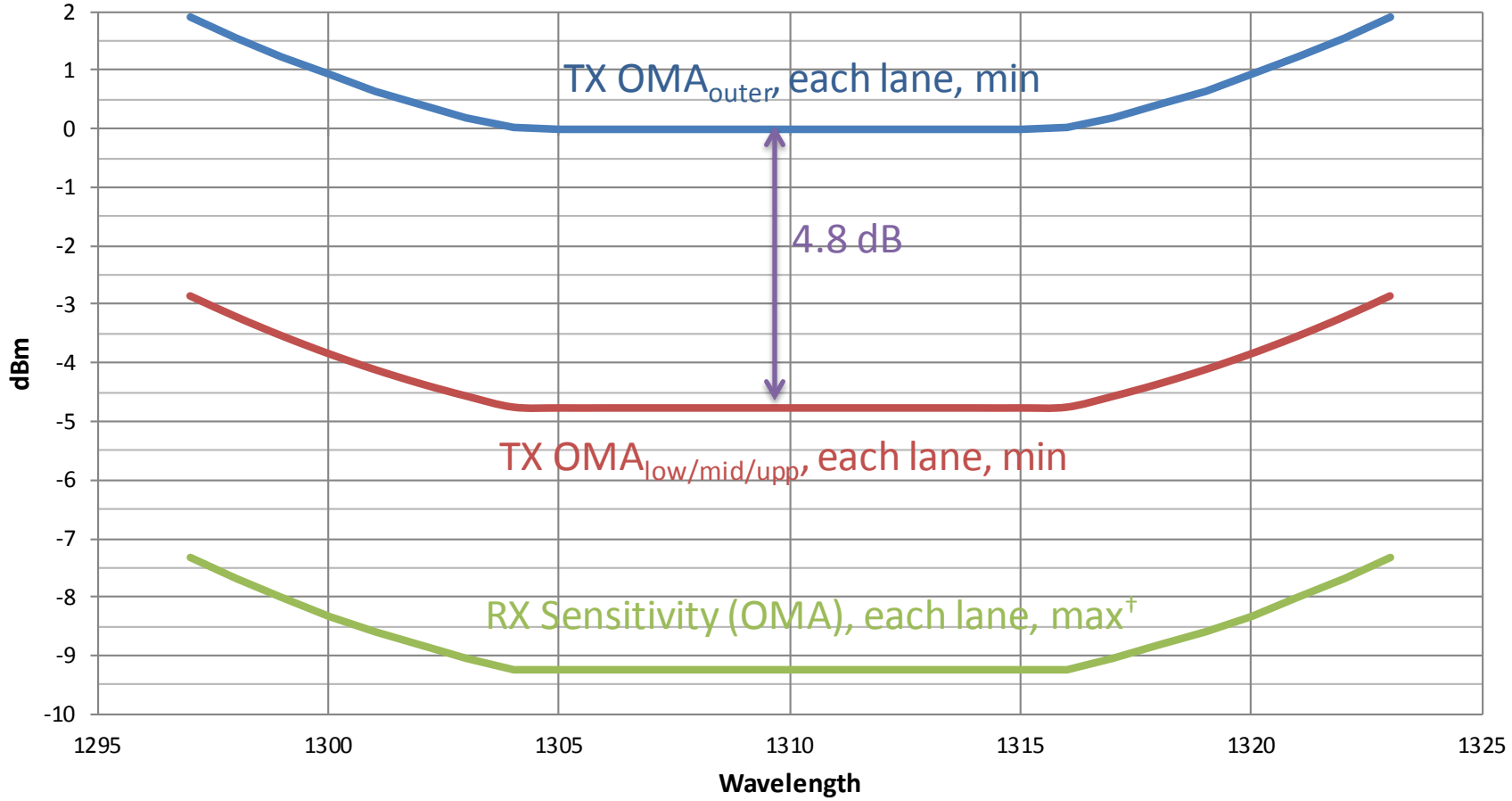
All Parameters Subject to Change in Task Force Review

400G-PSM4: Receiver Specifications (TP3)

	400G-PSM4
Signaling rate, each lane (Range)	53.125 ± 100 ppm GBd
Encoding type	PAM4
Wavelength(s)	1297 to 1323 nm
Receiver sensitivity (OMA), each lane max (dBm)†	MAX(-9.75+(λ-1310)^2/70,-9.25)
Average receive power, each lane max (dBm)	4.0
Average receive power, each lane min (dBm)	-5.1
Damage threshold (dBm)	6.5
Receiver reflectance, max (dB)	-26
Stressed receiver sensitivity (OMA), each lane max (dBm)	TBD
Conditions of stressed receiver sensitivity test:	
Vertical eye closure penalty, each lane (dB)	TBD
Stressed eye J2 Jitter, each lane (UI)	TBD
Stressed eye J4 Jitter, each lane (UI)	TBD
Stressed eye mask definition	TBD

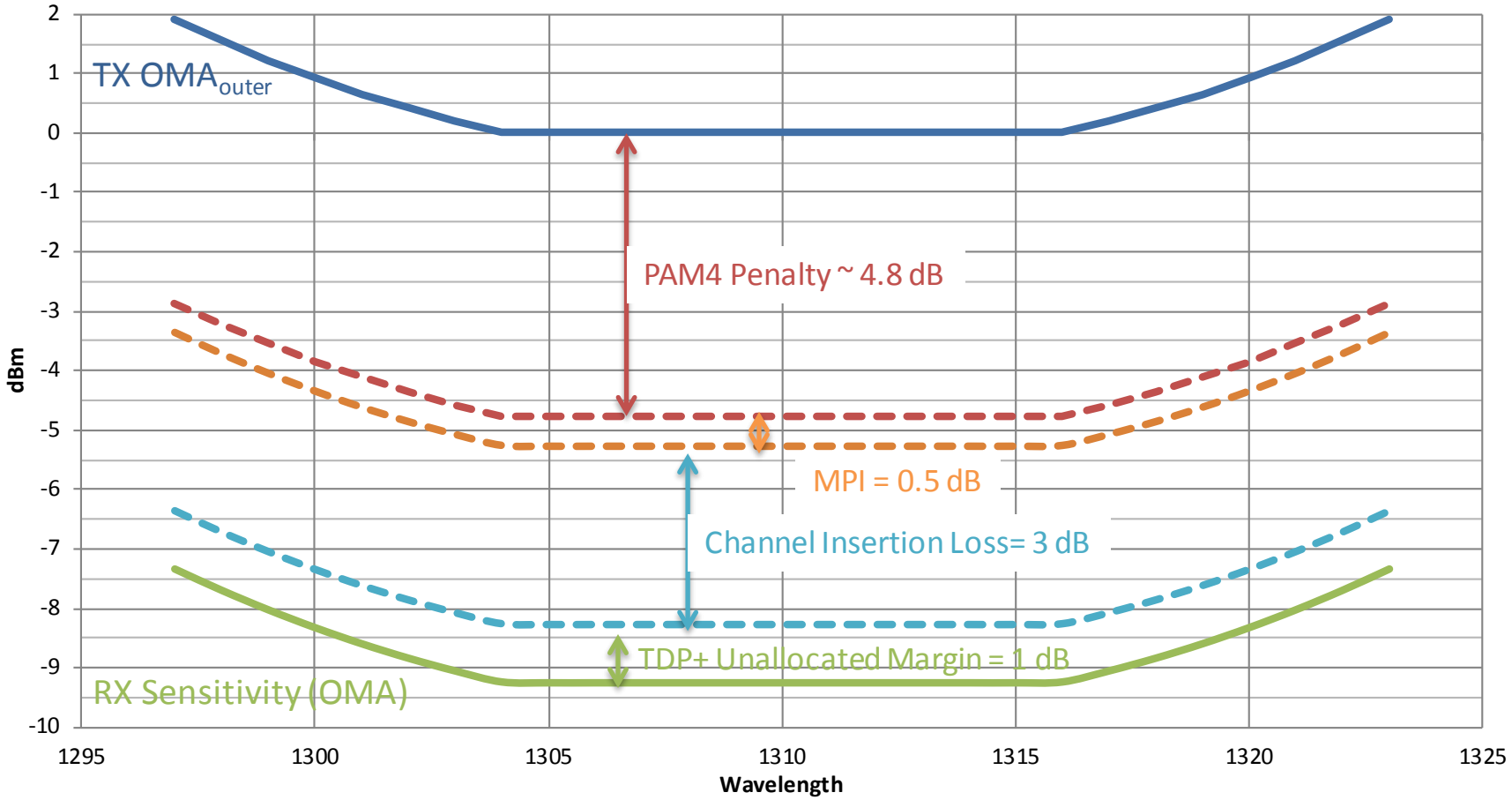
† Received sensitivity reported in 'NRZ mode' and uncorrected BER, equivalent to sensitivity for any sub-eye low/mid/upp
All Parameters Subject to Change in Task Force Review

400G-PSM4 Specifications



† Received sensitivity reported in 'NRZ mode' and uncorrected BER, equivalent to sensitivity for any sub-eye low/mid/upp
All Parameters Subject to Change in Task Force Review

400G-PSM4 Link Budget (at TDP = 0.8 dB)



† Received sensitivity reported in 'NRZ mode' and uncorrected BER, equivalent to sensitivity for any sub-eye low/mid/upp
All Parameters Subject to Change in Task Force Review

400Gb/s 8x50G PAM4 WDM 2km SMF PMD Baseline Specifications

P802.3bs 400 Gb/s Ethernet Task Force

IEEE 802 Plenary Session

13 – 15 July 2015

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- Vasudevan Parthasarathy, Broadcom
- Rick Pimpinella, Panduit
- Michael Ressl, Hitachi Cable
- Steve Swanson, Corning
- Jeff Twombly, Credo

Select References

- June 2015: 8x50G PAM4 2km SMF PMD Discussion

  http://www.ieee802.org/3/bs/public/adhoc/smf/15_06_09/cole_01a_0615_smf.pdf
- June 2015: 8x50G PAM4 2km duplex SMF Considerations

  http://www.ieee802.org/3/bs/public/adhoc/smf/15_06_09/stassar_01_0615_smf.pdf
- May 2015: 8x50G PAM4 WDM Baseline Specifications

  http://www.ieee802.org/3/bs/public/15_05/cole_3bs_01a_0515.pdf
- Sept. 2014: 8x50G WDM Technology Background

  http://www.ieee802.org/3/bs/public/14_09/stassar_3bs_01b_0914.pdf
- BTI

  http://www.ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf#page=19

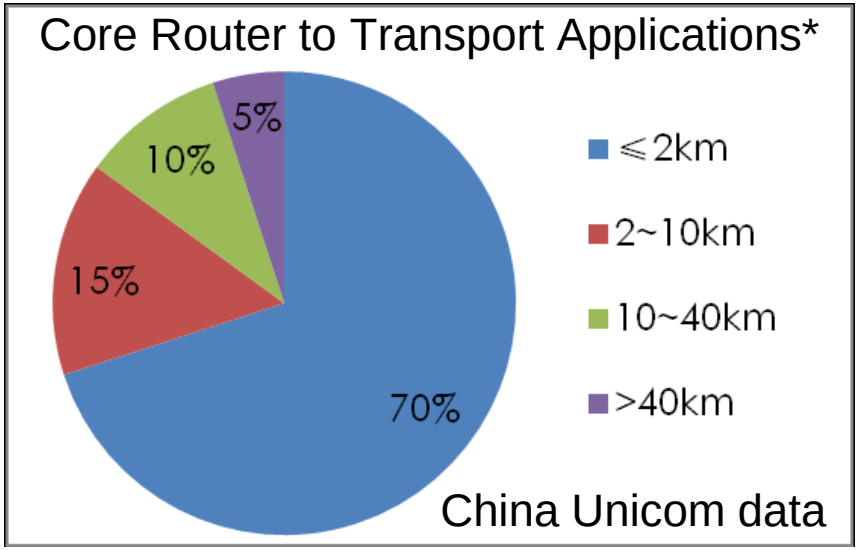
Introduction

- 8x50G PAM4 WDM 10km specs in cole_3bs_01a_0515 were adopted for the 10km reach SMF PDM objective

  http://www.ieee802.org/3/bs/public/15_05/motions_3bs_01_0515.pdf#page=10

- Adopting 8x50G PAM4 WDM 2km PMD based on existing technology will provide a cost effective solution for majority of core routing applications and result in a solid standard

- 400Gb/s Ethernet early adopters want standards based, interoperable 2km & 10km interfaces, supporting predictable development and build-out of 400Gb/s networks



* http://www.ieee802.org/3/400GSG/public/13_11/song_x_400_01a_1113.pdf#page=6

Transmit Characteristics

Description (Outer Eye)	Proposed 400GBASE-FR8	*Adopted 400GBASE-LR8*	Unit
Reach	2	*10*	km
Signaling Rate, each lane	26.6	*26.6*	GBd
Operating BER*	2.0E-04	*2.0E-04*	
Total average launch power (max)	13.2	*13.2*	dBm
OMA, each lane (max)	5.5	*5.7*	dBm
OMA, each lane (min)	0.0	*0.5*	dBm
Launch Power in OMA – TDP, each lane (min)	-1.0	*-0.5*	dBm
Transmitter and dispersion penalty, (TDP) each lane (max)	2.0	*2.2*	dB
Extinction ratio (ER) (min)	4.5	*4.5*	dB
RIN OMA (max)	TBD	*TBD*	dB/Hz
Optical return loss tolerance (max)	TBD	*TBD*	dB

* The exact operating BER will be determined by the final FEC and PMA definition

Receive Characteristics

Description (Inner Eye)	Proposed 400GBASE-FR8	*Adopted 400GBASE-LR8*	Unit
Signaling Rate, each lane	26.6	*26.6*	GBd
Operating BER*	2.0E-04	*2.0E-04*	
Receiver reflectance (max)	TBD	*TBD*	dB
Receiver Sensitivity (OMA), each lane (max)	-10.0	*-11.8*	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane (max)	21.0	*21.0*	GHz
Stressed receiver sensitivity (OMA), each lane (max)	TBD	*TBD*	dBm
Conditions of stressed receiver sensitivity test	TBD	*TBD*	

* The exact operating BER will be determined by the final FEC and PMA definition

Illustrative Link Power Budgets

Parameter	Proposed 400GBASE-FR8	*Adopted 400GBASE-LR8*	Unit
Reach	2	*10*	km
Power Budget (for maximum TDP)	11.0	*13.5*	dB
Operating Distance	2.0	*10.0*	km
Channel Insertion Loss	4.0	*6.3*	dB
Maximum Discrete Reflectance	TBD	*TBD*	dB
Allocation for Penalties* (for maximum TDP)	2.0	*2.2*	dB
Allocation for Modulation Penalties	5.0	*5.0*	dB

* Includes MPI penalty. As with all other parameters, it is subject to change in Task Force review.

WDM Lane Assignments

Lane	Center Frequency THz	Center Wavelength nm	Wavelength Range nm
L0	235.4	1273.55	1272.55 to 1274.54
L1	234.6	1277.89	1276.89 to 1278.89
L2	233.8	1282.26	1281.25 to 1283.28
L3	233.0	1286.66	1285.65 to 1287.69
L4	231.4	1295.56	1294.53 to 1296.59
L5	230.6	1300.05	1299.02 to 1301.09
L6	229.8	1304.58	1303.54 to 1305.63
L7	229.0	1309.14	1308.09 to 1310.19

Optical Margin

Description (Inner Eye)	Proposed 400GBASE-FR8	*Adopted 400GBASE-LR8*	Unit
Receiver Sensitivity (OMA), each lane, pre-DeMux (max)	-10.0	*-11.8*	dBm
DeMux Loss	3.0	*3.0*	dB
Cross-talk penalty	0.3	*0.3*	dB
Receiver Sensitivity (OMA), each lane, post-DeMux (max)	-13.3	*-15.1*	dBm
Receiver Sensitivity (OMA) single lane (typical measured)	-17	*-17*	dBm
Optical Margin	3.7	*1.9*	dB

Recommendations

- Adopt 8x50G PAM4 WDM 2km duplex SMF baseline specifications in this presentation for the P802.3bs 2km SMF PMD objective to enable cost effective solution for majority of applications that do not need 10km link budget
- Develop 2km and 10km SMF PMD specifications to interoperate at 2km reach to enable common deployment, and economies of scale through shared component volume
- Leverage strong synergy between 2km and 10km PMDs for common specification methodology and common compliance testing approach
- All baseline specification parameters will undergo further analysis and are subject to change by the Task Force

Thank you

400Gb/s 2km & 10km duplex SMF PAM-4 PMD Baseline Specifications

400 Gb/s Ethernet Task Force

IEEE 802.3 Interim Meeting

18 – 20 May 2015

Pittsburgh, PA

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Atul Srivastava, NTT Electronics

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Supporters

End Users

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- Martin Carroll, Verizon
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- Lu Huang, China Mobile
- Junjie Li, China Telecom
- Ichiro Ogura, PETRA
- Sam Sambasivan, ATT
- Shikui Shen, China Unicom
- Masahito Tomizawa, NTT
- Guangquann Wang, China Unicom
- Haiyi Zhang, CAICT (CATR)
- Glenn Wellbrock, Verizon
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System OEMs

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- Marc Bohn, Coriant
- Ayla Chang, Huawei
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- Eric Hall, Aurrion
- Jonathan Ingham, Avago
- Jonathan King, Finisar
- Robert Lingle, Jr., OFS
- Alan McCurdy, OFS
- Vasudevan Parthasarathy, Broadcom
- Rick Pimpinella, Panduit

Select Preceding References

- Sept. 2014: 8x50G WDM Technology background

  http://www.ieee802.org/3/bs/public/14_09/stassar_3bs_01b_0914.pdf

- Nov. 2014: Nominal Specifications

  http://www.ieee802.org/3/bs/public/14_11/cole_3bs_02a_1114.pdf

- Jan. 2015: Updated Nominal Specifications

  http://www.ieee802.org/3/bs/public/15_01/cole_3bs_02_0115.pdf

- BTI

  http://www.ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf#page=13

  http://www.ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf#page=19

Discussion

- During the March 2015 P802.3bs TF meeting 50G PAM-4 RX Sens. (inner eye OMA) data was presented
  - Finisar RX Sens. = ~-13.5dBm (BER = 2e-4)

    http://www.ieee802.org/3/bs/public/15_03/cole_3bs_02_0315.pdf#page=24
  - Huawei RX Sens. = ~-18dBm (BER = 2e-4)

    http://www.ieee802.org/3/bs/public/15_03/stassar_3bs_01a_0315.pdf#page=5
- Since the meeting, below deltas were identified:

Parameter	Finisar	Huawei
Noise Current	16.5pA/√HZ	15pA/√HZ
PD responsivity	0.5A/W	0.85A/W
Pattern	SSPR	PRBS15
GBaud	28	25.8

- With 0.8A/W PD responsivity, Finisar has since measured RX Sens. = ~-17dBm (BER = 2e-4)

Discussion, cont.

- -17 to -18dBm OMA RX Sens. enables 2km and 10km 8x50G PAM-4 PMDs using PIN PD RX
- Optical margin for 2km PMD results in sufficiently high manufacturing yield
- Optical margin for 10km PMD results in lower manufacturing yield
- Manufacturing a combination of 2km and 10km PMDs results in sufficiently high yield
- 25G linear APD technology when commercialized will have acceptable stand-alone 10km PMD manufacturing yield, although at a higher cost than PIN PD

Transmit Characteristics

Description (Outer Eye)	400GBASE-FR8	400GBASE-LR8	Unit
Reach	2	10	km
Signaling Rate, each lane	26.6	26.6	GBd
Operating BER*	2.0E-04	2.0E-04	
Total average launch power (max)	13.2	13.2	dBm
OMA, each lane (max)	5.5	5.7	dBm
OMA, each lane (min)	0.0	0.5	dBm
Launch Power in OMA – TDP, each lane (min)	-1.0	-0.5	dBm
Transmitter and dispersion penalty, (TDP) each lane (max)	2.0	2.2	dB
Extinction ratio (ER) (min)	4.5	4.5	dB
RIN OMA (max)	TBD	TBD	dB/Hz
Optical return loss tolerance (max)	TBD	TBD	dB

* The exact operating BER will be determined by the final FEC and PMA definition

Receive Characteristics

Description (Inner Eye)	400GBASE-FR8	400GBASE-LR8	Unit
Signaling Rate, each lane	26.6	26.6	GBd
Operating BER*	2.0E-04	2.0E-04	
Receiver reflectance (max)	TBD	TBD	dB
Receiver Sensitivity (OMA), each lane (max)	-10.0	-11.8	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane (max)	21.0	21.0	GHz
Stressed receiver sensitivity (OMA), each lane (max)	TBD	TBD	dBm
Conditions of stressed receiver sensitivity test	TBD	TBD	

* The exact operating BER will be determined by the final FEC and PMA definition

Illustrative Link Power Budgets

Parameter	400GBASE-FR8	400GBASE-LR8	Unit
Reach	2	10	km
Power Budget (for maximum TDP)	11.0	13.5	dB
Operating Distance	2.0	10.0	km
Channel Insertion Loss	4.0	6.3	dB
Maximum Discrete Reflectance	TBD	TBD	dB
Allocation for Penalties* (for maximum TDP)	2.0	2.2	dB
Allocation for Modulation Penalties	5.0	5.0	dB

* Includes MPI penalty. As with all other parameters, it is subject to change in Task Force review.

WDM Lane Assignments

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L5	230.6	1300.05	1299.02 to 1301.09
L6	229.8	1304.58	1303.54 to 1305.63
L7	229.0	1309.14	1308.09 to 1310.19

Optical Margin

Description (Inner Eye)	400GBASE-FR8	400GBASE-LR8	Unit
Receiver Sensitivity (OMA), each lane, pre-DeMux (max)	-10.0	-11.8	dBm
DeMux Loss	3.0	3.0	dB
Cross-talk penalty	0.3	0.3	dB
Receiver Sensitivity (OMA), each lane, post-DeMux (max)	-13.3	-15.1	dBm
Receiver Sensitivity (OMA) single lane (typical measured)	-17	-17	dBm
Optical Margin	3.7	1.9	dB

Recommendations

- Adopt 8x50G PAM-4 WDM duplex SMF architecture for P802.3bs 2km and 10km SMF PMD objectives as per baseline specifications in this presentation
- Develop the 2km and 10km specifications so that 10km is a higher performance variant of the 2km specification and can be built from upper end of the performance distribution of 2km PMD optical components
- Develop the 10km specification to be compatible with linear APD receivers
- All baseline specification parameters will undergo further analysis and are subject to change by the Task Force

2km & 10km PAM-4 PMD Baseline Specs

Thank you