Extended & Retracted Power v121

Lennart Yseboodt, Matthias Wendt (Philips)
Yair Darshan (Microsemi)
Philips Research
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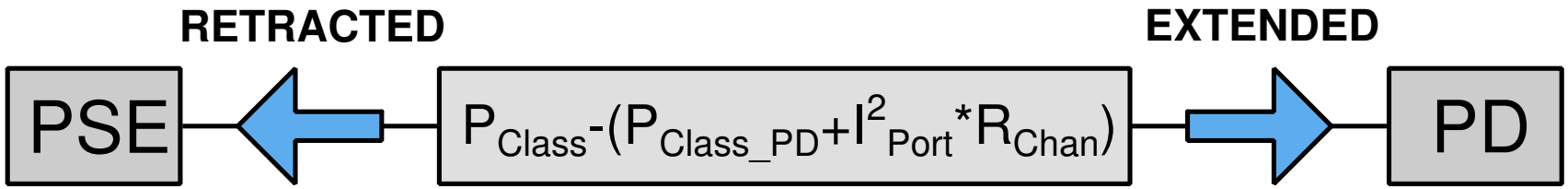
Definitions



Retracted Power: PSEs are allowed to reduce the power allocated (P_{Class}) below the power that would be required to support R_{Chan} = R_{Ch} if the PSE has additional information about the channel.

Extended Power: PDs are allowed to consume the power that the PSE has allocated for channel losses if the PD has additional information about the channel. The PD may not cause the PSE to source more than P_{Class}. This feature is proposed for 802.3bt Type 3 and 4 PSE/PDs.

Both features are useful and should be enabled/possible for bt.

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Retracted power

For a PSE to lower the allocated power below the values in Table 33-7, it needs to know either the actual R_{Chan} or V_{PD}. Due to temperature changes or other dynamic effects[1] this needs to be monitored continuously during POWER_ON stage. The most straightforward way for the PSE to learn V_{PD} is to communicate with the PD over DLL.

The simplest, most robust way for the PSE to perform retracted power is with cooperation (LLDP) from the PD.

[1] Increase in cable temperature increases cable loss, see yseboodt_01_0115.pdf

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Extended power

A PD that consumes more than P_{Class_PD} will need to monitor I_{Port} continuously to make sure power consumption does not exceed the PSE lowerbound template current I_{PSELT} (33-7). To do so the PD needs to know V_{PSE} since it influences I_{PSELT}.

Several methods exist:

- Assume 57V. Very simple, but yields suboptimal power gain.
- Measure V_{PD} at load (optionally correct for rectifier voltage drop).
- Measure V_{PD} at zero-load (provided the PD can control the load).

A PD is capable to perform extended power without cooperation from the PSE using simple measurements (V_{PD} and I_{Port}).

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Conclusion

For Type 3&4, classes 6 and 7, the PD should be allowed to perform extended power without negotiation and the PSE should request (over L2) to perform power retraction because:

- Delivering power is the goal of PoE.
  More power = enable more applications.
- DLL is mandatory for PDs but not for PSEs
- Midspans should be able to support extended power
- PSEs need PD information (over LLDP) anyhow

This will require us to clarify the current text to indicate that a PSE must be able to supply P_{Class} as defined in Table 33-7, regardless of R_{Chan}. To enable retracted power a new LLDP TLV must be defined[2].

[2] Proposed in: yseboodt_04_0115.pdf

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Straw poll 1

For Type 3 and 4 (class 6 and 7):

- PSEs will use LLDP to perform retracted power, LLDP TLVs will be defined to facilitate this
- PDs may perform extended power without making an LLDP request to the PD (to enable extended power also with PSEs that do not support LLDP)

Agree ?

Yes: Abstain: No:

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P_{Class}

$$P_{Class} = \left(V_{PSE} \cdot \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \cdot R_{Chan} \cdot P_{Class\_PD}}}{2 \cdot R_{Chan}} \right) \right) \qquad \text{(Eq. 33-3)}$$

Table 33–7—Physical Layer power classifications (P_{Class})

Class	Minimum power levels at output of PSE (P_{Class})
0	15.4 Watts
1	4.00 Watts
2	7.00 Watts
3	15.4 Watts
4	P_{Type} as defined in Table 33–11
NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–18. NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification.	

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P_{Class}

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

11	Continuous output power capability in POWER_ON state	P_{Con}	W	P_{Class}		1, 2	See 33.2.7.10, Table 33–7.
12	PSE Type power minimum	P_{Type}	W	$I_{Cable} \times (V_{Port\_PSE}$ min)		1, 2	See 33.1.4.

The PSE lowerbound template, I_{PSELT}, is defined by the following segments:

$$I_{PSELT}(t) = \left\{ \begin{array}{ll} I_{LIMmin} & \text{for } (0 \le t < T_{limmin}) \\ I_{Peak} & \text{for } (T_{limmin} \le t < T_{cutmin}) \\ \dfrac{P_{Class}}{V_{PSE}} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_{A} \qquad (33\text{–}7)$$

where

I_{LIMmin}	is the I_{LIM} min value for the PSE (see Table 33–11)
t	is the duration that the PI sources I_{Port}
T_{limmin}	is T_{LIM} min as defined in Table 33–11
T_{cutmin}	is T_{CUT} min, as defined in Table 33–11
I_{Peak}	is I_{Peak}, as defined in Equation (33–4)
P_{Class}	is P_{Class}, as defined in Table 33–7
V_{PSE}	is the voltage at the PSE PI

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