Autoclass Text: Only Sections with Changes are Included.

33.2.6 PSE classification of PDs and mutual identification

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2, Type 3, or Type 4 PD to differentiate between Type 1, Type 2, Type3, and Type4 PSEs. Additionally, mutual identification allows a Type 2, Type 3, or Type 4 PSE to differentiate between Type 1, Type 2, Type 3, and Type 4 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer classification.

Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto the PI and the PD responds with a current representing a limited number of power classifications. Based on the response of the PD, the minimum power level at the output of the PSE is P_{Class} as shown in Equation (33–3). Physical Layer classification encompasses two methods, known as 1-Event Physical Layer classification (see 33.2.6.1) and Multiple-Event Physical Layer classification (see 33.2.6.2).

The minimum power output by the PSE for a particular PD class is defined by Equation (33–3). Alternatively, PSE implementations may use $V_{PSE} = V_{Port\_PSE}$ min and $R_{Chan} = R_{Ch}$ max to arrive at over-margined values as shown in Table 33–7.

<u>If the PD connected to the PSE performs Autoclass (see section 33.3.5.3 and Annex 33-TBD), the PSE may set its minimum power output based on the power drawn during Autoclass.</u>

$$P_{Class} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^{2} - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) \right\}_{W} \qquad (33\text{–}3)$$

where

V_{PSE}	is the voltage at the PSE PI as defined in 1.4
R_{Chan}	is the channel DC pair loop resistance
P_{Class_PD}	is the PD's power classification (see Table 33–18)

Table 33–7—Physical Layer power classifications (P_{Class})

Class	Minimum power levels at output of PSE (P_{Class})
0	15.4 Watts
1	4.00 Watts
2	7.00 Watts
3	15.4 Watts
4	30W or P_{Type} as defined in Table 33–11, whichever is less
5 (4/4/1)	45W or PType as defined in Table 33–11, whichever is less
6 (4/4/2)	60W or PType as defined in Table 33–11, whichever is less
7 (4/4/3)	PType as defined in Table 33–11
NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–18. NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification.	

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 33.6) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation.

A PSE shall meet one of the allowable classification permutations listed in Table 33–8.

Subsequent to successful detection, a Type 1 PSE may optionally classify a PD using 1-Event Physical Layer classification. Valid classification results are Classes 0, 1, 2, 3, and 4, as listed in Table 33–7. If a Type 1 PSE does not implement classification, then the Type 1 PSE shall assign all PDs to Class 0. A Type 1 PSE may optionally implement Data Link Layer classification.

Table 33–8—PSE and PD classification permutations

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	**Physical Layer classification**	**Data Link Layer classification**		
Type 2, Type 3, or Type 4	Multiple-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No[1]	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	Multiple-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

NOTE 1—A Type 3 PSE that is limited to Type 1 power levels can be limited to 1-Event Physical Layer classification without required DLL capability.

Subsequent to successful detection, all Type 2, Type 3, and Type 4 PSEs perform classification using at least one of the following: Multiple-Event Physical Layer classification; Multiple-Event Physical Layer classification and Data Link Layer classification; or 1-Event Physical Layer classification and Data Link Layer classification.

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2, Type 3, or Type 4 PSE shall return to the IDLE state.

33.2.6.2 PSE Multiple-Event Physical Layer classification

When Multiple-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a series of classification and mark events—CLASS_EV1, MARK_EV1, CLASS_EV2, MARK_EV2, CLASS_EV3, MARK_EV3, CLASS_EV4, MARK_EV4, CLASS_EV5, and MARK_EV_LAST—as defined in the state diagram in Figure 33–9.

Type 2 PSEs shall provide a maximum of 2 class and 2 mark events. Type 3 PSEs shall provide a maximum of 4 class and 4 mark events. Type 4 PSEs shall provide a maximum of 5 class and 5 mark events.

A PSE in the state CLASS_EV1 shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{CLE1} in Table 33–10 The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–TBDA1.

A PSE in the state CLASS_EV1_LCF shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{LCF} in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–TBDA1 between 6ms and 75ms after transitioning into the state CLASS_EV1_LCF. The PSE may continue to monitor the current past 75ms in order to determine if the PD will perform Autoclass (see section 33.3.5.3).

When the PSE is in the state MARK_EV1, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV2, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV3, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE3} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK_EV3, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV4, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE3} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK_EV4, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV5, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE3} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK_EV_LAST, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME2} in Table 33–10.

The mark event states, MARK_EV1, MARK_EV2, MARK_EV3, MARK_EV4, and MARK_EV_LAST, commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–17.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min as defined in Table 33–10, a Type 2, Type3, or Type4 PSE shall return to the IDLE state. The class events shall meet the I_{Class_LIM} current limitation. The mark events shall meet the I_{Mark_LIM} current limitation. All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{Port_PSE} in 33.2.3. The PSE shall complete Multiple-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

If the result of the first class event is Class 4, the PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2, Type 3, or Type 4 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 2 PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event. If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 3 or Type 4 PSE treats the PD as a Type 1 PD and shall omit the subsequent mark and class events and classify the PD according to the result of the first class event.

A Type 3 or Type 4 PSE shall skip all subsequent class events and transition directly to Mark_EV_LAST if the class signature detected during CLASS_EV3 is 4. A Type 4 PSE shall skip MARK_EV_4 and CLASS_EV5 and transition directly to Mark_EV_LAST if the class signature detected during CLASS_EV4 is 1 or 2

33.2.8 Power supply allocation

A PSE does not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's class.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See Annex 33-TBD for more information on how Autoclass can be used to manage the allocation of power.

See 33.6 for a description of Data Link Layer classification.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

33.3.5.3 Autoclass

Type 3 and type 4 PDs may choose to implement an extension of Physical Layer classification known as Autoclass. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the PD to which it is connected. Please see Annex 33-TBD for more information on Autoclass.

PDs implementing Autoclass shall not have a class_sig_A of '0'. In addition, PDs implementing Autoclass shall remove its classification current at T_{ACS} resulting in a classification signature of '0' for the remainder of CLASS_EV1. PDs implementing Autoclass carry out the rest of the Physical Layer classification as described in sections 33.3.5.1 or 33.3.5.2.

After power up, PDs implementing Autoclass shall consume their maximum power draw throughout the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2}, measured from when V_{Port_PD} rises above V_{Port_PD} min. The PD shall not draw more power than the power consumed during the time from T_{AUTO_PD1} to T_{AUTO_PD2} plus TBD% at any point until V_{Port_PD} falls below V_{Reset_th}.

Table 33–TBD—Autoclass electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Autoclass Signature Timing	T_{ACS}	ms	77.0	83.0	Measured from transition to state CLASS_EV1
2	Autoclass Power Draw Start	T_{AUTO_PD1}	s		TBD	Measured from when V_{Port_PD} rises above V_{Port_PD} min
3	Autoclass Power Draw End	T_{AUTO_PD2}	s	TBD		Measured from when V_{Port_PD} rises above V_{Port_PD} min

33.3.7.2 Input average power

The maximum average power, P_{Class_PD} in Table 33–18 or PDMaxPowerValue in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below P_{Class_PD} as described in 33.6. PDs may also adjust their maximum required operating power below P_{Class_PD} by using Autoclass (see section 33.3.5.3).

NOTE—Average power is calculated using any sliding window with a width of 1 s.

33.3.7.4 Peak operating power

$V_{Overload}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, the peak power shall not exceed P_{Class_PD} max for more than T_{CUT} min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max.

The RMS, DC and ripple current shall be bounded by Equation (33–10):

Equation 33-10 (No Change)

where

I_{Port}	is the RMS input current
I_{Port_dc}	is the DC component of the input current
I_{Port_ac}	is the RMS value of the AC component of the input current

The maximum I_{Port} value for all operating V_{Port_PD} range shall be defined by the following equation:

$$I_{portmax} = \left\{ \frac{P_{Class\_PD}}{V_{Port\_PD}} \right\}_A \qquad (33–11)$$

where

$I_{portmax}$	is the maximum DC and RMS input current
V_{Port_PD}	is the static input voltage at the PD PI
P_{Class_PD}	is the maximum power, P_{Class_PD} max, as defined in Table 33–18

Peak power, P_{Peak_PD}, for Class 4 is based on Equation (33–12), which approximates the ratiometric peak powers of Class 0 through Class 3. This equation may be used to calculate peak operating power for ~~P_{Peak_PD}~~ P_{Class_PD} values obtained via Data Link Layer classification or Autoclass.

$$P_{Peak\_PD} = \{1.11 \times P_{Class\_PD}\}_W \qquad (33–12)$$

where

$P_{\text{Peak\_PD}}$ is the peak operating power
$P_{\text{Class\_PD}}$ is the input average power

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.