Mark & Hold feasibility study

MIKLOS LUKACS, JUNE 2017

PD disconnect is reliably detectable in the Classification Mark state

Disconnect detection method depends on the Detect – Classification architecture of the PSE

Agenda:

- High level description of architectures available on the market
- Provide solution for both architectures
- Laboratory measurement results

Detect & Classify Hardware variations

- PSE Detect-Class architecture I.
  - Detect: Force current – measure voltage using internal circuits of the PSE controller IC
  - Classify: using the Ext. FET for voltage generation and measure the current on the external 0.25 Ohm resistor
- PSE Detect-Class architecture II.
  - Detect: Force voltage – measure current using internal circuits of the PSE controller IC
  - Classify: using the ‚same' internal voltage source what is used for Detect

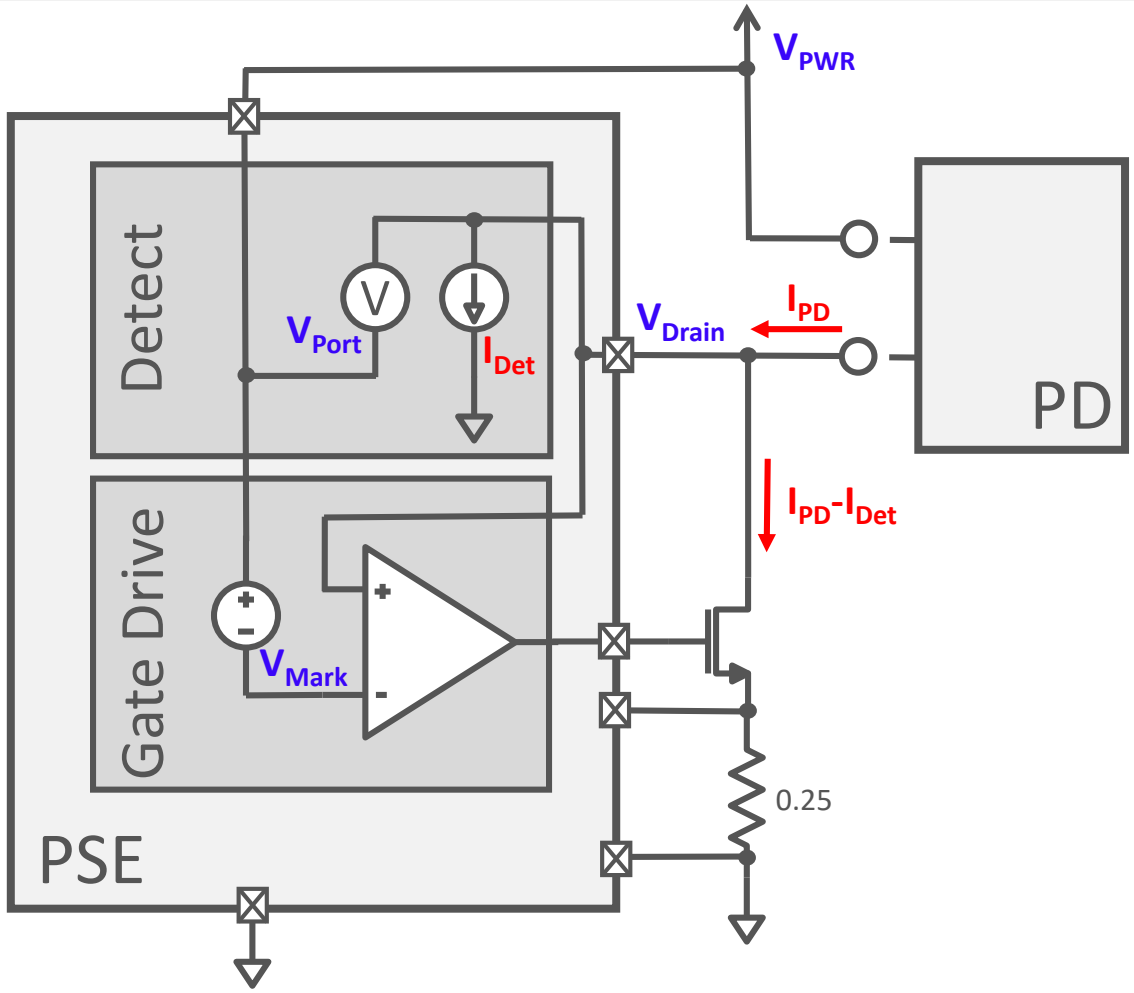
PD Disconnect detection in Mark

- PSE Conditions (Table 145-14):
  - Mark event voltage: $7V < V_{Mark} < 10V$
  - Mark event current: $0.25mA < I_{Mark} < 4mA$
  - Type 1 PDs doing only detect in this voltage range
- Approaches
  - Measure Mark event current
    - Works well with Architecture II. PSEs
      - Sense resistor is >> bigger and internal
    - Not optimal for Architecture I. PSEs
      - Noise, circuit offset voltages
  - Check the voltage on the Drain of the external FET
    - Works well with Architecture I. PSEs
      - Using existing hardware resources only

Check PD disconnect with PSE Detect-Class architecture I.

A voltage output current-comparator can be built:

- Do Detect and Class as Normal
- When in the last Mark
  - Keep forcing V_{Mark}
  - Enable I_{det} (<200uA)
  - Measure V_{Port}
  - Until the PD is disconnected it will draw 250uA min, which allows the Gate Drive loop to operate and set V_{Drain} to V_{Mark}.
  - If the PD is removed then I_{det} pulls V_{Drain} to GND
  - If $V_{Port} > V_{Mark}$ (+margin) then the PD is disconnected

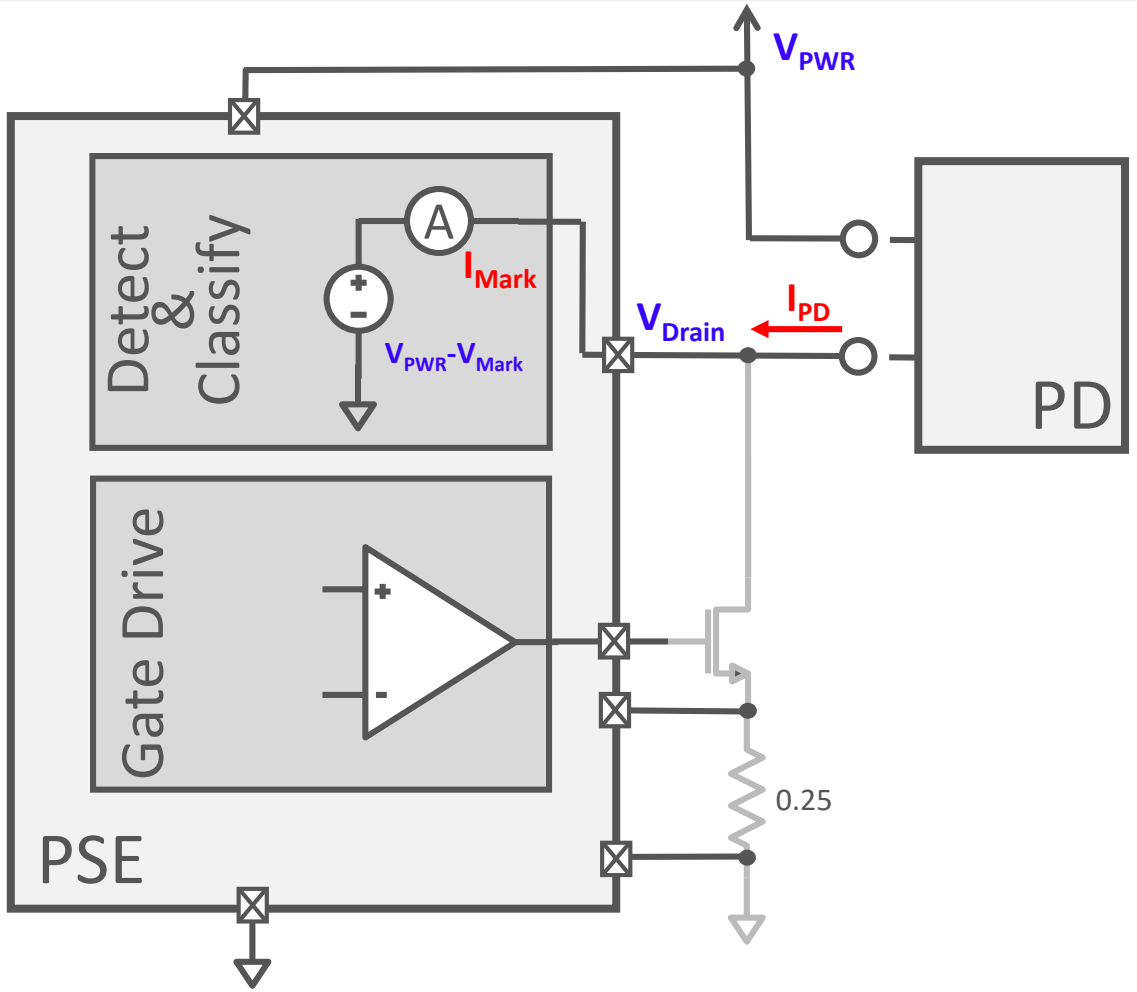


Reminder:

- Detect: Force I – measure V
- Classify: using the Ext. FET

Check PD disconnect with PSE Detect-Class architecture II.

- Do Detect and Class as Normal
- When in the last Mark
  - Keep forcing $\mathbf{V_{PWR}}$-V_{Mark}
  - Measure I_{Mark}
  - If I_{Mark} > 150uA then the PD is disconnected



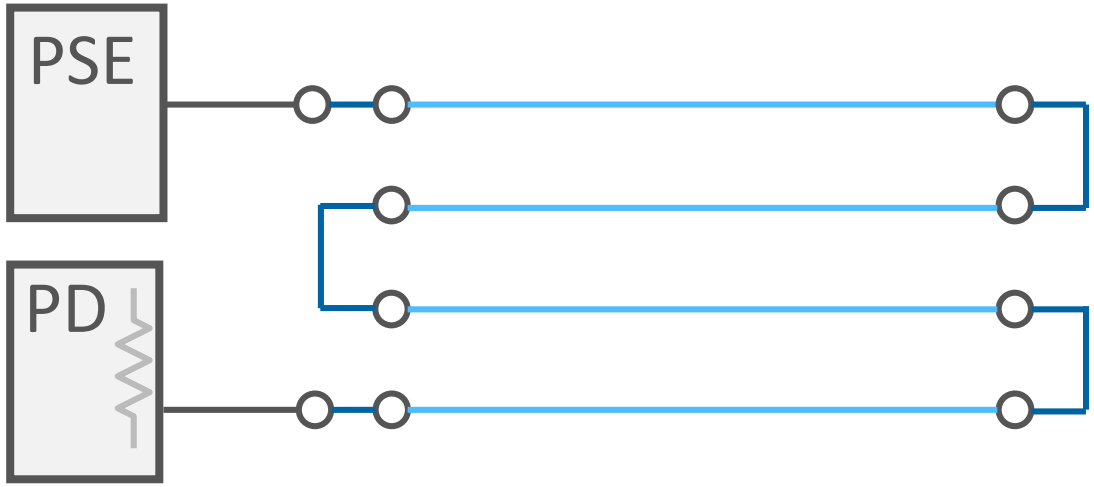
Reminder:

- Detect & Class: Force V – measure I

Lab measurement - Measurement setup

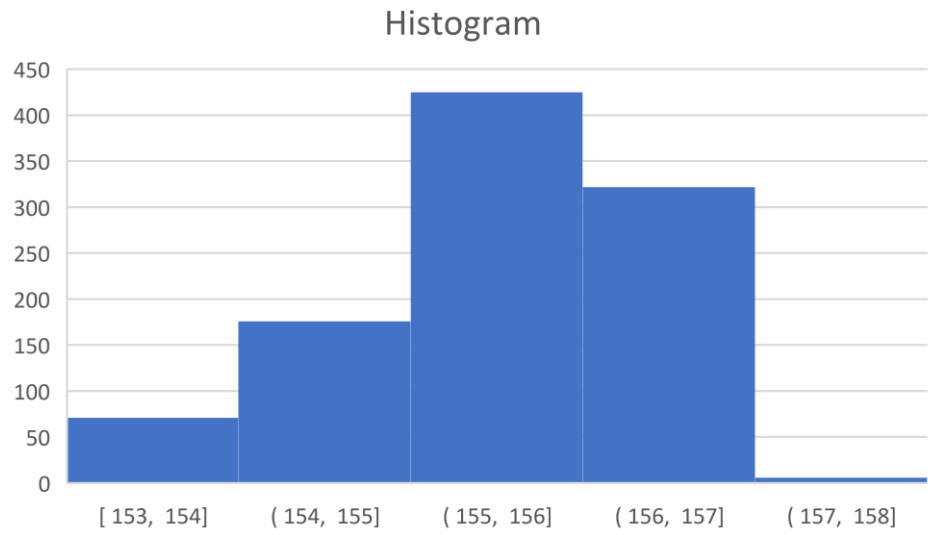
- PD side: resistive load, R = 51kOhm
- PSE side: Silicon Labs Si3459 EVB
  - PI voltage is set to 8V (V_{PWR} = 50V, V_{Drain} = 42V)
  - Calculated current: 156,8uA
  - Mark current is measured by the Si3459, 1000 times
  - Delay between measurements: 50ms

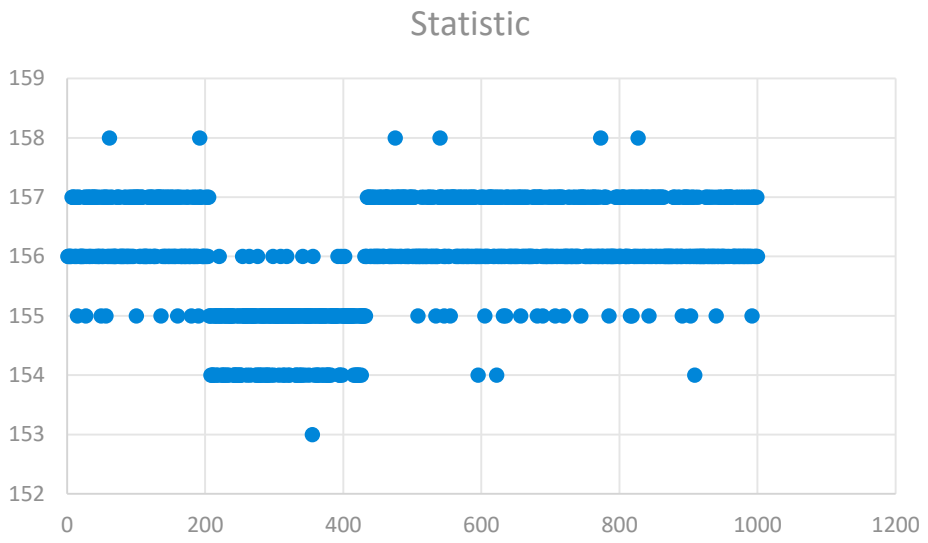
- Cabling A:
  - Short cable (<1m)
- Cabling B
  - Standard office environment
  - 4pcs of Cat5 cables, running parallel from the outlet to the server room
  - mixed with other cable types (power)
  - Each cable is ~30m in length
  - The cables connected serially to form a single cable with ~120m total length



Lab measurement - Measurement result – short cable

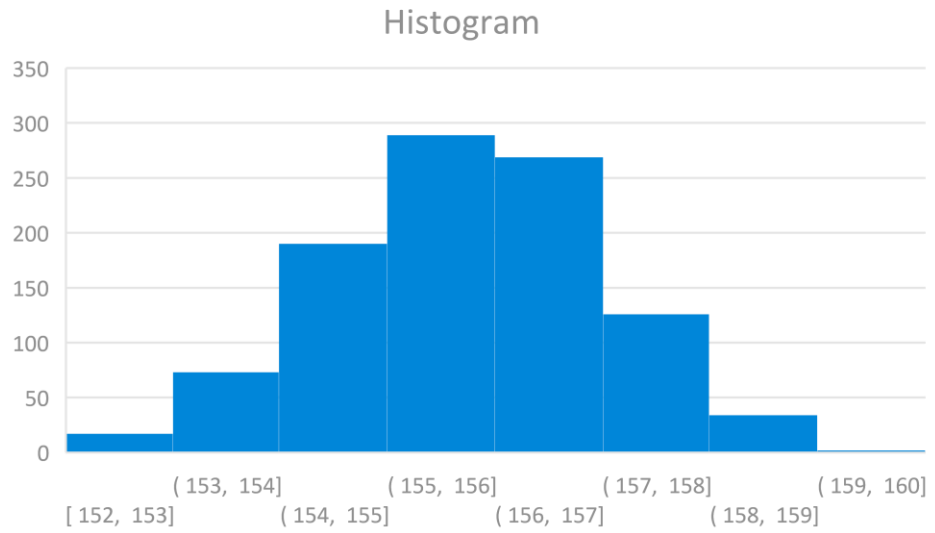
- Measured average current: 156uA
- Standard deviation: 0.9uA

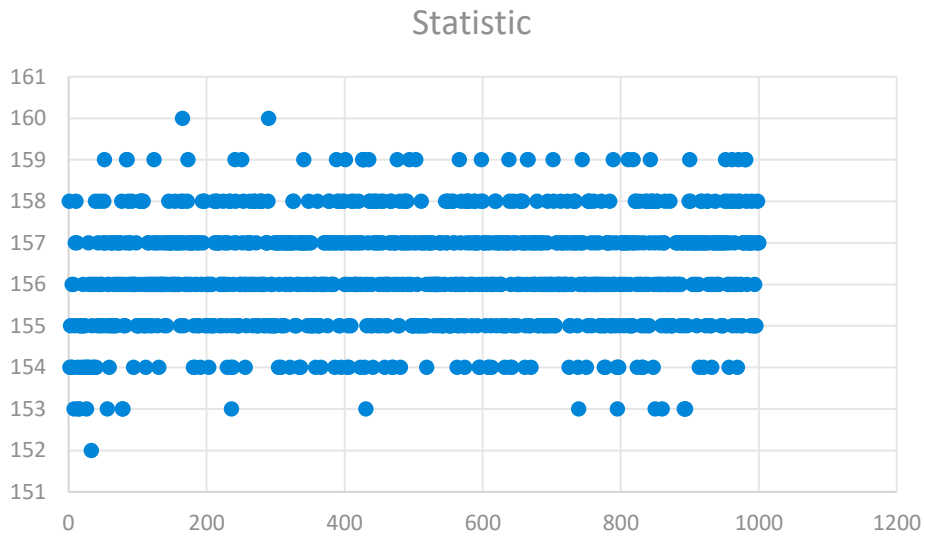




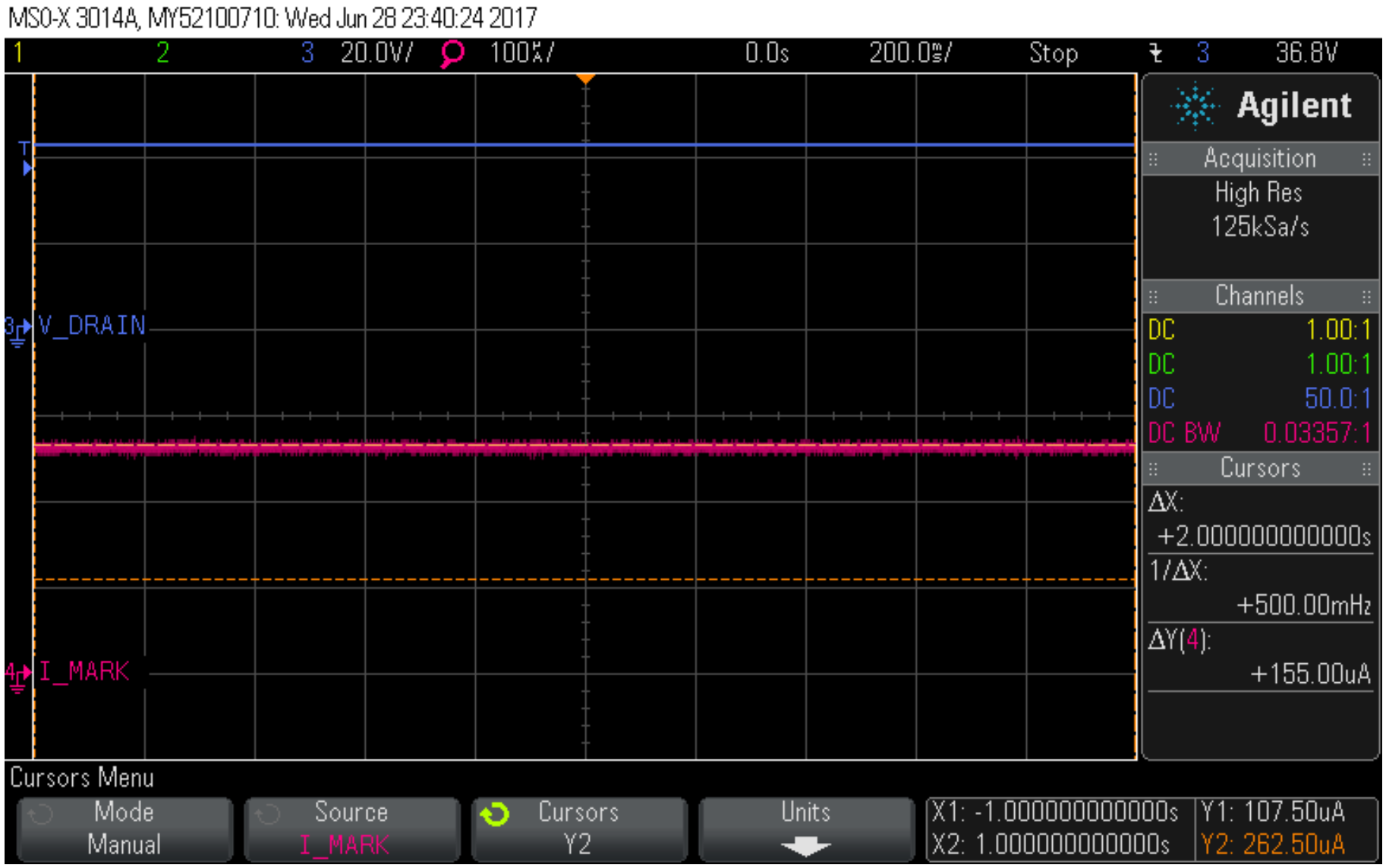
Lab measurement - Measurement result – long cable

- Measured average current: 156.2uA
- Standard deviation: 1.3uA

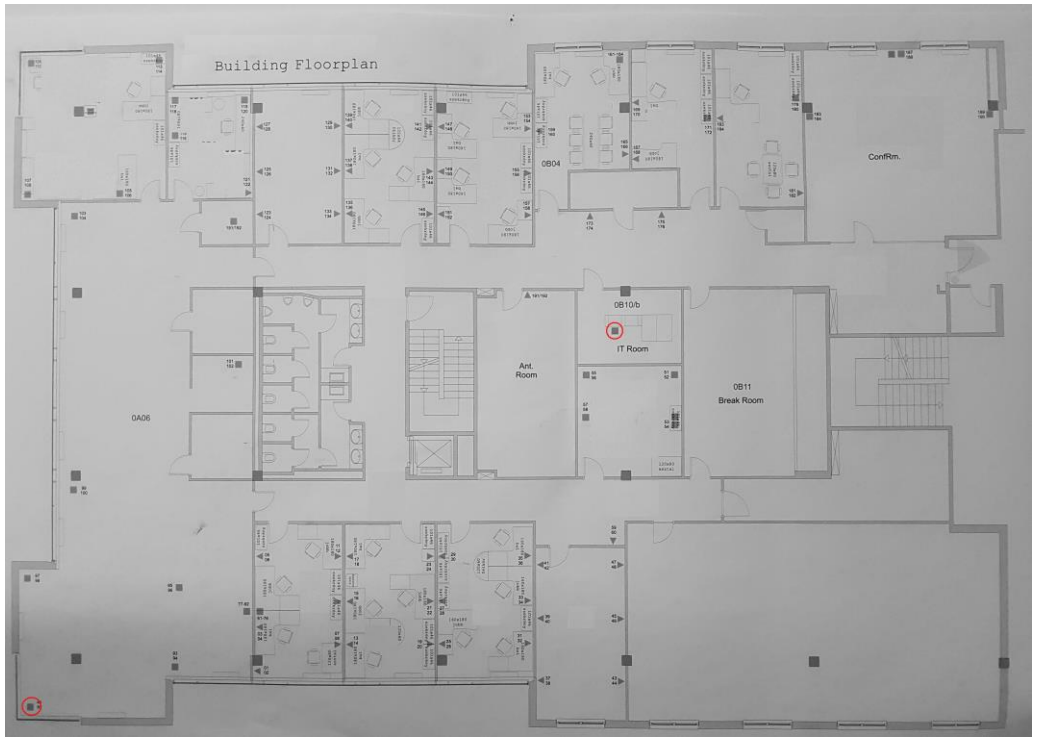


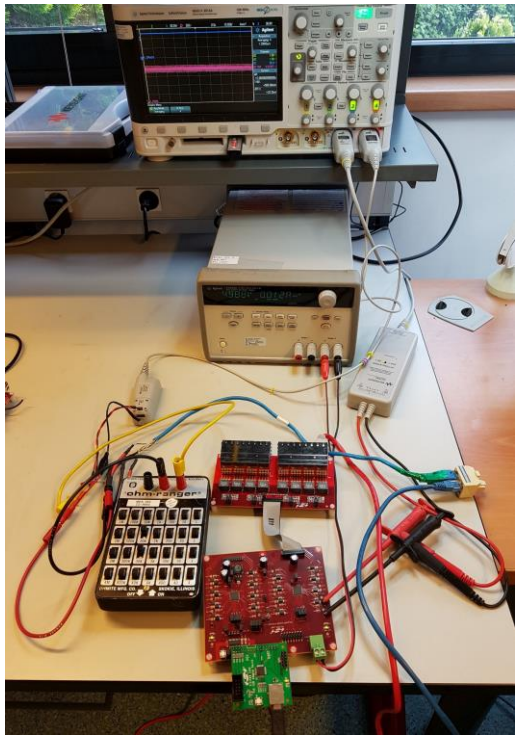


Lab measurement - Oscilloscope screenshot



Lab measurement - Pictures





Summary

- The allowed minimum PD current in the MARK state is reliably measurable.
- Two methods were presented using the existing different hardware architectures
- Proven with lab measurements also

End