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145.5.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively.

~~Data Link Layer classification of PSEs connected to a single-signature PD, shall provide the behavior in the state diagram defined in Figure 145–39 and Figure 145–40. Data Link Layer classification of PSEs connected to a dual-signature PD, shall provide the behavior in the state diagram defined in Figure 145–43.~~

Data Link Layer classification of PSEs shall provide the behavior in the state diagrams defined in Figure 145–39, Figure 145–40, and Figure 145–43.

Single-signature PD Data Link Layer classification shall provide the behavior of the state diagram defined in Figure 145–41, ~~and~~ Figure 145–42, and Figure 145–44. Dual-signature PD Data Link Layer classification shall provide the behavior of the state diagram defined in Figure 145–41 and Figure 145–44.

Execute the following renames per the Table as follows:

From:	To:
145.5.3.2 Attribute to state diagram variable mapping (single-signature)	145.5.3.2 Attribute to state diagram variable mapping (single-mode DLL)
Table 145–39—Attribute to state diagram variable cross-reference for single-signature operation	Table 145–39—Attribute to state diagram variable cross-reference for single-mode DLL operation
145.5.3.3 PSE power control state diagrams (single-signature)	145.5.3.3 PSE power control state diagrams (single-mode DLL)
Figure 145–39—PSE power control state diagram for single-signature PDs	Figure 145–39—PSE power control state diagram for single-signature PDs
145.5.3.4 Single-mode DLL PD power control state diagrams	145.5.3.4 Single-signature PD power control state diagrams
Figure 145–41—Single-signature PD power control state diagram	Figure 145–41—Single-mode DLL PD power control state diagram
145.5.3.5 Attribute to state diagram variable mapping (dual-signature)	145.5.3.5 Attribute to state diagram variable mapping (dual-mode DLL)
Table 145–40—Attribute to state diagram variable cross-reference for dual-signature operation	Table 145–40—Attribute to state diagram variable cross-reference for dual-mode DLL operation
145.5.3.6 PSE power control state diagrams (dual-signature)	145.5.3.6 PSE power control state diagrams (dual-mode DLL)
Figure 145–43—PSE power control state diagram for dual-signature PDs	Figure 145–43—PSE power control state diagram for dual-mode DLL
145.5.3.7 Dual-signature PD power control state diagrams	145.5.3.7 Dual-mode DLL PD power control state diagrams
Figure 145–44—Dual-signature PD power control state diagram	Figure 145–44—Dual-mode DLL PD power control state diagram
145.5.4 State change procedure across a link (single-signature)	145.5.4 State change procedure across a link (single-mode DLL)
145.5.4.1 PSE state change procedure across a link (single-signature)	145.5.4.1 PSE state change procedure across a link (single-mode DLL)
145.5.4.2 PD state change procedure across a link (single-signature)	145.5.4.2 PD state change procedure across a link (single-mode DLL)
145.5.5 State change procedure across a link (dual-signature)	145.5.5 State change procedure across a link (dual-mode DLL)
145.5.5.1 PSE state change procedure across a link (dual-signature)	145.5.5.1 PSE state change procedure across a link (dual-mode DLL)
145.5.5.2 PD state change procedure across a link (dual-signature)	145.5.5.2 PD state change procedure across a link (dual-mode DLL)

Insert new subclause 145.5.3a before 145.5.4 as follows:

145.5.3a Power requests and allocations

The variables PDRequestedPowerValue and PDRequestedPowerValue_mode(X) allow a PD to request an amount of power from the PSE. The variables PSEAllocatedPowerValue and PSEAllocatedPowerValue_alt(X) allow the PSE to allocate an amount of power to the PD.

PSEs shall use values in the range defined in Table 145–41 for PSEAllocatedPowerValue and PSEAllocatedPower-Value_alt(X) where X can be A or B. PDs shall use the values in the range defined in Table 145–42 for PDRequested-PowerValue and PDRequestedPowerValue_mode(X) where X can be A or B.

Table 145–41 — Permitted values for PSEAllocatedPowerValue and PSEAllocatedPowerValue_alt(X)

Powering mode	PD configuration	PSEAllocatedPowerValue	PSEAllocatedPowerValue_alt(X)
2-pair	—	$1 - 255^a$	0
4-pair	single-signature	$1 - 999$	0
	dual-signature	0	$1 - 499$

[a] NOTE—A PSE that has encountered a fault that requires to operate in 2-pair mode, may use values 1–499 for this variable.

Table 145–42 — Permitted values for PDRequestedPowerValue and PDRequestedPowerValue_mode(X)

Powering mode	PD configuration	PDRequestedPowerValue	PDRequestedPowerValue_mode(X)
—	single-signature	$1 - 999$	0
2-pair	dual-signature	$1 - 255^a$	$1 - 499$
4-pair		0	$1 - 499$

[a] NOTE—A PSE that has encountered a fault that requires to operate in 2-pair mode, may use values 1–499 for this variable.

145.5.3.3 PSE power control state diagrams (single-signature)

~~This subclause contains the variables and state diagrams the PSE uses when connected to a single-signature PD, or when it is providing power over 2 pairs.~~

This state diagram controls the PSEAllocatedPowerValue variable, which is used to allocate power to a PD. It is applicable when the PD is a single-signature PD, or when the PD is supplied in 2-pair mode.

145.5.3.4 Single-signature PD power control state diagram

Add the following text to this empty subclause:

This state diagram controls the PDRequestedPowerValue variable, which is used to request power from a PSE. It is applicable when the PD is a single-signature PD, or when the PD is supplied in 2-pair mode.

145.5.3.6 PSE power control state diagrams (dual-signature)

Add the following text to this empty subclause:

This state diagram controls the PSEAllocatedPowerValue_alt(X) variables, which are used to allocate power to the individual Modes of a dual-signature PD. It is applicable when the PD is a dual-signature PD that is supplied in 4-pair mode.

145.5.3.7 Dual-signature PD power control state diagrams

Add the following text to this empty subclause:

This state diagram controls the PDRequestedPowerValue_mode(X) variables, which are used to allocate power to the individual Modes of a dual-signature PD. It is applicable when the PD is a dual-signature PD that is supplied in 4-pair mode.

145.5.3.6.3 State diagrams

$(!pse\_dll\_enable\_alt(X) + !pse\_dll\_ready\_alt(X)) * (sig\_type = dual)$

$(!pse\_dll\_enable + !pse\_dll\_ready) * (sig\_type=dual)$

IDLE

$PSEAllocatedPowerValue\_alt(X) \Leftarrow 0$
$PDRequestedPowerValueEcho\_alt(X) \Leftarrow 0$
$TempVar\_alt(X) \Leftarrow 0$

$pse\_dll\_ready\_alt(X)$

pse_dll_ready

INITIALIZE

$PSEAllocatedPowerValue\_alt(X) \Leftarrow PSE\_INITIAL\_VALUE\_alt(X)$
$PDRequestedPowerValueEcho\_alt(X) \Leftarrow PSE\_INITIAL\_VALUE\_alt(X)$
$TempVar\_alt(X) \Leftarrow PSE\_INITIAL\_VALUE\_alt(X)$

UCT

RUNNING

$!local\_system\_change\_alt(X) *$
$(MirroredPDRequestedPowerValue\_alt(X) \neq$
$TempVar\_alt(X)) *$
$(PSEAllocatedPowerValue\_alt(X) =$
$MirroredPSEAllocatedPowerValueEcho\_alt(X))$

$local\_system\_change\_alt(X)$

PD_POWER_REQUEST

$TempVar\_alt(X) \Leftarrow$
$MirroredPDRequestedPowerValue\_alt(X)$
$pse\_power\_review\_alt(X)$

PSE_POWER_REVIEW

$pse\_power\_review\_alt(X)$
$local\_system\_change\_alt(X) \Leftarrow FALSE$

$(PSE\_NEW\_VALUE\_alt(X) <$
$PSEAllocatedPowerValue\_alt(X)) +$
$(PSEAllocatedPowerValue\_alt(X) =$
$MirroredPSEAllocatedPowerValueEcho\_alt(X))$

UCT

MIRROR_UPDATE

$PSEAllocatedPowerValue\_alt(X) \Leftarrow$
$PSE\_NEW\_VALUE\_alt(X)$
$PDRequestedPowerValueEcho\_alt(X) \Leftarrow TempVar\_alt(X)$
IF X = alt_pri THEN
   $pse\_power\_update\_pri \Leftarrow TRUE$
ELSE
   $pse\_power\_update\_sec \Leftarrow TRUE$
END

UCT

$(PSE\_NEW\_VALUE\_alt(X) \geq$
$PSEAllocatedPowerValue\_alt(X)) *$
$(PSEAllocatedPowerValue\_alt(X) \neq$
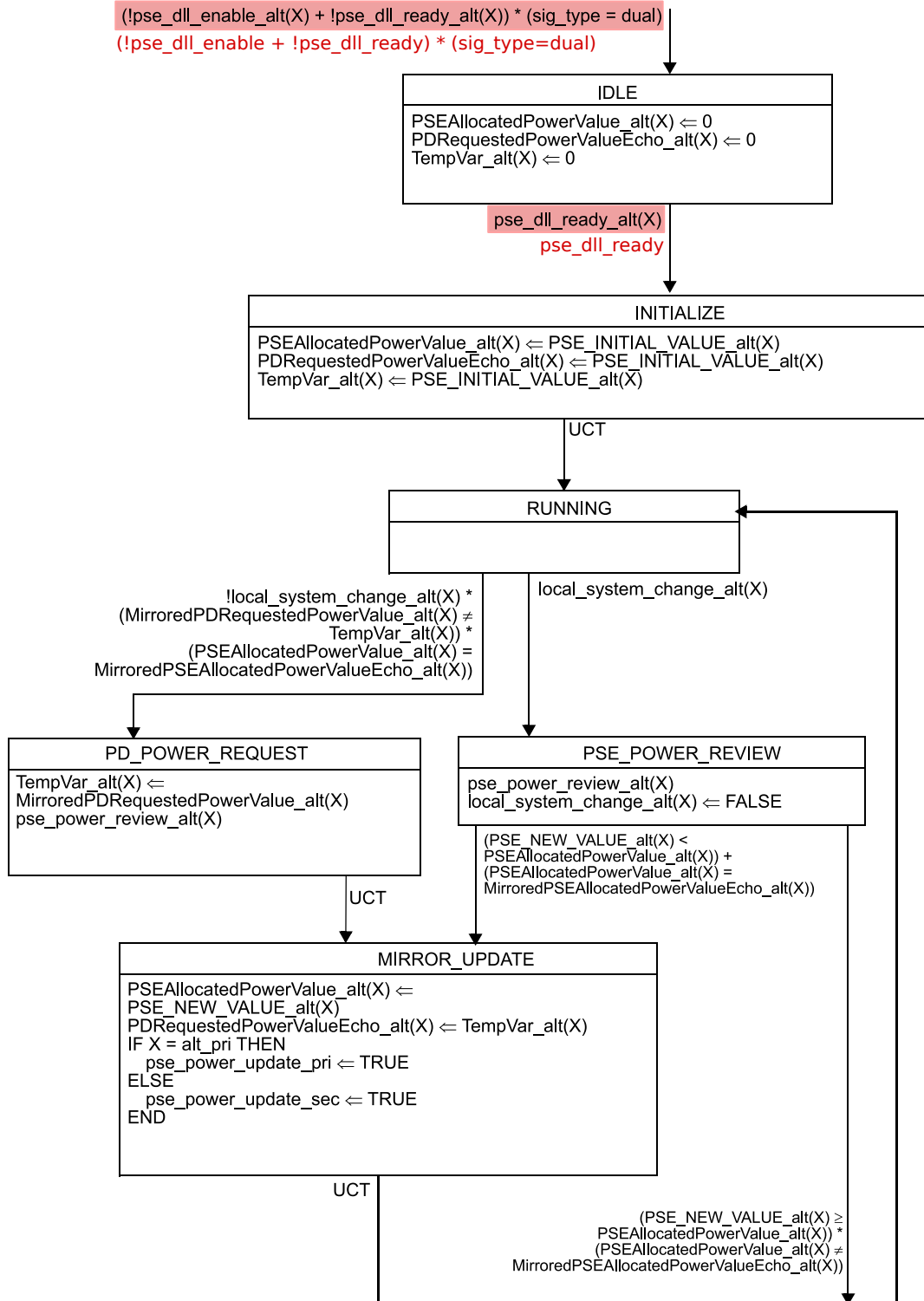$MirroredPSEAllocatedPowerValueEcho\_alt(X))$

Figure 145–43 — PSE power control state diagram for dual-signature PDs

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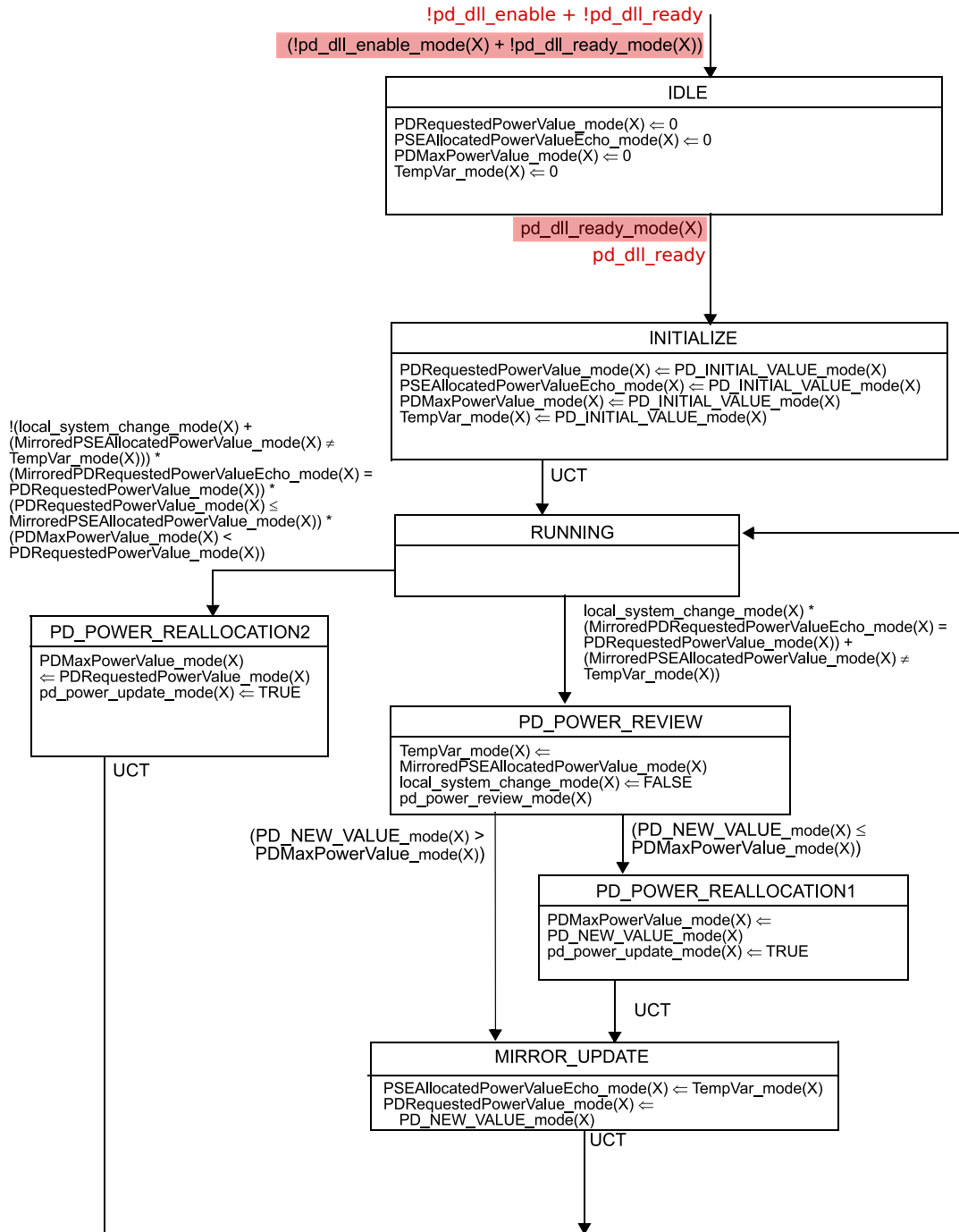### 145.5.3.7.4 State diagrams

Figure 145–44 — Dual-signature PD power control state diagram

145.5.5 State change procedure across a link (dual-signature)

Add new subclause under 145.5.5 as follows:

145.5.5.1a Transitions between 2-pair and 4-pair mode (dual-signature)

When a PSE, connected to a dual-signature PD, transitions from 4-pair to 2-pair operation, it shall assign the value of PSEAllocatedPowerValue_alt(X), where X is the powered Alternative, to PSEAllocatedPowerValue. The purpose of this is that the PD can continue operating over the remaining powered Mode.

When a PSE, connected to a dual-signature PD, transitions from 2-pair to 4-pair operation, it shall assign the value of PSEAllocatedPowerValue to PSEAllocatedPowerValue_alt(X), where X is the Alternative that was initially powered.

A dual-signature PD that is switched from 4-pair to 2-pair mode requests the amount of power it needs for 2-pair operation in the PDRequestedPowerValue variable. Per Table 145–42 this is the requested power for the active Mode.

79.3.2 Power via MDI TLV

…

The Power via MDI TLV shown in Figure 79–3 was originally defined in IEEE Std 802.1AB-2005 Annex G.3. This original TLV only supported the first three fields of Figure 79–3, labeled basic fields, enabling discovery and advertisement of Power via MDI capabilities. The Power via MDI TLV was revised by IEEE Std 802.3at-2009 to add a further three fields, labeled DLL classification extension, to provide Data Link Layer (DLL) classification capabilities. The Power via MDI TLV was revised again by IEEE Std 802.3bt-201x to add a further nine fields, labeled Type 3 and Type 4 extension to support additional capabilities offered by Type 3 and Type 4 PSEs and PDs.

~~Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension.~~

…

Append the following paragraph as follows:

If a Type 1 or Type 2 power entity implements Data Link Layer classification, it shall support the Power Via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered. If a Type 3 or Type 4 power entity implements Data Link Layer classification, it shall support both the DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Type 1 and Type 2 devices shall not include the Type 3 and Type 4 extension fields in transmitted LLDPDU's.

79.3.2.4.1 Power type

Move the PD 4PID bit from Table 79–6d (System setup field) to bit position 2 in Table 79-4 (Power type/source/priority field) as follows:

Table 79–6d—System setup field

Bit	Function	Value/meaning
7:6	Reserved	Transmit as zero. Ignore on receive.
5:2	Power typex	5 4 3 2 1 1 1 1 = Type 4 dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Type 3 dual-signature PD 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Type 4 single-signature PD 1 0 0 0 = Type 4 PSE 0 1 1 1 = Type 3 single-signature PD 0 1 1 0 = Type 3 PSE 0 1 0 1 = Type 2 PD 0 1 0 0 = Type 2 PSE 0 0 1 1 = Type 1 PD 0 0 1 0 = Type 1 PSE 0 0 0 1 = Reserved/Ignore 0 0 0 0 = Reserved/Ignore
1	PD 4PID	1 = PD supports powering of both Modes simultaneously 0 = PD does not support powering of both Modes simultaneously
0	PD Load	1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated. 0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.

Move PD 4PID

Table 79–4—Power type/source/priority field

Bit	Function	Value/meaning
7:6	power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	power source	Where power type = PD 5 4 1 1 = PSE and local 1 0 = Reserved 0 1 = PSE 0 0 = Unknown Where power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3:2	Reserved	Transmit as zero, ignore on receive
1:0	power priority	1 0 1 1 = low priority PD 1 0 = high priority PD 0 1 = critical priority PD 0 0 = priority unknown (default)

Move 4PID to bit 2

79.3.2.5 PD requested power value

Replace content above the dashed line with content below the dashed line as follows:

The PD requested power value field shall contain the PDs requested power value defined in Table 79–5, for Type 1, Type 2, and single-signature Type 3 and Type 4 PDs. The fields for PD requested power value shall be set to the sum of PD requested power value Mode A and PD requested power value Mode B in Table 79–6a, for Type 3 and Type 4 dual-signature PDs.

- -

The PD requested power value field shall contain the PDs requested power value defined in Table 79–5.

Change Table 79–5 as follows:

Table 79–5 — PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through ~~255~~ 999.

79.3.2.6 PSE allocated power value

Replace content above the dashed line with content below the dashed line as follows:

The PSE allocated power value field shall contain the PSE's allocated power value defined in Table 79–6 for PSEs connected to single-signature PDs and Type 1 and Type 2 PDs.

The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field, as defined in Table 79–6a, shall be provided in the PSE allocated power value field for Type 3 and Type 4 PSEs connected to a dual-signature PD. The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field may be provided in the PSE allocated power value field for Type 1 and Type 2 PSEs when connected to a dual-signature PD.

- -

The PSE allocated power value field shall contain the PSEs allocated power value defined in Table 79–6.

Change Table 79–6 as follows:

Table 79–6 — PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through ~~255~~ 999.

79.3.2.6a Dual-signature PD requested power value Mode A and Mode B

The "Dual-signature PD requested power value Mode A and Mode B" fields shall contain the PD requested power value defined in Table 79–6a and Table 79–6aa for Mode A and for Mode B of a dual-signature PD.

If Mode (X) is non-active while the other mode is active, the inactive PD requested power value Mode (X) field value shall be set to 0.

Single-signature PDs shall set the PD requested power value Mode A and Mode B fields to 0.

"Dual-signature PD requested power value Mode A" and "Dual-signature PD requested power value Mode B" are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

Change Table 79–6a as follows and create new Table 79–6aa:

Table 79–6a — Dual-signature PD requested power value field for Mode A

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal +0 through 499.

Table 79–6aa — Dual-signature PD requested power value field for Mode B

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal +0 through 499.

79.3.2.6b PSE allocated power value Alternative A and Alternative B

The "PSE allocated power value Alternative A field" and the "PSE allocated power value Alternative B" field shall contain the values in Table 79–6b and Table 79–6ba. for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.

Change Table 79–6b as follows and create new Table 79–6ba:

Table 79–6b — PSE allocated power value field for Alternative A

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal +0 through 499.

Table 79–6ba — PSE allocated power value field for Alternative B

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal +0 through 499.

Move the paragraph below (with changes) to above Table 79–6b in this subclause.

The "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives. "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" These fields are the power levels at the dual-signature PD PI. The PSE uses this value these values to compute $P_{Class\text{-}2P}$ as defined in 145.2.7. A PSE providing power to a Type 1, Type 2, or single-signature Type 3 or Type 4 PD, places 0 in the "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields defined in Table 79–6b.