1. Adding “single-signature whenever relevant.
2. Adding the missing text for dual-signature.

33.3.7.6 PD behavior during transients at the PSE PI

~~*Editor’s Note: 1. Type 3 and Type 4 to be added (to parts other than the newly added first paragraph).*~~

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.8.2. A single-signature PD shall include Cport as defined in Table 33–28. A dual-signature PD shall meet this requirement for each pairset.

PDs with power draw greater than Class 4 may require extra capacitance to maintain operation during PSE transients. Class 5 and 6 single-signature PDs will meet the requirement with Cport ≥ 10µF. Class 5 dual-signature PDs should include these Cport values at each pairset. Class 7 and 8 single-signature PDs will meet this requirement with Cport ≥ 20µF.

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI.
A Type 2 or single-signature Type 3 PD with peak power draw that does not exceed *P*Class_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI.
A dual-signature Type 3 and Type 4 PD with peak power draw that does not exceed *P*Class_PD-2P max and has an input capacitance of 180 µF or less per pairset requires no special considerations with regard to transients at the PD PI.

A single-signature Type 4 PD with peak power draw that does not exceed PClass PD max and has an input capacitance of 360µF or less requires no special considerations with regards to transients at the PD PI.-PDs that do not meet these requirements shall comply with the following:

~~a)~~ A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–34) after TLIM min (see Table 33–17 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33–1). The current limit meets Equation (33–30) and the voltage ramps from VPort_PSE min to VPort_PSE max at 2250 V/s.

A Type 2 or a single-signature Type 3 PD that demands less than Class 5 power levels shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–34) within 4 ms. During this test, the PD PI voltage is driven from VPort_PSE min to VPort_PSE min+2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond TLIM-2P min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance within 2.5% of RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM-2P per Equation (33–30). The current limit per pairset at the MDI (MDI ILIM-2P) is defined by Equation (33–30)~~:~~.

A dual-single-signature Type 3 PD that demands less than Class 5 power levels over a pairset shall meet both of the following over that pairset:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–35) within 4 ms. During this test, the PD PI voltage is driven from VPort_PSE-2P min to VPort_PSE-2P min+2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond TLIM-2P min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE-2P min to

56 V at 2250 V/s, the source impedance within 2.5% of RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM-2P per Equation (33–30). The current limit per pairset at the MDI (MDI ILIM-2P) is defined by Equation (33–30).

A single-signature Type 3 PD that demands Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template value (see Figure 33–34) within 4ms. During the test, the voltage of both PD modes is driven from VPort_PSE min to VPort_PSE min + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω and a source that supports a current greater than 5.0 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM-2P min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE min to 56 V at 2250 V/µs, the source impedance within 2.5% of RCh as defined in Table 33–1, and the voltage source limits the current to MDI ILIM-2P per Equation (33–30).

A dual-signature Type 3 PD that demands Class 5 power level over a pairset shall meet both of the following over that pairset:

a) The PD mode input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template value (see Figure 33–35) within 4ms. During the test, the voltage of both PD modes is driven from VPort_PSE-2P min to VPort_PSE-2P min + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω and a source that supports a current greater than 5.0 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM-2P min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE-2P min to 56 V at 2250 V/µs, the source impedance within 2.5% of RCh as defined in Table 33–1, and the voltage source limits the current to MDI ILIM-2P per Equation (33–30).

A single-signature Type 3 or Type 4 PD that demands more than Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 3.0 A and shall settle below the PD extended template value (see Figure 33–34) within 4 ms. During the test, the voltage of both PD modes is driven from VPort_PSE min to VPort_PSE min + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω and a source that supports a current greater than 5.0 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE min to 56 V at 2250 V/µs, the source impedance within 2.5% of RCh as defined in Table 33–1, and the voltage source limits the current to MDI ILIM-2P per Equation (33–30).

Equation 33-30 was moved to here in ordet not to break the flow of the use cases.

The current limit per pairset at the MDI (MDI ILIM-2P) is defined by Equation (33–30):

$$\{pse_{\text{ILIM-2P min}}\}_{\text{mA}} < \{mdi_{\text{ILIM-2P}}\}_{\text{mA}} \leq \{pse_{\text{ILIM-2P min}}\}_{\text{mA}} + 5_{\text{mA}} \qquad (33\text{–}30)$$

where

*pse*ILIM-2Pmin is the PSE ILIM-2P min as defined in Table 33–17
*mdi*ILIM-2P is the per pairset current limit at the MDI (MDI ILIM)

~~*Editor's Note: Type 4 DS PDs need to be considered for following text (as do lower class DS PDs).*~~