33.2.7.1 PSE Single-Event Physical Layer classification

When Single-Event Physical Layer classification is implemented by Type 1 and Type 2 PSEs, classification consists of the application of V_{Class} and the measurement of I_{Class} in a single classification event 1-EVENT_CLASS—as defined in the state diagram in Figure 33–13.

The PSE shall provide to the PI V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–15. Polarity shall be the same as defined for V_{Port_PSE} in 33.2.3 and timing specifications shall be as defined by T_{pdc} in Table 33–15.

The PSE shall measure the resultant I_{Class} and classify the PD based on the observed current specified in Table 33–14. All measurements of I_{Class} shall be taken after the minimum relevant class event timing in Table 33–15. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured I_{Class} is within the range of I_{Class_LIM}, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state.

33.2.7.2 PSE Multiple-Event Physical Layer classification

When Multiple-Event Physical Layer classification is implemented, classification consists of a series of classification and mark events as defined in the state diagram in Figure 33–13, Figure 33–19, Figure 33–20, and Figure 33–21.

Voltages, V_{Class}, V_{Mark}, and V_{Reset} are specified in Table 33–15. Currents I_{Class_LIM}, and I_{Mark_LIM} are specified in Table 33–15. PD classification signature measurements of I_{Class} are specified in Table 33–11, Table 33–12 and Table 33–14. Classification times, T_{pdc}, T_{LCE}, T_{CLE1}, T_{CLE2}, T_{CLE3}, T_{ME1}, T_{ME2}, and T_{Reset} are specified in Table 33–15. The referenced Autoclass time, T_{ACS} is specified in Table 33–27.

Type 2 PSEs shall provide a maximum of two class events and two mark events. Type 3 PSEs shall provide a maximum of four class events and four mark events for single-signature PDs and a maximum of 3 class events and three mark events on each pairset for dual-signature PDs unless a class reset event clears the class and mark event counts. Type 4 PSEs shall provide a maximum of five class events and five mark events for single-signature PDs and a maximum of four class events and four mark events on each pairset for dual-signature PDs unless a class reset event clears the class and mark event counts. Type 3 and Type 4 PSEs may issue a class reset event to perform mutual identification.

The timing specification for Type 1 and Type 2 PSEs in the state CLASS_EV1 shall be T_{CLE1}. The timing specification for Type 3 and Type 4 PSEs in the state CLASS_EV1_LCE_PRI, CLASS_EV1_LCE_SEC, CLASS_EV1_LCE_RESET_PRI, or CLASS_EV1_LCE_RESET_SEC shall be T_{LCE}.

The total timing specification for Type 3 and Type 4 PSEs in the states CLASS_EV1_LCE and CLASS_EV1_AUTO shall be T_{LCE}. The PSE in the state CLASS_EV1_AUTO shall measure I_{Class} within T_{pdc} to determine if the PD will perform Autoclass. If the Autoclass enabled Type 3 or Type 4 PSE in the state CLASS_EV1_LCE does not measure I_{Class} in the range of class signature 0 before T_{ACS} min and the PSE in the state CLASS_EV1_AUTO does measure I_{Class} in the range of class signature 0 after T_{ACS} max this indicates the PD will perform Autoclass. (See 33.3.5.3).

When the PSE is in the state CLASS_EV2, CLASS_EV2_PRI, or CLASS_EV2_SEC, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification.

When the PSE is in the state CLASS_EV3, CLASS_EV3_PRI, CLASS_EV3_SEC, CLASS_EV4, CLASS_EV4_PRI, CLASS_EV4_SEC, or CLASS_EV5 the PSE shall provide to the PI V_{Class}, subject to the T_{CLE3} timing specification.

In the states CLASS_EV1, CLASS_EV1_LCE, CLASS_EV1_LCE_PRI, CLASS_EV1_LCE_SEC, CLASS_EV2, CLASS_EV2_PRI, CLASS_EV2_SEC, CLASS_EV3, CLASS_EV3_PRI, CLASS_EV3_SEC, CLASS_EV4, CLASS_EV4_PRI, CLASS_EV4_SEC, CLASS_EV5, CLASS_EV1_LCE_RESET_PRI, and CLASS_EV1_LCE_RESET_SEC, the PSE shall measure I_{Class} within T_{pdc} and classify the PD based on the observed current.

When the PSE is in the state MARK_EV1, MARK_EV1_PRI, MARK_EV1_SEC, MARK_EV2_PRI, MARK_EV2_SEC, MARK_EV3, MARK_EV3_PRI, MARK_EV3_SEC, or MARK_EV4, the PSE shall provide to the PI V_{Mark}. The timing specification shall be as defined by T_{ME1}.

When the Type 3 or Type 4 PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark}. The timing specification shall be as defined by T_{ME1}.

When the Type 2 PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark}. The timing specification shall be as defined by T_{ME2}.

When the PSE is in the state MARK_EV_LAST, MARK_EV_LAST_PRI and MARK_EV_LAST_SEC, the PSE shall provide to the PI V_{Mark}. The timing specification shall be as defined by T_{ME2}.

The mark event states, MARK_EV1, MARK_EV1_PRI, MARK_EV1_SEC, MARK_EV2, MARK_EV2_PRI, MARK_EV2_SEC, MARK_EV3, MARK_EV3_PRI, MARK_EV3_SEC, MARK_EV4, MARK_EV_LAST, MARK_EV_LAST_PRI and MARK_EV_LAST_SEC commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–26.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min, a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state. The PSE shall limit class event currents to I_{Class_LIM} and shall limit mark event currents to I_{Mark_LIM}.

All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–15. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for $V_{Port\_PSE\text{-}2P}$ in 33.2.4. The PSE shall complete Multiple-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min, unless in the CLASS_RESET_PRI or CLASS_RESET_SEC states. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Class} for a period of at least T_{Reset} min before starting a new detection cycle.

If the result of the first class event is Class 4, a Type 2 PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete. If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 2 PSE treats the PD as a Type 1 PD and may

omit the subsequent mark and class events and classify the PD according to the result of the first class event.

When a PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE assigns the PD Class 3, 4, or 6, whichever is the highest that it can support.

Classification events may appear on one or both pairsets.

A Type 3 or Type 4 PSE connected to a dual-signature PD, implementing 4PID based on classification and enabled for only one class event, shall issue an initial three classification events to determine the Type of the connected PD, then transition to either the CLASS_RESET_PRI or CLASS_RESET_SEC.

When the PSE is in the state CLASS_RESET_PRI or CLASS_RESET_SEC the PSE shall provide to the PI V_{Reset}, subject to the T_{Reset} timing specification.