C_{Port} and $C_{Port\text{-}2P}$ baseline v122

Info (not part of baseline)

The current definition of "C_{Port} per pairset" is confusing since this capacitance behaves in a completely different way depending on the PD being a single- or dual-signature device. Also the effective total capacitance value of a dual-signature PD is twice that of a single-signature PD for the same value of "C_{Port} per pairset".
Proposal:
For single-signature PDs we use C_{Port}, which is the total capacitance of the PD.
For dual-signature we use $C_{Port\text{-}2P}$ which is the capacitance on a pairset.

33.3.7 PD power

Add a new item 13 after item 12 in Table 33–28 as follows:

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
12	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		3, 4	See 33.3.7.3, 33.3.7.6
13	Pairset capacitance during MDI_POWER states	$C_{Port\text{-}2P}$	µF	5.00		3, 4	See 33.3.7.3, 33.3.7.6

33.3.7.3 Input inrush current

Remove the following text (page 134, lines 21–30)

Input inrush currents at startup, I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$ are limited by the PSE if C_{Port} per pairset is less than 180 µF for:

- single-signature PDs, assigned to Class 0 to 6
- dual-signature PDs assigned to Class 1 to 5

and if C_{Port} per pairset is less than 360 µF for single-signature PDs assigned to Class 7 to 8, as specified in Table 33–17. If C_{Port} per pairset is larger, input inrush current shall be limited by the PD such that I_{Inrush_PD} max and $I_{Inrush\_PD\text{-}2P}$ max are satisfied.

Insert the following text in its place

Input inrush currents at startup, I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$, as defined in Table 33–17, are limited by the PSE if $C_{Port} < 180$ µF for single-signature PDs assigned to Class 0 to 6, and if $C_{Port} < 360$ µF for PDs assigned to Class 7 or 8. Input inrush current at startup, $I_{Inrush\_PD\text{-}2P}$, is limited by the PSE if $C_{Port\text{-}2P} < 180$ µF for dual-signature PDs. If a PD has a larger C_{Port} or $C_{Port\text{-}2P}$ value, then the PD shall limit the input inrush current such that I_{Inrush_PD} max and $I_{Inrush\_PD\text{-}2P}$ max, as defined in Table 33–17, are met.

C_{Port} in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE ~~encounters~~ sees as load when operating one or both pairsets, when connected to a single-signature PD. $C_{Port\text{-}2P}$ in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. ~~When a PSE is connected to a dual-signature PD, C_{Port} value requirements are specified in 33.3.7.6.~~ See Figure 33–33 for a simplified PSE-PD C_{Port} and $C_{Port\text{-}2P}$ interpretation model.

Replace Figure 33–33 as follows:

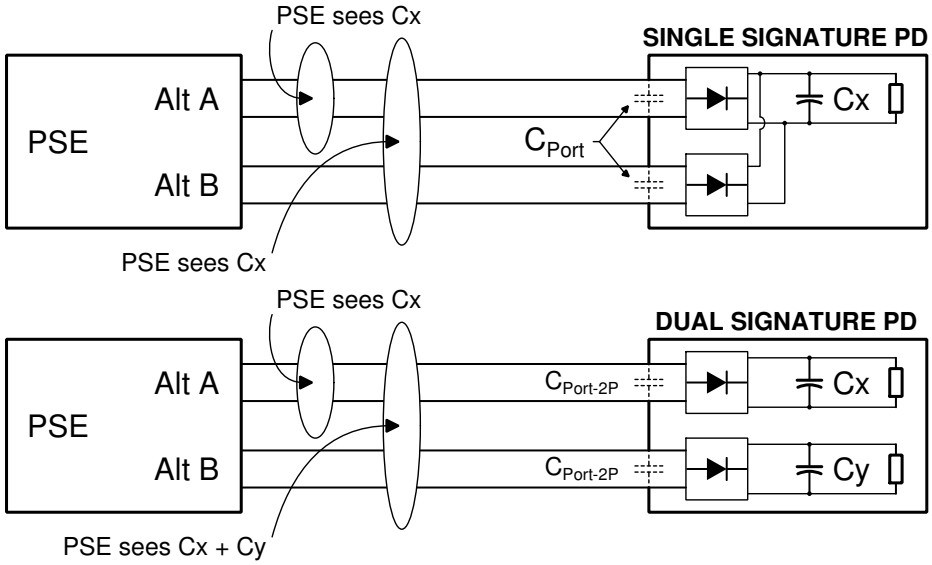

Figure 33–33 — C_{Port} and $C_{Port-2P}$ interpretation model

33.3.7.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.8.2. A single-signature PD shall include C_{Port} as defined in Table 33–28. A dual-signature PD shall ~~meet this requirement for~~ include $C_{Port-2P}$ as defined in Table 33–28 on each pairset.