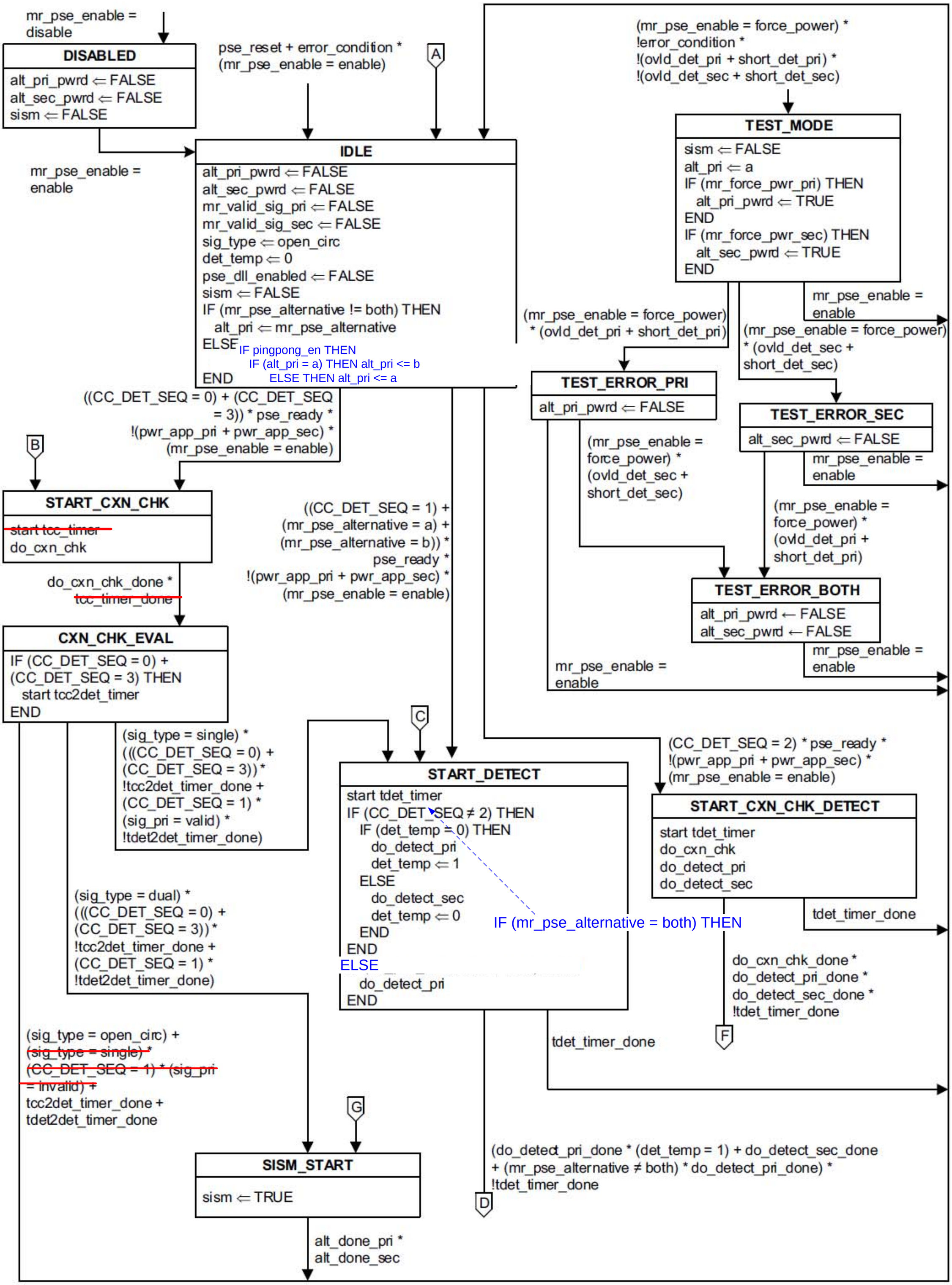


**Figure 33–15—Type 3 and Type 4 top level PSE state diagram**

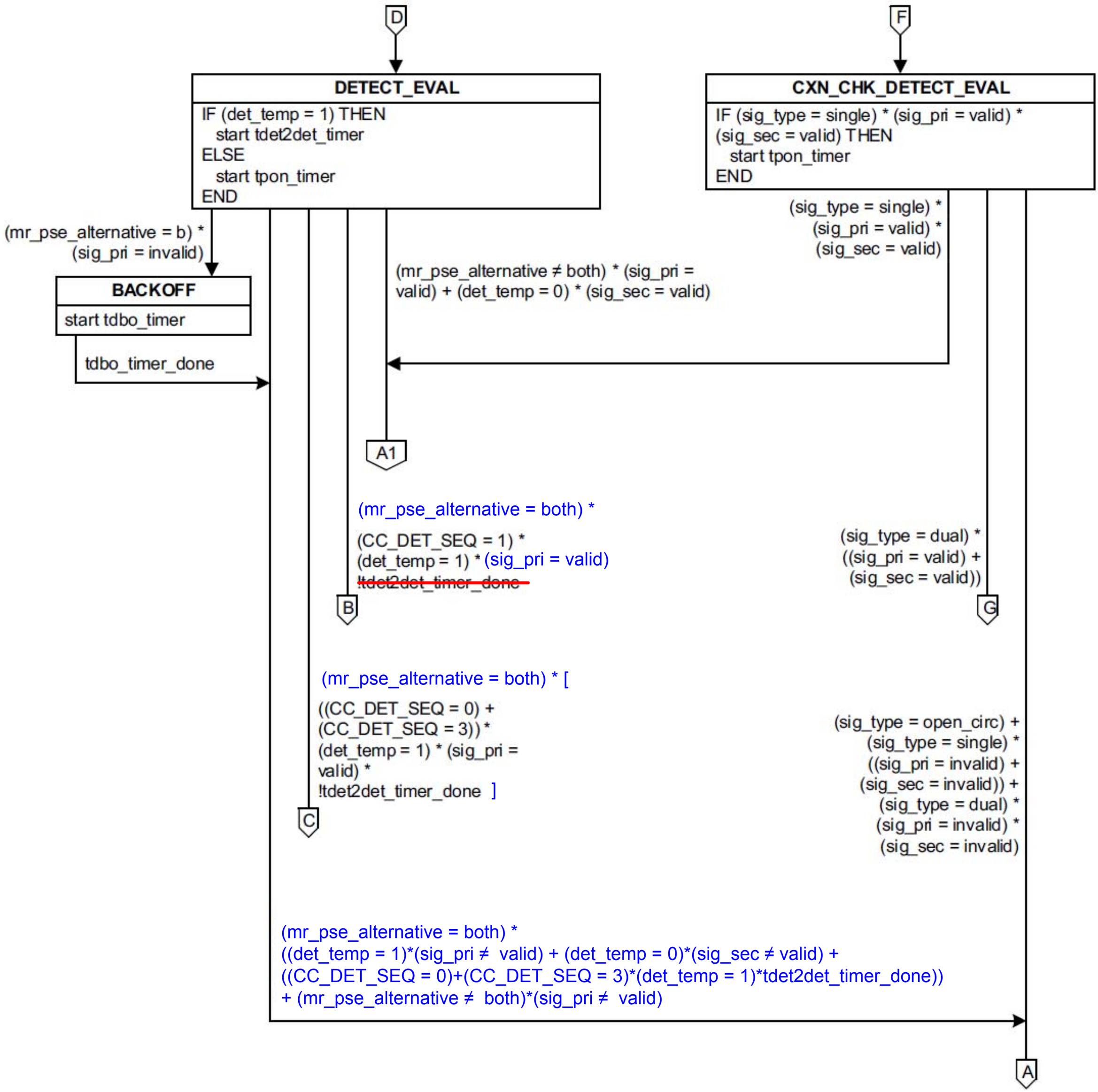


**Figure 33–15—Type 3 and Type 4 top level PSE state diagram (continued)**

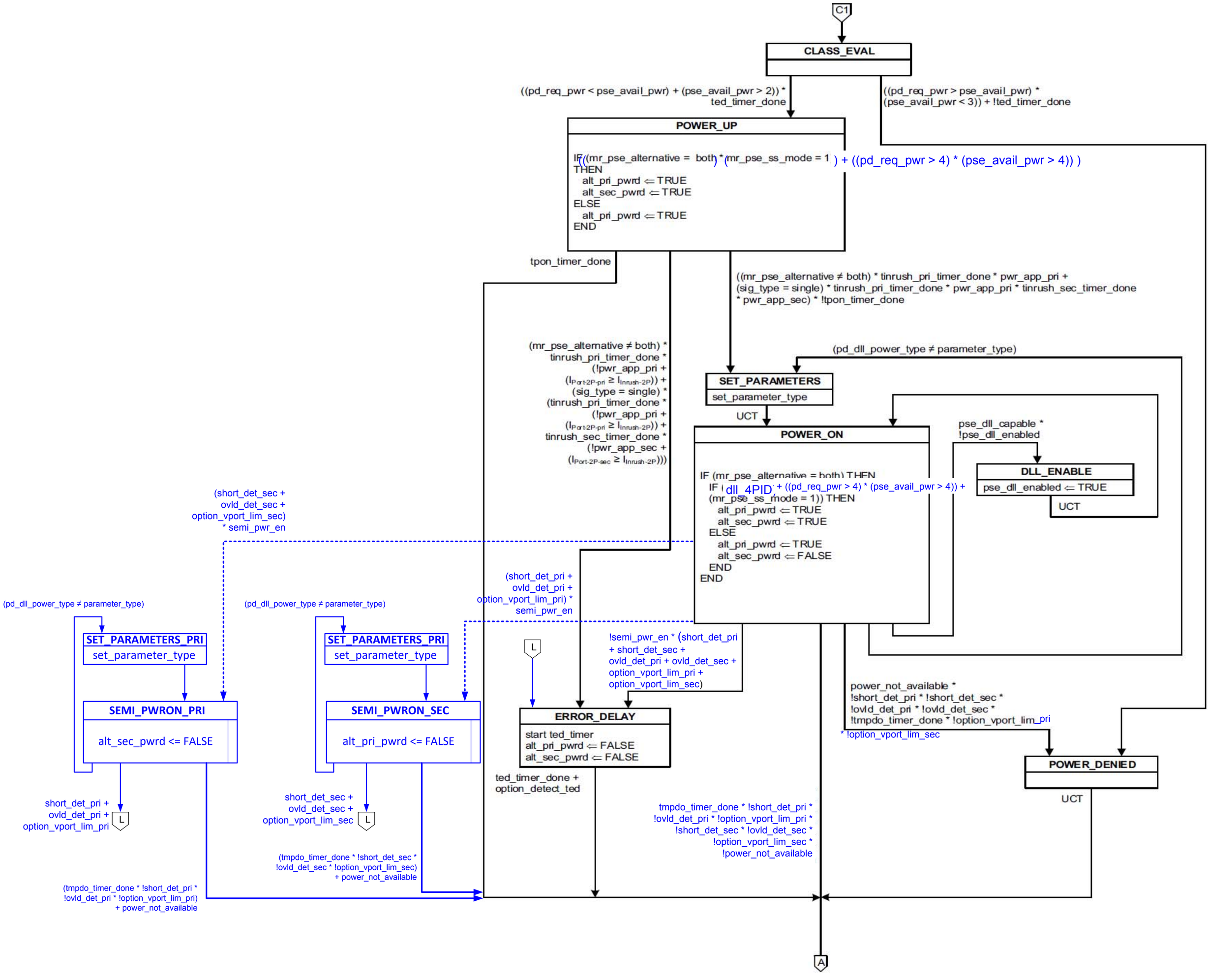


**Figure 33–15—Type 3 and Type 4 top level PSE state diagram (continued)**

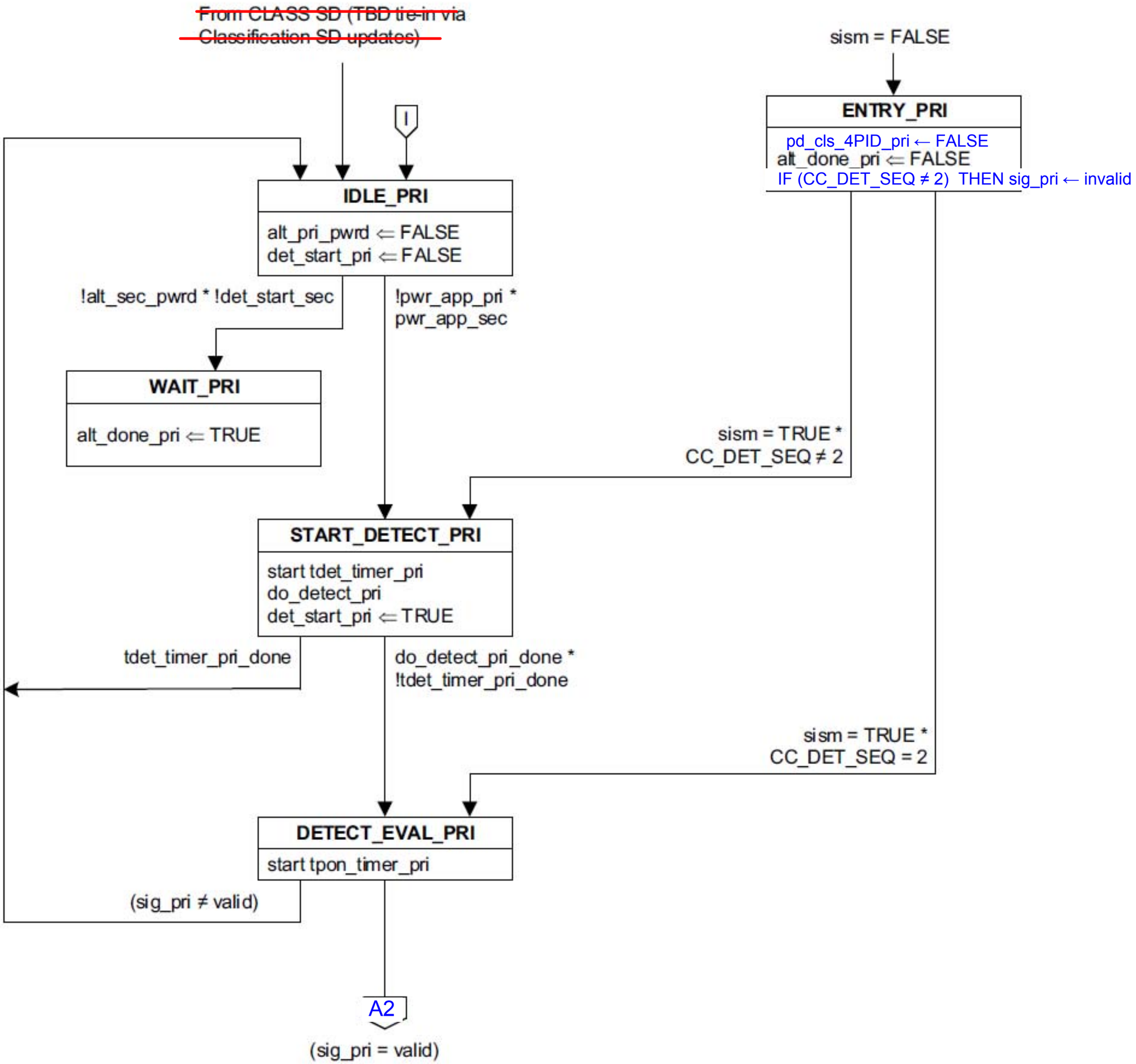


**Figure 33–16—Type 3 and Type 4 Primary Alternative dual-signature semi-independent PSE state diagram**

C2

From CLASS SD (TBD tie-in via Classification SD updates)

**CLASS_EVAL_PRI**

IF (pd_cls_4PID_pri * (sig_pri = valid) * (sig_sec = valid) + pwr_app_sec) THEN
  PD_4pair_cand_pri <= TRUE
ELSE
  PD_4pair_cand_pri <= FALSE
END

(pd_req_pwr_pri ≤ pse_avail_pwr_pri) * ted_timer_pri_done * (PD_4pair_cand + !alt_sec_pwrd + pwr_app_sec)

(pd_req_pwr_pri > pse_avail_pwr_pri) + (!PD_4pair_cand * alt_sec_pwrd) + !ted_timer_pri_done

**POWER_UP_PRI**

alt_pri_pwrd ⇐ TRUE
det_start_pri ⇐ FALSE

tpon_timer_pri_done

tinrush_timer_pri_done * pwr_app_pri * !tpon_timer_pri_done

(pd_dll_power_type ≠ parameter_type)

**SET_PARAMETERS**

set_parameter_type

UCT

tinrush_timer_pri_done * (!pwr_app_pri + ($I_{Port-2P_pri} \geq I_{Inrush-2P}$))

pse_dll_capable * !pse_dll_enabled

**POWER_ON_PRI**

**DLL_ENABLE**

pse_dll_enabled ⇐ TRUE

UCT

short_det_pri + ovld_det_pri + option_vport_lim

**ERROR_DELAY_PRI**

start ted_timer_pri
alt_pri_pwrd ⇐ FALSE

ted_timer_pri_done + option_detect_ted_pri

power_not_available_pri * !short_det_pri * !ovld_det_pri * !tmpdo_timer_pri_done * !option_vport_lim

**POWER_DENIED_PRI**

UCT

tmpdo_timer_pri_done * !short_det_pri * !ovld_det_pri * !power_not_available_pri * !option_vport_lim

I

**Figure 33–17—Type 3 and Type 4 Primary Alternative dual-signature semi-independent PSE state diagram (continued)**

PD_4pair_cand <= TRUE

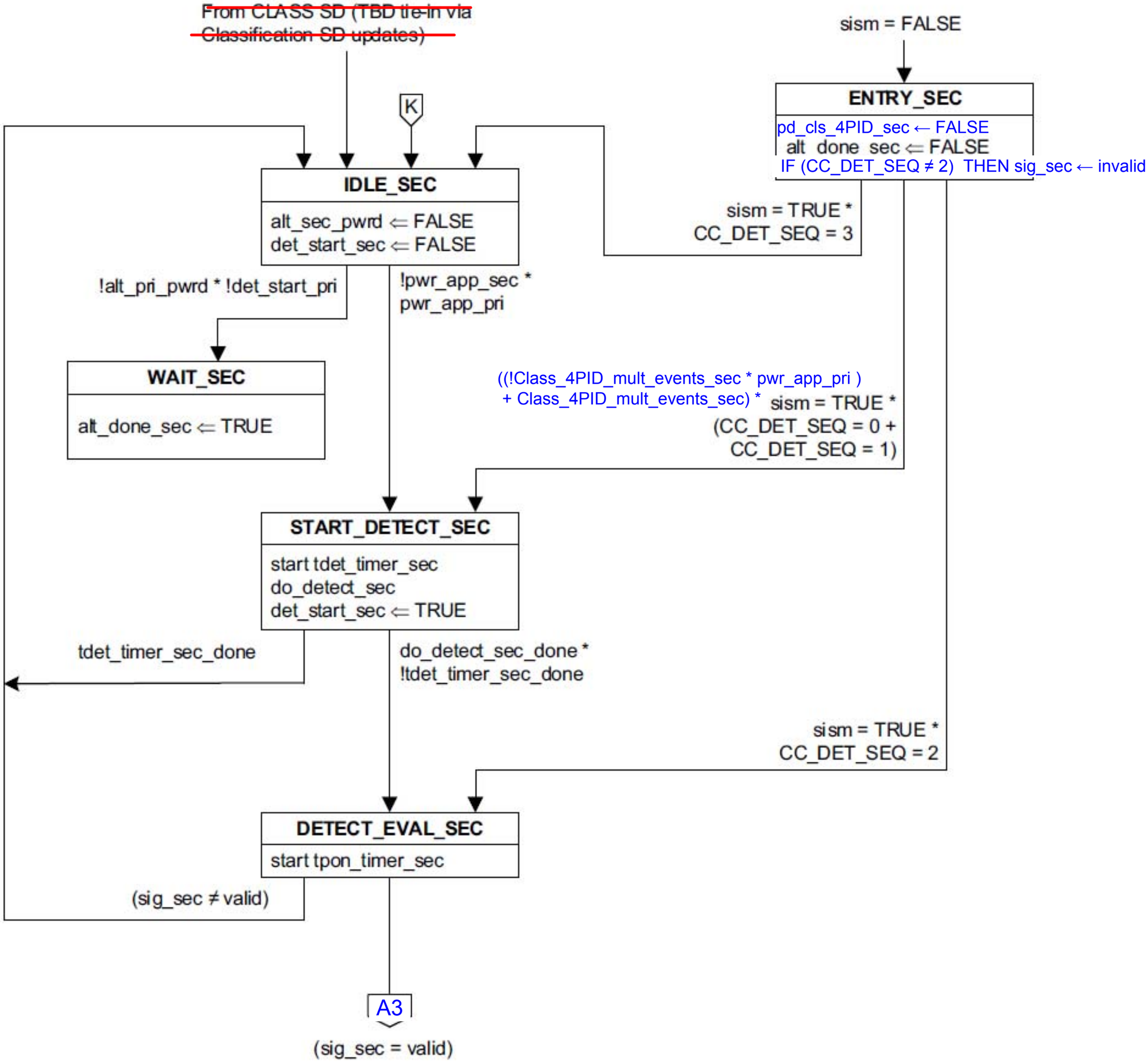


**Figure 33–18—Type 3 and Type 4 Secondary Alternative dual-signature semi-independent PSE state diagram**

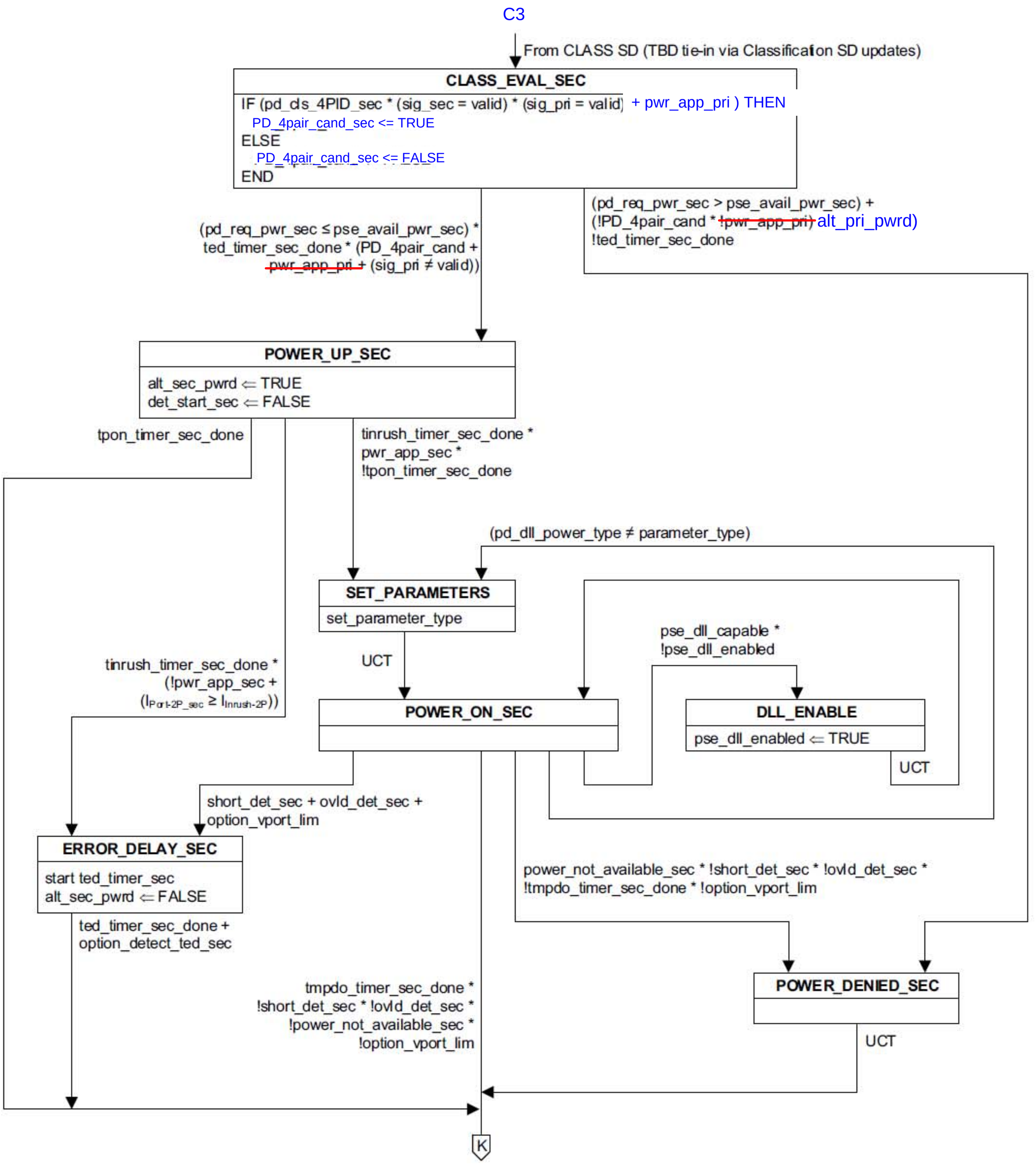


**Figure 33–18—Type 3 and Type 4 Secondary Alternative dual-signature semi-independent PSE state diagram (continued)**

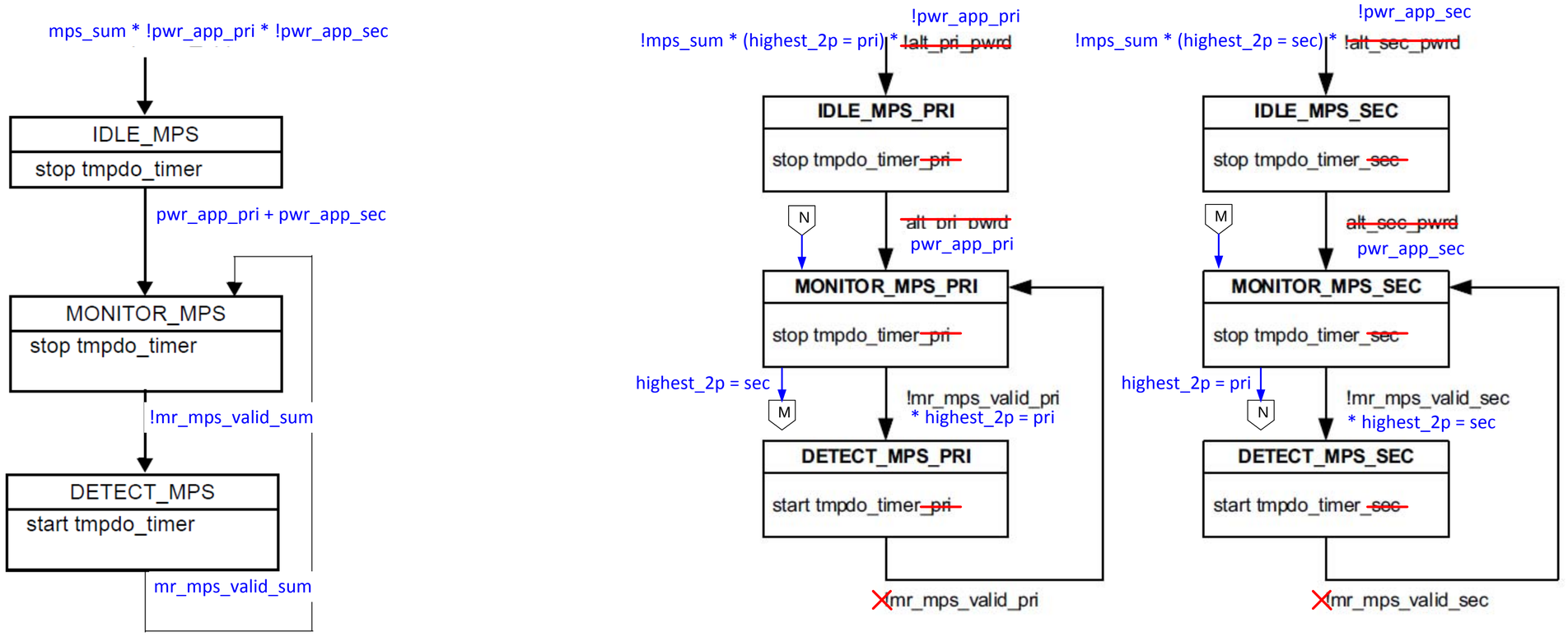


**Figure 33–22—Type 3 and Type 4 PSE MPS monitor state diagram**
for SS PD

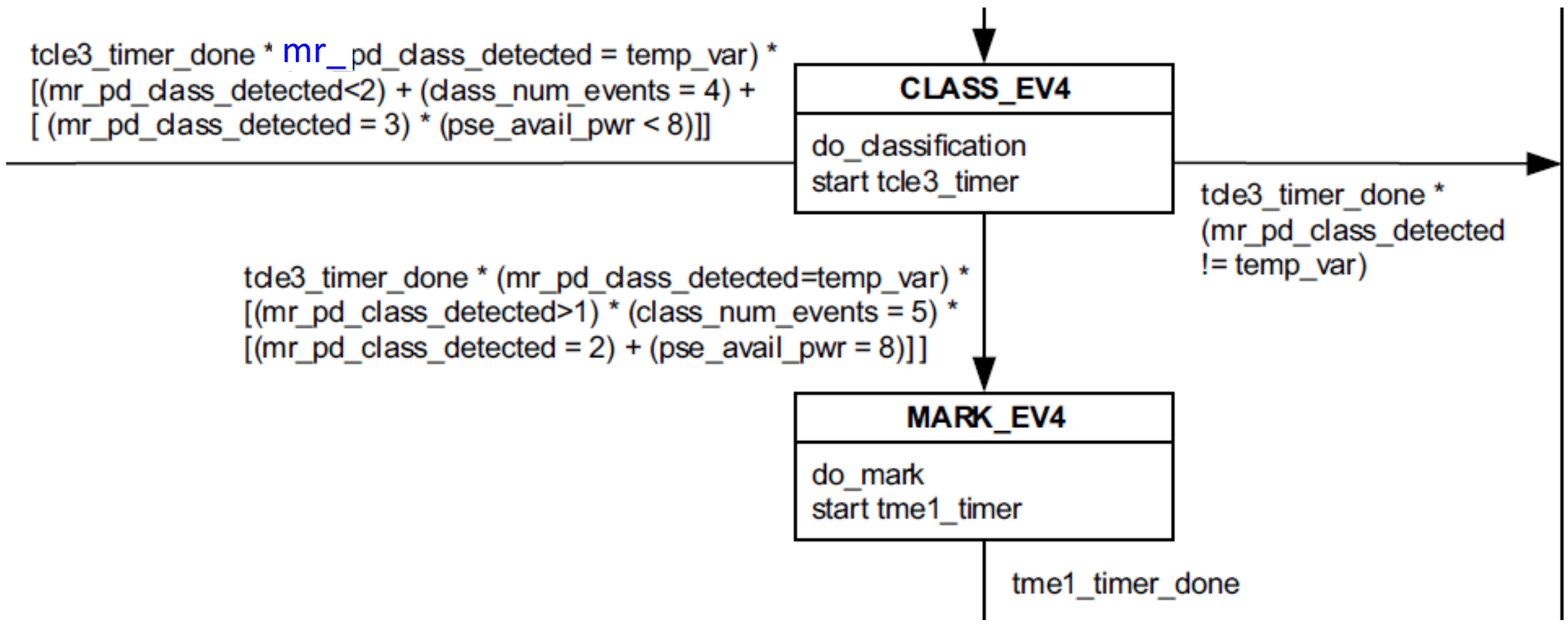


**Figure 33–19—Type 3 and Type 4 PSE single-signature classification state diagram**

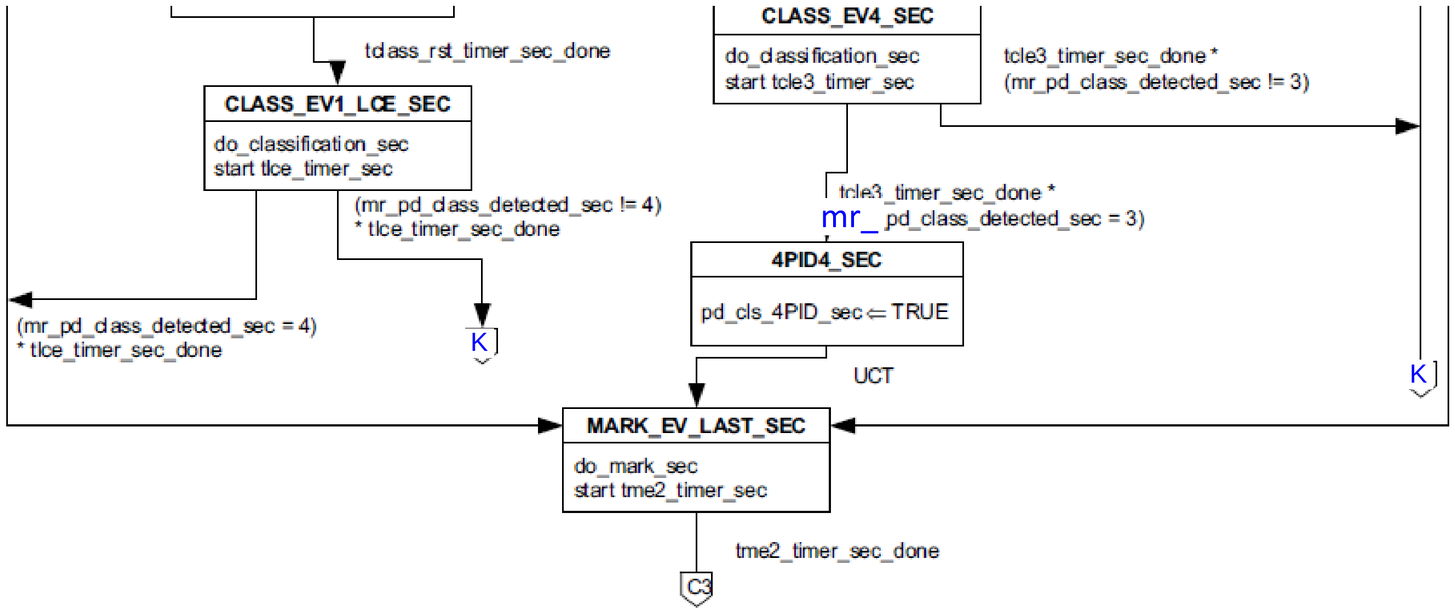


**Figure 33–20—Type 3 and Type 4 PSE dual-signature classification state diagram on the Primary Alternative**

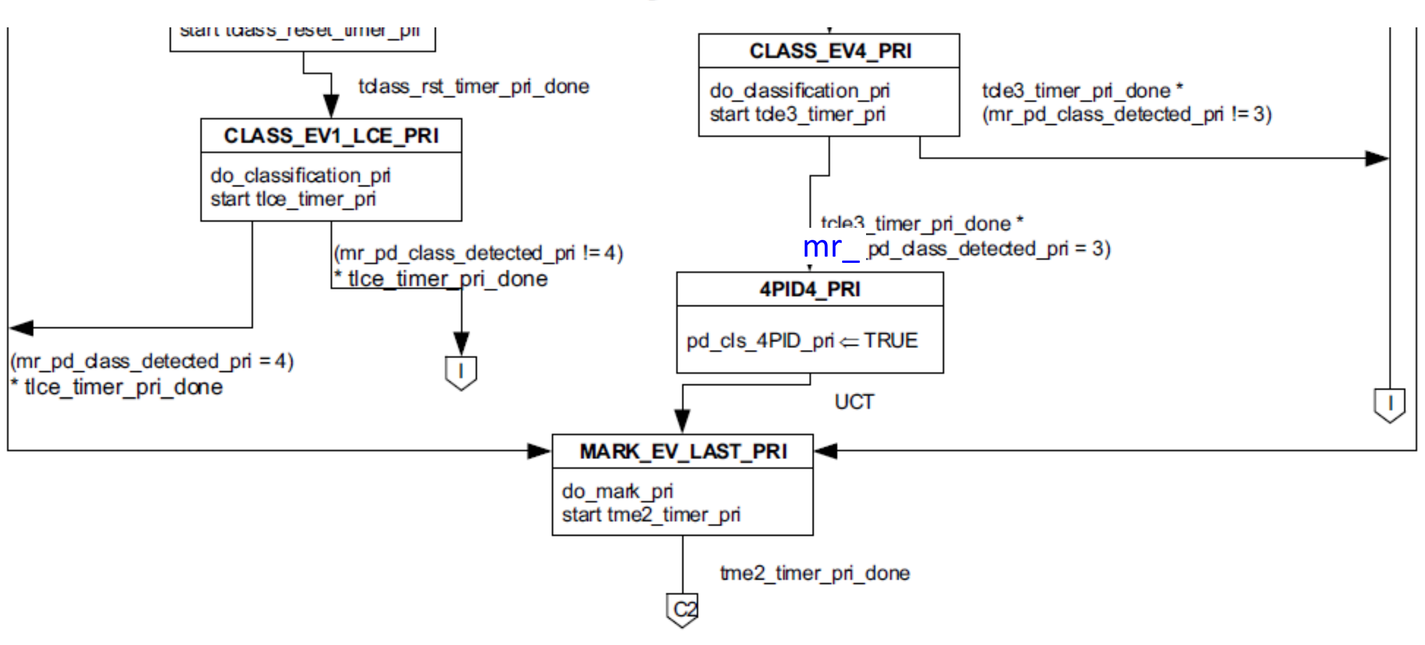


**Figure 33–21—Type 3 and Type 4 PSE dual-signature classification state diagram on the Primary Alternative**

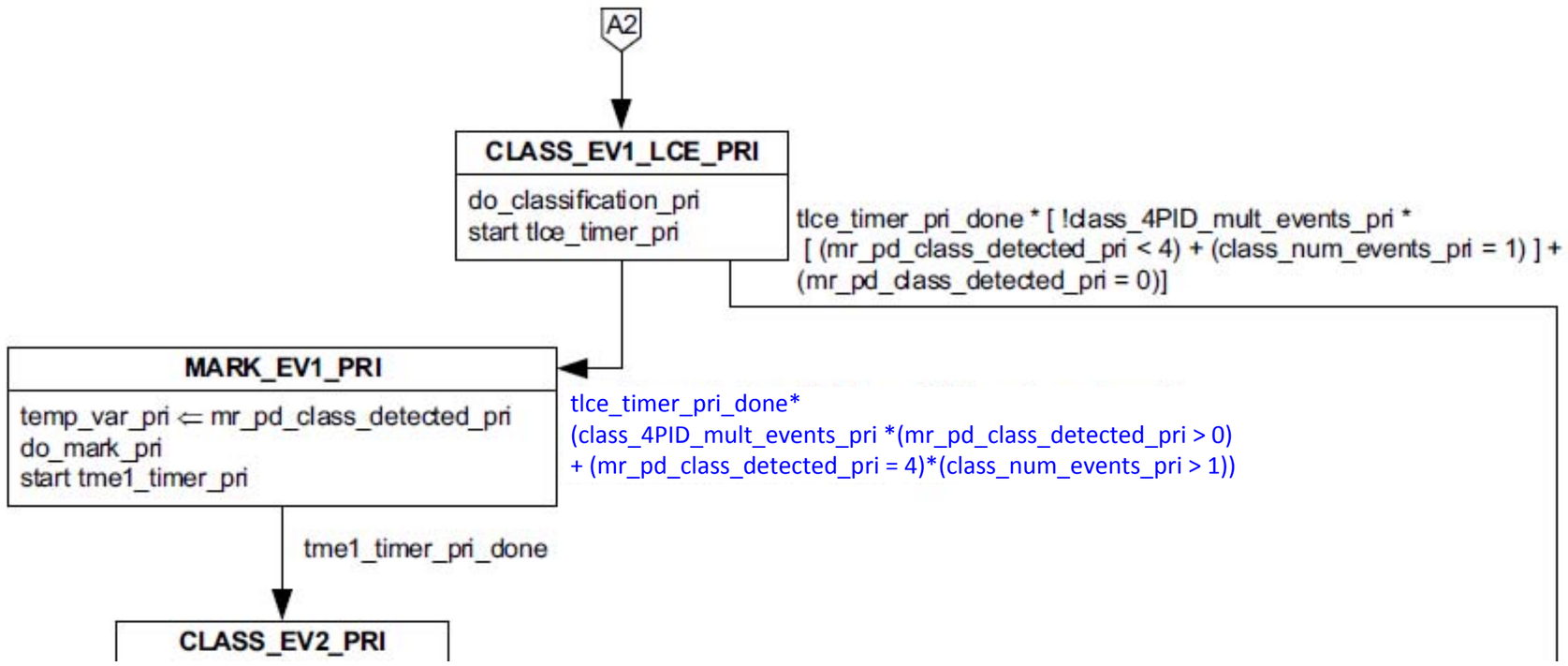


**Figure 33–21—Type 3 and Type 4 PSE dual-signature classification state diagram on the Primary Alternative**

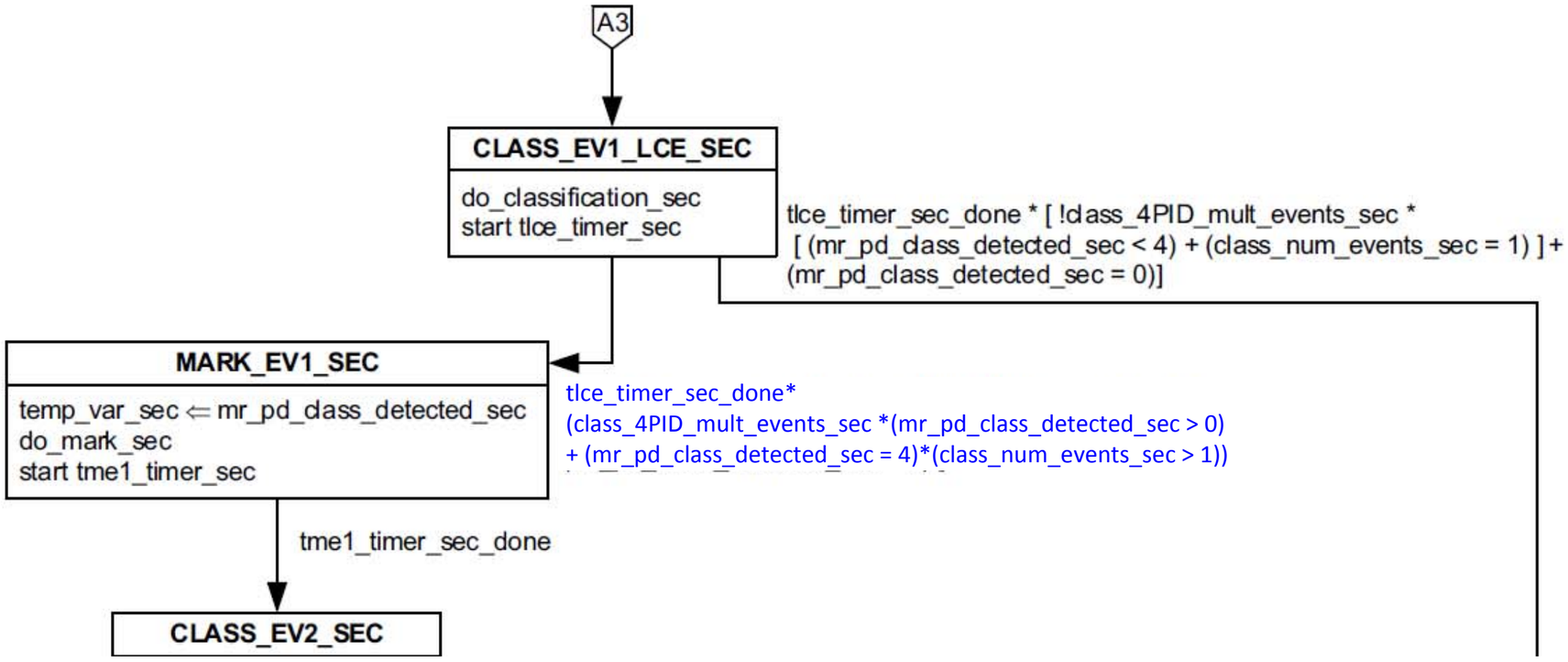


**Figure 33–20—Type 3 and Type 4 PSE dual-signature classification state diagram on the Primary Alternative**