Comments about Transients at PD PI lasting less than 30us and baseline text

Comment #1

The following text needs some improvement to ensure proper specification of the voltage transients (page 105)

33.2.8.2 Voltage transients

A Type 2, Type 3, and Type 4 PSE shall maintain an output voltage no less than K_{Tran_lo} below $V_{Port\_PSE\text{-}2P}$ min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 33.2.8.7.

Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance allows a Type 1 or Type 2 PD to operate for any input voltage transient lasting less than 30 µs. Transients lasting more than 250 µs shall meet the $V_{Port\_PSE\text{-}2P}$ specification.

At line 7 replace :

The minimum PD input capacitance allows a Type 1 or Type 2 PD to operate for any input voltage transient lasting less than 30 µs.

With :

The minimum PD input capacitance C_{port} min or $C_{port\text{-}2P}$ min defined in Table 33-28, allows PDs of any Type to operate for input voltage transients which cause V_{PD} to drop as low as 0V lasting less than 30 µs as specified in 33.3.7.6

Remedy explanation:

This improvement is necessary even if there is not a “shall” here, because it is referenced as normative in the PD section (33.3.7.6).

1. The name of the PD input capacitance is Cport or Cport-2P as defined in Table 33-28
2. It is necessary to extend the text to all PD Types, single and dual Signature.
3. The voltage transients specified in this paragraph are meant to cause the PD voltage to drop, and the maximum drop is 100%, i.e. 0V
4. A reference to the PD normative text is useful (see below next comment)

33.2.8.2 Voltage transients

Modify the second paragraph as follows:

Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance C_{Port} min or $C_{Port\text{-}2P}$ min defined in Table 33-28, allows PDs of any Type to operate for input voltage transients which cause V_{PD} to drop as low as 0V lasting less than 30µs as specified in 33.3.7.6

Comment #2

33.3.7.6 PD behavior during transients at the PSE PI

Editor's Note: 1. Type 3 and Type 4 to be added (to parts other than the newly added first paragraph).

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.8.2. A single-signature PD shall include C_{port} as defined in Table 33–28. A dual-signature PD shall meet this requirement for each pairset.

In order to allow PD with Classes 5 to 8 to operate without interruption during a 30us input transient, a larger minimum Cport is necessary:

Table 33-28 Item 12 Cport
Split in 3 rows, one for all Types Classes 0-4, for and two for Types 3 and 4 addressing classes 5-6 and 7-8.

Remedy explanation:
Since the max current for Types 3 may be as high as 2x Icable, a double minimum capacitance is recommended to allow the PD voltage to stay above VOFF_PD (30V) with the same margin taken for Types 1 and 2 ➔ 10uF for Type3
Type4 PD max current is even higher than that, so 20uF is recommended

33.3.7 PD power

Modify item 12 in Table 33–28 as follows:

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
12	PI capacitance during MDI_POWER states, Single Signature Class 0 to 4	C_{Port}	uF	5.00		all	See 33.3.7.6, 33.3.7.3
	PI capacitance during MDI_POWER states Single Signature Class 5, 6			10.0		3,4	
	PI capacitance during MDI_POWER states Single Signature Class 7, 8			20.0		4	
13	Pairset capacitance during MDI_POWER states Dual Signature Class 0 to 4	$C_{Port-2P}$	uF	5.00		3,4	See 33.3.7.6, 33.3.7.3
	Pairset capacitance during MDI_POWER states Dual Signature Class 5			10.00		4	

and delete lines 18-21 – page 138

Appendix:
Example calculation for Class8 PD shows that a 5uF capacitance is not enough to guarantee the operation during a 30us transient.

For Type4 Class8 $$C_{Port}min = \frac{M*I_{LOAD\_MAX}*30us}{(V_{ON\_PD}-V_{OFF\_PD})} = \frac{1.05*1.92A*30us}{(39V-33V)} = 10.08\text{uF}$$

when selecting practical Von and Voff with margins which take into consideration the presence of input diode bridge (3V on both Von_pd_max and Voff_pd_min)

M>=1 represents the effect of current increase due to voltage decrease as for constant load power. So actually the minimum capacitance will be higher than 10.08uF.

The factor 1.05 is the Ppeak_PD effect as well.