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Short MPS Detection Analysis-Recommended PSE, PD and Specification guidelines.

Last part of the discussion in
http://www.ieee802.org/3/bt/public/jan16/darshan_11_0116.pdf
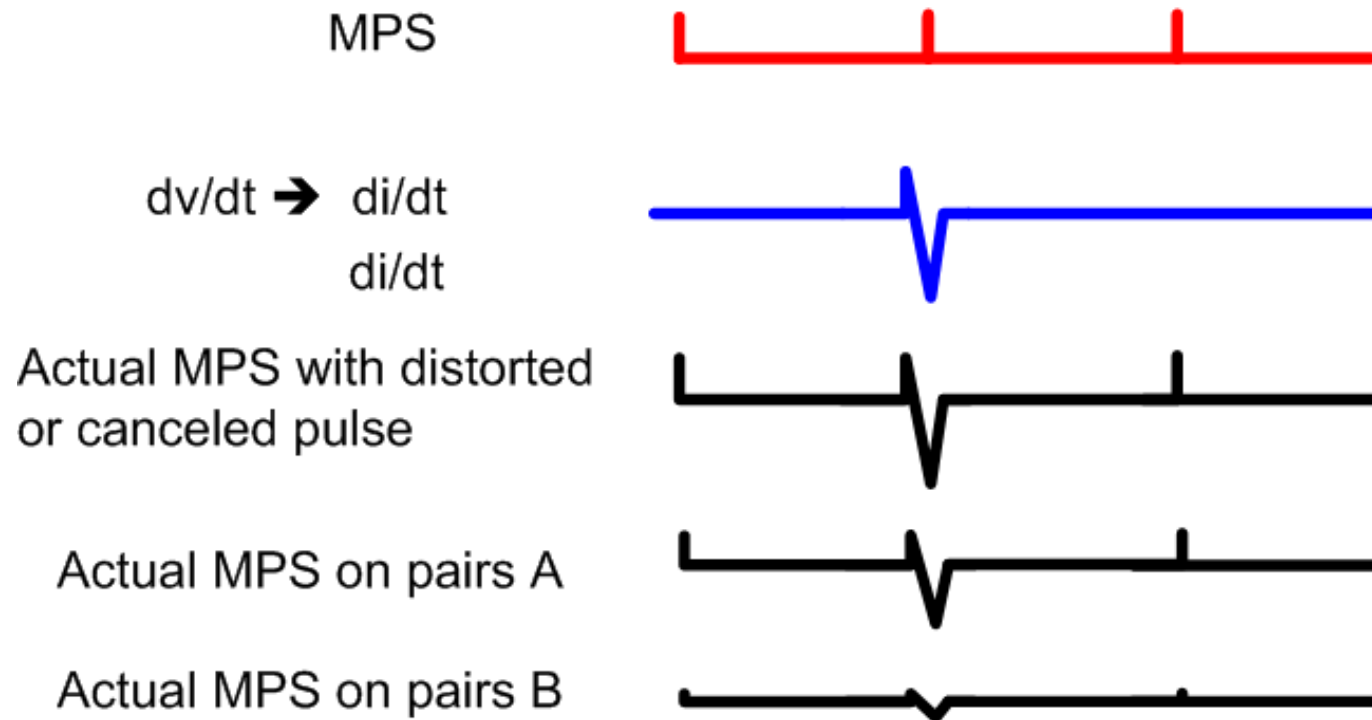
March 2016

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Objectives

- **To prevent false DC Disconnect when short MPS =7msec is used with Type 3 and 4 systems**

  - To investigate the reliability of detecting short MPS (7msec) in Type 3 and Type 4 PSEs connected to single-signature PDs in the following use cases:

    – Asynchronous PSEs trying to detect the pair with maximum current under unbalance conditions right after the transition from POWER_UP to POWER_ON.

    – PSE dv/dt

    – PD di/dt

    – PSE transition from POWER_UP to POWER_ON state causing PSE dv/dt and PD di/dt

  - For any MPS detection concept (SUM or pair with max. current)

- To present simple recommended guidelines.

- To define simple spec requirement.

The problem statement

- When short MPS pulse disappear because it was destroyed by noise/transient event of any kind, it means there is missing data, PSE can't do nothing about it. **We can't say this is PSE problem because it is undefined behavior. When behavior is defined, PSE can do something about it…**

- PSE can only assume that the PD is OK and ignore the missed pulse and decide to keep the port ON.

- OR

- The PSE can decide that there is MPS absent and to shut of the port.

- PSEs normally aware if he is the noise source and find the correct decision.

- The problem is that it is not specify what action the PSE may do in this case.

- How MPS pulse can be damage/distorted/disappear etc.? See next slides.

What is False DC Disconnect scenario?

MPS

dv/dt ➜ di/dt

di/dt

Actual MPS with distorted or canceled pulse

Actual MPS on pairs A

Actual MPS on pairs B

- The problem: Short MPS pulse width is within the system time constants for V/I transients.
- dv/dt of 1V/1ms will create 10mA current transient with just Cpd=5uF.
- If an MPS pulse is distorted or canceled due to di/dt event, the PSE may disconnect the power although the PD is connected and operating (*).
- It is a problem for lighting equipment that normally have fixed infrastructure and for other applications that "must work" is their main objective.

(*) In addition transient pulse may be added and cause PD to keep operating while MPS is truly absent. This is False maintain power situation. It depends on PD construction, Cpd, EMI filters, if using diode bridge or active diode bridge in the PD.

Background: when Type 1 and 2 MPS pulse was used or why in Type 1 and 2 we have no potential issues.

- **The minimum MPS pulse width is 75msec.**

- **75msec>>from all transient events (PSE dv/dt or PD di/dt)**

- **It is sufficiently large pulse duration that can survive any PSE-PD cross effect during transients and transitions between states e.g. POWER_UP to POWER_ON states.**

  - See details in: http://www.ieee802.org/3/bt/public/jan16/darshan_11_0116.pdf

- **As a result PSE can easily detect Type 1/2 MPS pulse.**
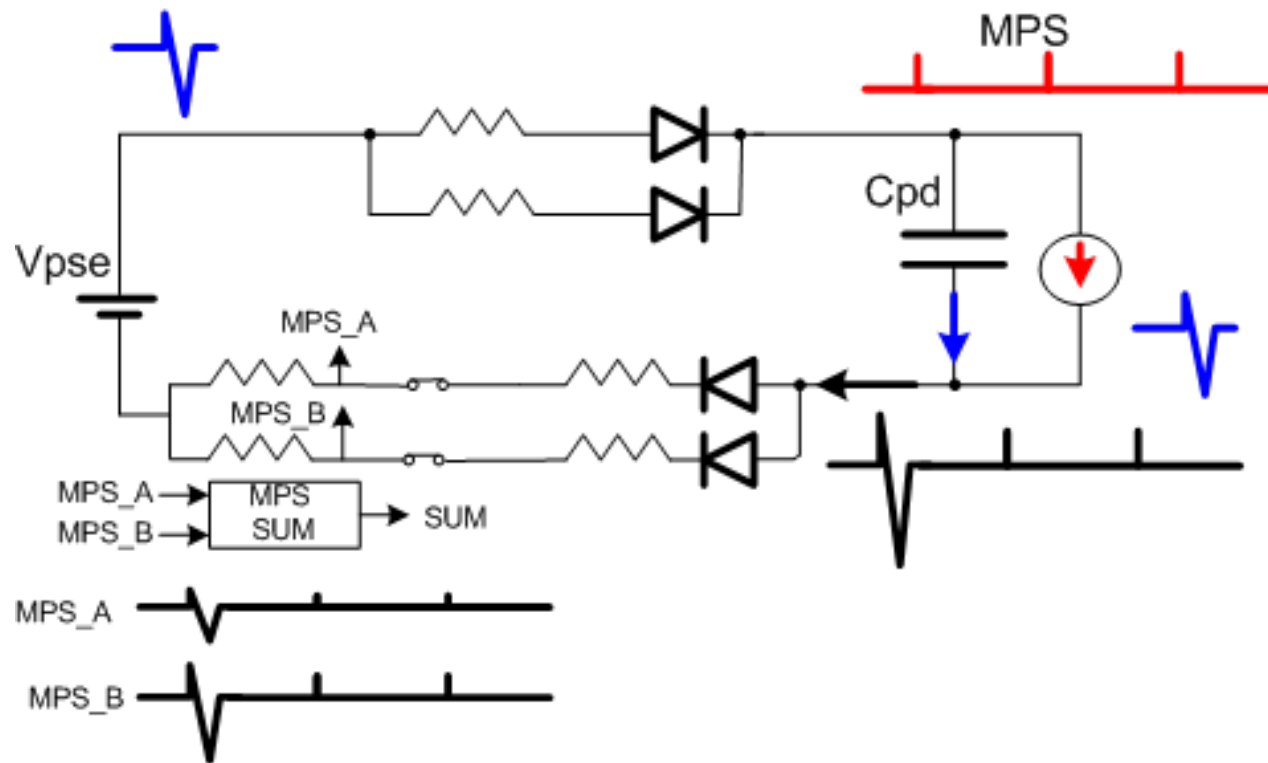
Background: when Type 3 and 4 short MPS pulse is used or why in Type 3 and 4 there is a potential false disconnect.

- The minimum MPS pulse width is 7msec. **10 times smaller.**

- 7msec pulse is closer to the range of practical PD load current transients and practical PSE dv/dt transients and may affected by it by way of cancelations and/or distortion of a single MPS pulse.

- In addition it is possible to miss the first pulse during transition between POWER_UP to POWER_ON(*).

- The above is relevant to:
  - All Type 3 and 4 PSEs architectures
  - All MPS pulse detection options (SUM or the pair with maximum current)

- As a result, the PSE may miss the detection of an MPS pulse within a TMP+MPDO cycle during any kind of transient **events**. See next slides for possible solutions.

- (*) during this transition PSE may miss detect the MPS current pulse due to dv/dt or di/dt or when asynchronous PSEs may miss the first pulse and may not be able to determine the polarity of the unbalance.

Case 1: Asynchronous PSEs and PSE dv/dt

- ## As shown in:
  http://www.ieee802.org/3/bt/public/jan16/darshan_11_0116.pdf

- It is possible that asynchronous Type 3 or 4 PSEs may missed the first MPS pulse during the transition of the PSE from POWER_UP to the POWER_ON or more important, the transition of the PD from Inrush to minimum MPS pulse current.

- ## <u>Solutions:</u>

- At the PSE side: Can be resolved by the PSE by many effective ways e.g. increasing the host sampling frequency or other techniques that we have discussed pending the PSE and PSE host architecture etc.

- PD side: Good design practice can be found in Annex A.

Case 2: PSE dv/dt and its effect on short MPS pulse current   -1

Example for what happen with multiport cross regulation or transition of power backup :
dv/dt=1V/1msec will generate 10mA peak current with Cpd=10uF .

- ▪ PD consume only minimum MPS pulse current
- ▪ PSE dv/dt cause di/dt in Cpd that sums up with MPS pulse
- ▪ The result is distorted MPS pulse or canceled MPS pulse
- ▪ PSE may miss the pulse and may disconnect the PD (*).

(*) Sensitivity of short MPS pulse to PSE dv/dt is increased when active diode bridge is used.

PSE dv/dt and its effect on short MPS pulse current   -2

- **Possible solutions in the PSE:**

- To allow PSE to ignore absence of MPSE pulse within TMPS+TMPDO cycle during any transient event in the system and keep the system ON.

PD dI/dt and its effect on short MPS pulse current

- PD di/dt will generate the same effect on MPS pulse current as if the PSE dv/dt cause the di/dt to the PD.

- However this is entirely controlled by the PD and can be avoided by PD design so the individual PD can take care of it in away that it will control the di/dt and ensure the MPS current pulse integrity.

Solution for all sources of MPS pulse distortion

To add the following text to clause 33.2.10.1.2 page 117 line 39:

Type 3 and Type 4 PSEs when operating with Type 3 and Type 4 short pulse MPS, may ignore MPS absence at any time within a TMPS+TMPDO cycle during transient events and may keep the pairset powered ON for the entire TMPS+TMPDO cycle when one of the following events is occurred:

a) During any PSE dv/dt transients which keeps the Vport_PSE within its operating range.

b) During any PD load current transient that is permitted by this spec.

c) During the transition from POWER_UP state to POWER_ON state.

Thank You

Annex A: Recommended guideline for the PD.
(It is not proposed as a PD requirement)

The following is the PD requirement regarding the transition form long MPS which is the default (short_mps=FALSE) value to short MPS (short_mps= TRUE) .

Type 3 and Type 4 PDs may determine if the PSE they are connected to supports low MPS by measuring the length of the first class event. The default value for short_mps is FALSE. If it chooses to implement low MPS, a PD may set short_mps to TRUE if the first class finger is longer than TLCF_PD min and shall set short_mps to TRUE if the first class finger is longer than TLCF_PD max.

Recommendations to handle PD unexpected behavior during the transition of PSE from POWER_UP to POWER_ON

Types 3/4 PDs will stay in short_mps=FALSE for at least TMPS+TMPDO time delay from POWER_UP start. After this time period they can move to short MPS. There is no need for this delay if PD is using minimum DC current above 10mA.