Analysis of High Side Current Sensing Architecture with Single Power Channel

System Efficiency, Accuracy, Thermal and System Costs Considerations

Jean Picard

May 2014

Supporters

- Fred Schindler / SeenSimply
- Kousalya Balasubramanian / Cisco
- Yair Darshan / Microsemi
- Miklos Lukacs / SiLabs
- Sesha Panguluri / Broadcom
- Antonio Garza / Cisco
- Victor Renteria / Bel Stewart & TRP Connector

Goal of this Presentation

The motivation of this work is to clarify and correct statements in stewart_01_0514.pdf presentation. This is done by analyzing the new architecture [1] which uses two high side current sensing elements and a single PSE power switch.

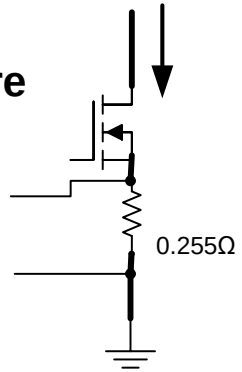
- Power Dissipation and Heat
- Current Measurement and FET Control Complexity
- System Cost

1 – See stewart, “4 Pair PoE Cost Comparison Redux”

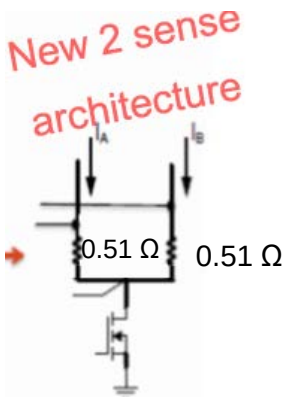
Impact of DC Disconnect Accuracy on High Side Current Sensing and System Efficiency

- The new architecture [1] uses one sense resistor per 2P, as shown below.
- As explained in previous presentation [2] , if “bt” PSE is connected to a single “at” PD interface, the DC disconnect threshold **CANNOT** change
  - ⇒ is same as defined in “at” spec: 5-10 mA
  - ⇒ **this mandates a “global” (4P) sense resistor value** of 0.255 Ohms[3] while doing DC disconnect measurement otherwise the accuracy of the measurement goes down.
  - ⇒In the present case, same current is split between 2 elements and there is still only one power switch, this mandates **0.51 Ω** per resistor, to just maintain same accuracy.
- The system power loss in high power is **the same**, there is **no** improvement and it is still problematic.

Old Architecture



New Architecture



1-power channel configuration drives all pairs at same time.

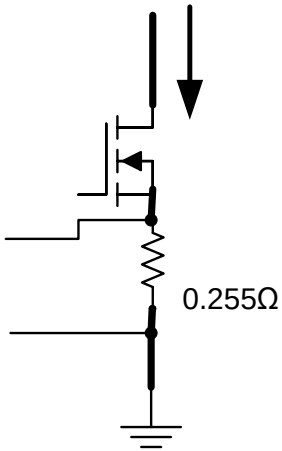
This limitation is due to its architecture.

2 – See Picard, “An Optimum Approach to Apply DC Disconnect”

3 - Lowest in industry sense resistor value used by PSE controllers working with external MOSFET is 0.255 Ohm.

Calculation Example

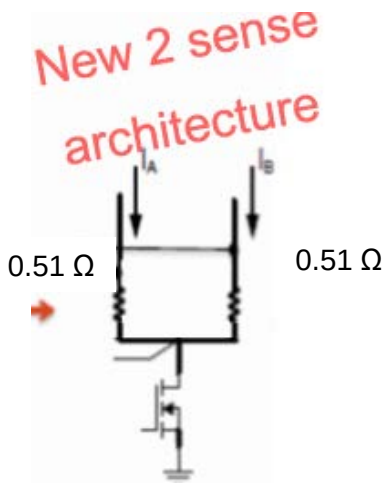
- PD with 51W input and 40m cable length (for more details see [2])
- As shown below, the system power loss in high power is **the same** as the old architecture, there is **no** improvement.
- As explained before [2], the 4P efficiency savings are (still) lost by excess power dissipation on the sense resistor. The concept of **4P power savings is lost.**
- Consequently, the following conclusions of document 1 are proven to be incorrect.
  - Slide 11 says "*Heat argument eliminated by 2 sense architecture*".
  - Slide 8 says "*Rsense argument eliminated by 2 sense architecture*



Old Architecture

Calculation Example:

$(1.08A)^2 \times 0.255\ \Omega = 0.296W$



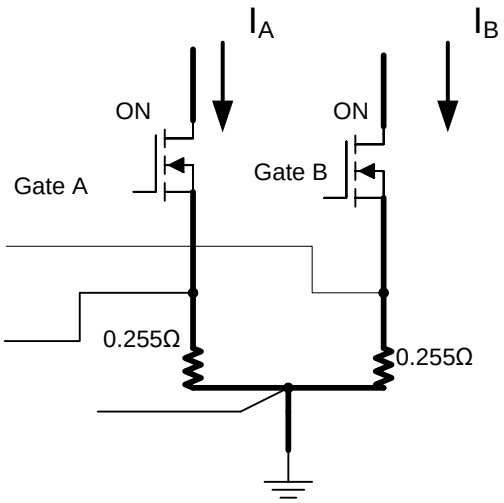
New Architecture

Calculation Example:

$(0.54A)^2 \times 0.51\ \Omega \times 2 = 0.296W$

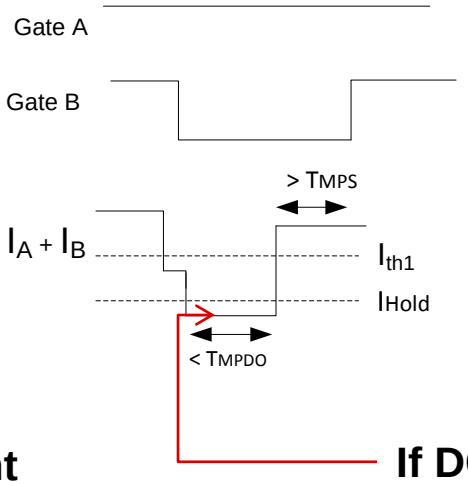
Why the 2 Switches Approach is More Efficient and Accurate at Same Time ?

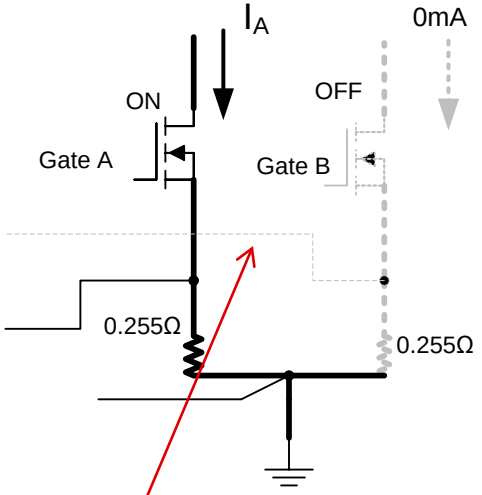
- **Methodology:**
  - Drive 4P if “bt” PD
  - If “at” PD:
    - Drive 4P, then when DC disconnect is “suspected”, do DC disconnect check with **1st switch only** for high accuracy.
  - This explains why with 2 switches, each sensing resistor can be as low as 0.255 ohm (and not 0.51 ohm).
- This method combines all the positive system aspects



If regular “at” load current

If “at”PD

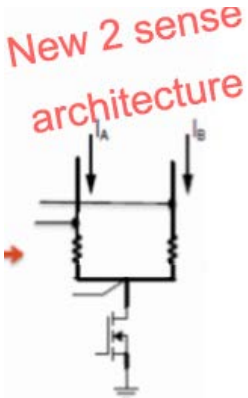




If DC disconnect is “suspected”

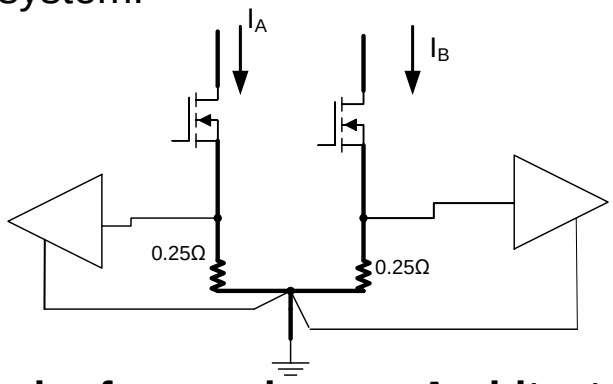
Additional Thermal Problems with High Side Current Sensing

- Dissipation is from 2 main elements, the FET and the resistor.
- The FET heat is usually transmitted to air through FET body and drain PCB trace/copper surface, which size is limited.
- The Resistor heat is usually directly transmitted to GND plane through electrical & thermal contact, which large copper surface helps to keep temperature low.
- But, with the high side sensing, the resistors are on the drain of the FET:
  - There is no longer any GND plane to which the resistor can transfer its heat.
  - **Where will the heat go?**
- Even worse, both the resistors and FET transfer their heat to the same drain trace, which is limited in size.
- This can be the source of serious FET temperature problems and failures.

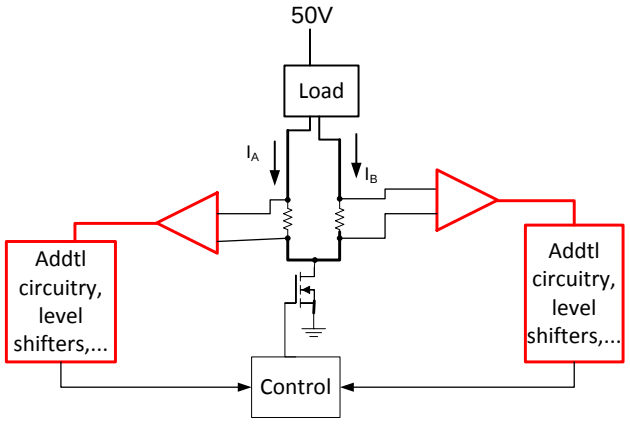


Other Considerations, Complexity & Costs

- Sensing voltage across a shunt with one side referenced to GND is easiest
- The architecture using two “floating” drain current sense resistors (one for each pair) introduces significant design complexity:
  - Requires means to shift that voltage down to digital domain voltage range.
  - Using a difference amplifier to measure a small voltage and ignore a large common mode voltage is challenging.
  - Even worse when the common mode is **“variable”** (the drain is not a constant voltage).
  - Requires accurate rail to rail, low offset/high speed, high CMRR current sense instrumentation amplifier for each of the current sense drain resistors
  - Needs additional circuit blocks for each sense resistor to manage high speed short circuit and closed loop ILimit control. Reaction to severe overload (ex: short circuit) must be fast, otherwise very high current may be reached which would be detrimental to the system.



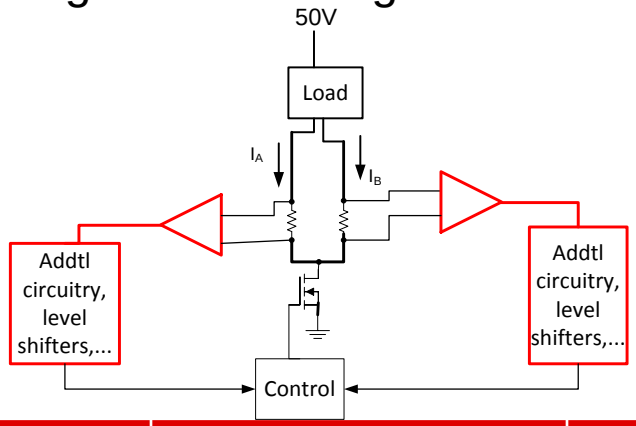
Simple Ground referenced sense Architecture



New 2 high side sense Architecture

High Side sensing: Complexity & Costs

- One approach would be to have floating circuitries “riding” on the DRAIN pin, adding a LOT of complexity.
  - Much larger size than a low side, high speed comparator with the direct feedback to the GATE amplifier .
- Another approach would be to fully isolate and float (for each channel) the A/D, Ilim and Isc blocks,…, which means fundamental changes.
- So, the savings with high side sensing would be minimal, if any.



	2-power channel	1-power channel High side Drain sensing
Gate Driver	2	1
Current Sense	2 very simple	2 Highly complex
# pins	+3 per 4P	+1 per 4P

Systems Costs and Complexity

- Below is a summary of overall cost per port.
- Note that document 1 says "*field data support 1.25x*" for the MOSFET is not clear. The 1.5x shown below is based on true high volume prices.
  - In fact, this factor could even be 2x, since the volume would be much lower for the bigger FET (most of "30W and lower" market would use a smaller FET).
- Also (not shown below), the 2-power channel architecture has indirect savings from being more efficient.

With high side sensing →

		Dual Power Channel		Single Power Channel	
Component	Weighting	Increase over AT*	Effective Contribution	Increase over AT*	Effective Contribution
Magjack	61.0%	15.0%	9.15%	35.0% → 15%	21.35% → 9.15% *
PCB	14.0%	0.0%	0.00%	20.0% → 35%	2.80% → 4.9%
PoE Controller	14.0%	100.0%	14.00%	40.0% → 90%	5.60% → 12.6%
FET	8.0%	100.0%	8.00%	50.0%	4.00%
Sense Resistor	1.5%	100.0%	1.50%	200.0%	3.00%
TVS Diode	1.5%	100.0%	1.50%	0.0% → 100%	0.00% → 1.5%
Total Cost Increase			34.15%		36.75% → 35.15%

* Magjack savings applicable only if **overload protection (ICUT) is a requirement per 2P** to avoid damage to the data transformers.

Summary

In summary, the high side drain current sensing combines all the negative system aspects of complexity, thermal, efficiency with *no* cost benefit.

PD Configuration	Dual Power Channel	Single Power Channel with High Side Sensing
"bt" PD Interface, High Power PDs	Simple thermal design	Thermal issues, highly problematic thermal design
Single "at" PD Interface	High accuracy, Low complexity	Highest PSE dissipation & temperature, Highest system + PCB cost, Highest Complexity
	Lowest PSE dissipation & temperature	
	Lowest system cost	
	Highest system efficiency	Medium-Low system efficiency