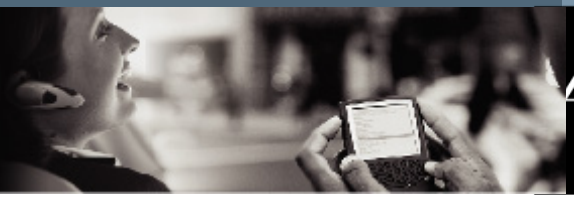
IEEE802.3bt
4 Pair PoE Cost Comparison Redux

H. Stewart – Linear Technology



LINEAR TECHNOLOGY

Goal of this Presentation

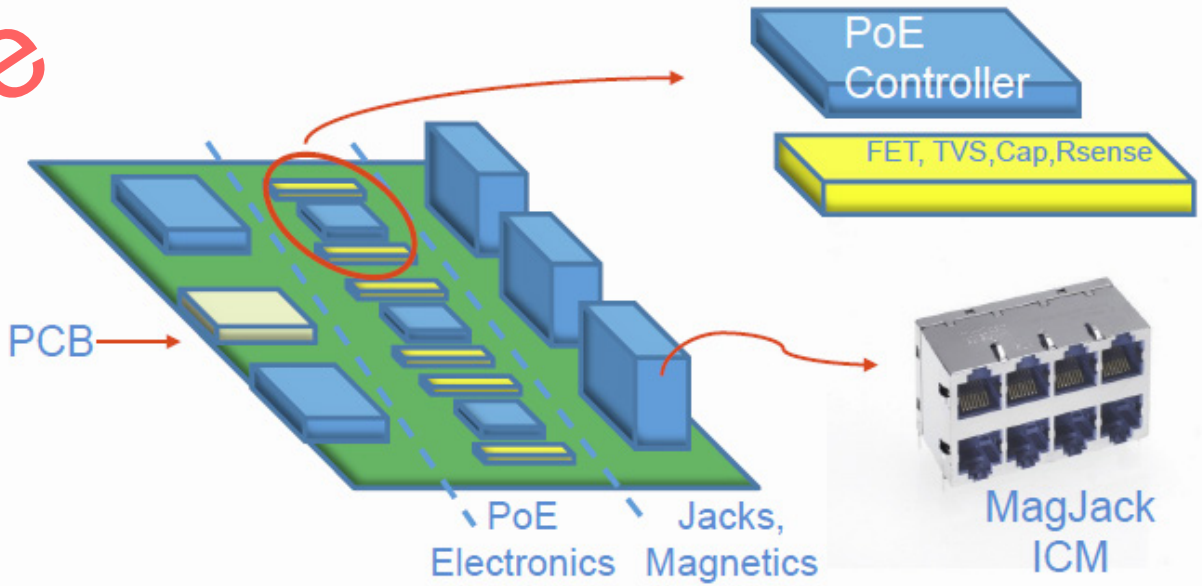
- Respond to March 2014 Cost Comparison presentation

“Markup” Approach

- Again, thanks to the team who put together the March 2014 Cost presentation
  - http://www.ieee802.org/3/bt/public/mar14/balasubramanian_02_0314.pdf
- Built these slides on top of March 2014 Cost presentation
  - Allows audience to compare approaches
  - Redlines used to call out differences
  - My hope is that this approach allows audience to view both sets of data without coloring data

PSE Breakout: 24-port 4PPOE Switch Example

Agree

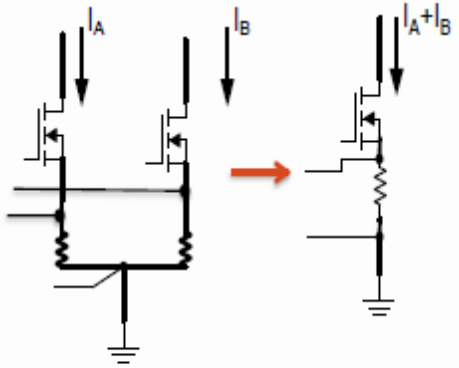


- Costs impacted by the choice of 2-Power Channel vs. 1-Power Channel architectures will be explored using a **24 Port Switch Use Case**
- The multipliers are compared to a 30W IEEE 802.3-AT base case
  - The multipliers are an estimate since actual prices and volumes vary
- The analysis includes components whose cost vary between the 2 implementations
  - Common components like Power Supply etc., are not included

PSE Breakout: Controller IC Cost Impact
External FET Solution

Solution	Cost Increase over 30W AT		Delta Between 1- and 2-Power Channel
	2-Power Channel	1-Power Channel	
External FET	2x	1.4x	-30%

- 1 Power Channel must support high accuracy ADC
  - 2x dynamic range/Higher SNR results in silicon cost increase
    - A larger dynamic range puts more stress on analog circuit design to meet accuracy requirements.
    - Could also require more complex digital circuitry.
    - Makes it more difficult to implement on low-cost mixed signal process[1].
- 2-Power Channel
  - Requires two “AT” chip ports per RJ45

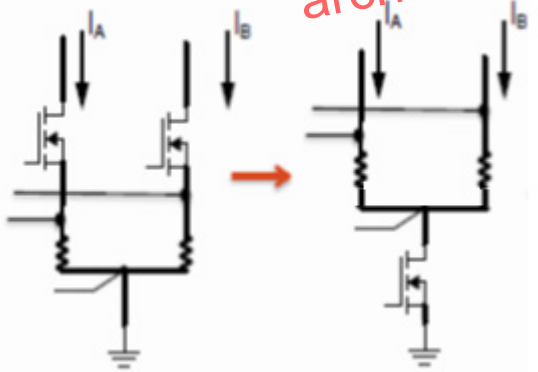


PSE Breakout: Controller IC Cost Impact
External FET Solution

Solution	Cost Increase over 30W AT		Delta Between 1- and 2-Power Channel
	2-Power Channel	1-Power Channel	
External FET	2x	1.2x ~~1.4x~~	-40% ~~-30%~~ (aka +67%)

- 1 Power Channel must support high accuracy ADC
  - ~~2x~~ dynamic range/Higher SNR results in silicon cost ~~increase~~
    - A larger dynamic range puts more stress on analog circuit design to meet accuracy requirements.
    - Could also require more complex digital circuitry.
    - Makes it more difficult to implement on low-cost mixed signal process[1].
- 2-Power Channel
  - Requires two "AT" chip ports per RJ45

New 2 sense architecture



LINEAR TECHNOLOGY

PSE Breakout: Controller IC Cost Impact Internal FET Solution

Agree

Solution	Cost Increase over 30W AT		Delta Between 1- and 2-Power Channel
	2-Power Channel	1-Power Channel	
Integrated FET	2x	1.8x	-10%

- 1 Power Channel
  - Silicon Area Increase
    - Major contributing factor for this size increase is the FET
      - Required to keep total power dissipation at acceptable level and match power losses
- 2 Power Channel
  - Requires two “AT” ports per RJ45

PSE Breakout: Port TVS/Rsense Components Cost Impact

Component	Cost Increase over 30W AT		Delta between 1- and 2-power channel
	2-Power Channel	1-Power Channel	
TVS	2x	2x ~~1x~~	0% ~~-50%~~
Rsense	2x	2x ~~3x~~	0% ~~+50%~~

- ***TVS***: 2-power channel case requires 1 TVS per 2-pair.
- ***Rsense***: Assumes same sense resistor value (for current measurement accuracy during DC-Disconnect for existing "AT" PDs

2 POWER CHANNEL:
Sample Power Dissipation per sense resistor: (for 60W Case)
- $P = I^2R = 0.6*0.6*0.25 = 0.09W^1$
- Including derating 0.25W rated sense would be good
- Sense Resistor Size – 1809

1 POWER CHANNEL:
Sample Power Dissipation per sense resistor: (for 60W case)
- $P = I^2R = 1.2*1.2*0.25 = 0.36W.$
- Including derating 1W rated sense would be good
- Sense Resistor Size – 2512

Rsense argument eliminated by 2 sense architecture

External

PSE Breakout: Port FET Component Cost Impact

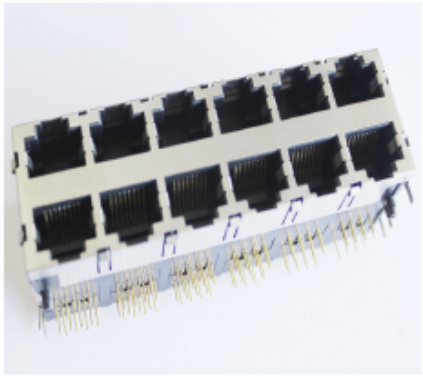
Component	Cost Increase over 30W AT		Delta between 1- and 2-power channel
	2-Power Channel	1-Power Channel	
FET	2x	~~1.5x~~ 1.25x	~~-25%~~ -40%

- FET Choice is controlled by two considerations
  - Thermal Dissipation during normal operation
  - SOA (Safe Operating Area)
- Same power dissipation for 2 Power Channel and 1 Power channel assumed

2 POWER CHANNEL:	1 POWER CHANNEL:
- Current per FET = Iport/2 - Twice number of FETs per port	- Current per FET = Iport - SOA performance for 1 Power channel should support higher current compared to 2 power channel in all situations (including Short circuit) - FET die Size of 1 power channel = 2 X FET die size of 2 power channel → Cost Impact

Field data supports 1.25x multiple

PSE Breakout: Magnetics/Jack Cost Impact



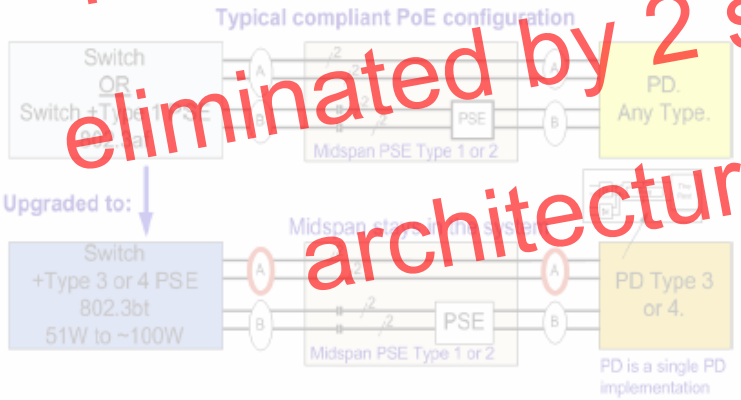
Cost Increase over 30W AT		Delta between 1- and 2-power channel
2-Power Channel	1-Power Channel	
1.15x[2]	1.15x ~~1.35x~~[1,2]	0% ~~27%~~

1,2 – See "Magnetics Cost Increase Notes" in backup slides for more information.

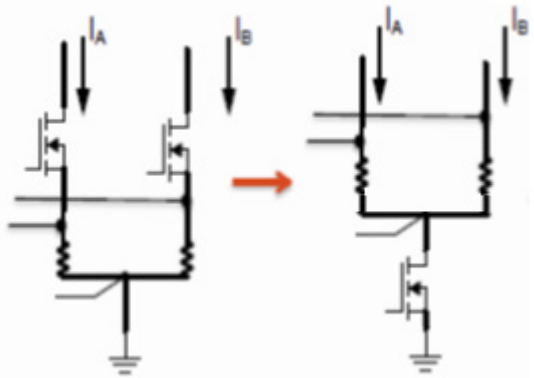
2 POWER CHANNEL:
- Independent control over each 2pair
- Worst case current per 2 Pair magnetics = Iport/2

1 POWER CHANNEL:
- Has no independent control over each of the 2pair
- Worst case current per 2 pair magnetics = Iport (refer to picture below)
- To avoid damage, bigger Magnetics needed to handle higher current → Cost Increase

MagJack argument eliminated by 2 sense architecture

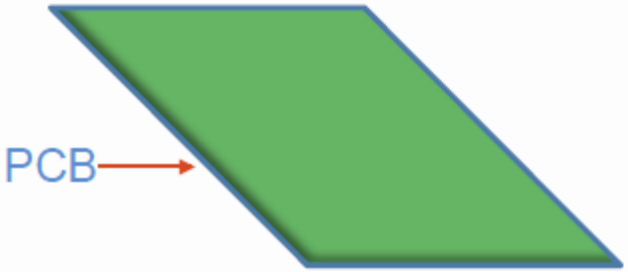


- When there is a 2-p
  span connected to
- If end span wins th
  - 1 power chann
    on one 2-pair.
  - For example, if
    provided over 2
    Magjack as opp



LINEAR TECHNOLOGY

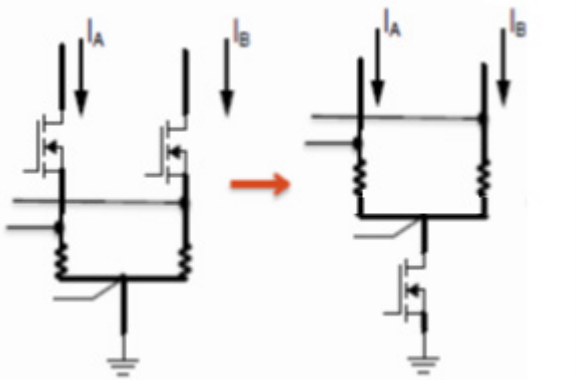
PSE Breakout: PCB Cost Impact



Cost Increase over 30W AT		
2-Power Channel	1-Power Channel	Delta between 1- and 2-power channel
1x	1x ~~1.2x~~	0% ~~+20%~~

- Thermal Dissipation needs drive increased cost
  - Using the 1-power channel approach instead of the 2-power channel approach introduces additional dissipation
    - For a group of 4 ports operating at high power (60W PSE output):
      - 1-Power channel has 2X dissipation compared to 2-Power channel
        - Since the Rsense voltage is same between 2-Powe
          provide accuracy
      - Multiple GND planes, thicker copper (ex: 2 our
      - Larger board area needed for same number
      - Maximum number of high power ports per unit

Heat argument eliminated by 2 sense architecture



LINEAR TECHNOLOGY

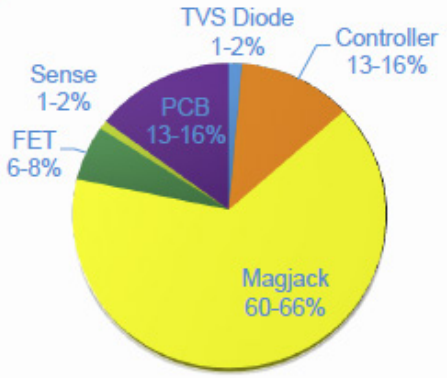
PSE System Comparison: Component Cost Weighting

Agree

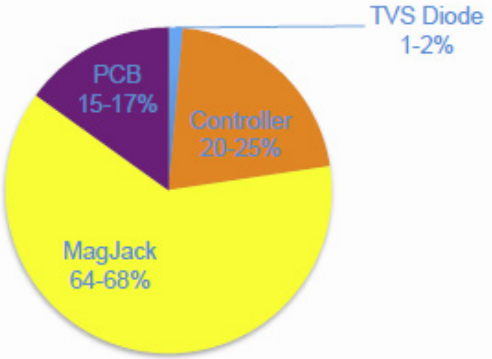
- Not all components contribute equally towards system cost
- Contribution in a typical base system of 2Pair 30W is shown
  - These percentages were taken from a variety of sources and vendors; thus ranges are given for each component

Component	Contribution in 30W 2-Pair External FET solution	Contribution in 30W 2-Pair Internal FET Solution
Sense	1-2%	NA
FET	7-9%	NA
TVS diode	1-2%	1-2%
Controller	13-16%	20-25%
PCB	13-16%	15-17%
Magjack	60-66%	64-68%

Component Contribution – External FET



Component Contribution - Internal FET



- The minimum of the component contributions are used along with the multipliers shown in slides 8-13 to arrive at the total system comparison between 1-power and 2-power channel

LINEAR TECHNOLOGY

PSE Breakout: Cost Comparison Summary
External FET Solution

- Taking into consideration the weighting of the various components, the data shows that when building a 60W system using external FETs:

17% more costly

The 2-Power Channel architecture is approximately ~~2% less~~ costly than the 1-Power Channel architecture.

$$\Delta = 1 - 1 + Dual\ Power\ Channel\ Cost\ Increase / 1 + Single\ Power\ Channel\ Cost\ Increase = 1 - 1 + 0.34 / 1 + 0.37 = 0.02$$

		Dual Power Channel		Single Power Channel	
Component	Weighting	Increase over AT*	Effective Contribution	Increase over AT*	Effective Contribution
Magjack	61.0%	15.0%	9.15%	15% ~~35.0%~~	9.15% ~~21.35%~~
PCB	14.0%	0.0%	0.00%	0% ~~20.0%~~	0% ~~2.80%~~
PoE Controller	14.0%	100.0%	14.00%	20% ~~40.0%~~	2.8% ~~5.60%~~
FET	8.0%	100.0%	8.00%	25% ~~50.0%~~	2% ~~4.00%~~
Sense Resistor	1.5%	100.0%	1.50%	100% ~~200.0%~~	1.5% ~~3.00%~~
TVS Diode	1.5%	100.0%	1.50%	100% ~~0.0%~~	1.5% ~~0.00%~~
Total Cost Increase			34.15%		16.95% ~~36.75%~~

* Cost increase indicated is for a 60W system compared to a 30W AT system.

LINEAR TECHNOLOGY

PSE Breakout: Cost Comparison Summary
Internal FET Solution

- Taking into consideration the weighting of the various components, the data shows that when building a 60W system using external FETs:

The 2-Power Channel architecture is approximately 7% less costly than the same cost as the 1-Power Channel architecture.

$$\Delta = 1 - 1 + Dual\ Power\ Channel\ Cost\ Increase / 1 + Single\ Power\ Channel\ Cost\ Increase = 1 - 1 + 0.31 / 1 + 0.41 = 0.07$$

		Dual Power Channel		Single Power Channel	
Component	Weighting	Increase over AT*	Effective Contribution	Increase over AT*	Effective Contribution
Magjack	64.0%	15.0%	9.60%	15% 35.0%	9.15% 22.40%
PCB	15.0%	0.0%	0.00%	0% 20.0%	0% 3.00%
PoE Controller	20.0%	100.0%	20.00%	100% 80.0%	1.5% 16.00%
TVS Diode	1.0%	100.0%	1.00%	100% 0.0%	1.5% 0.00%
Total Cost Increase			30.60%		30.60% 41.40%

* Cost increase indicated is for a 60W system compared to a 30W AT system.

LINEAR TECHNOLOGY

60W vs 100W PSE Thought Experiment

- LPS limits PSE output power to 100W
- At V_{PSE_MAX} = 57V, I_{100W_MAX} = 1.75A
  - Derate this number by 10% to account for CUT accuracy and LPS margin
  - 100W Power per pairset is 1.575/2 = 788mA
  - 60W Power per pairset is 600mA
- For a given FET and Rsense technology an IC supports a limited power density
  - 100W Power per pairset is $I^2R = 0.788^2 \times R = 0.62R$
  - 60W Power per pairset is $I^2R = 0.6^2 \times R = 0.36R$

60W vs 100W Thought Experiment Cont'd

- Internal FET PSE architectures are limited by their ability to avoid generating and/or safely dissipating heat

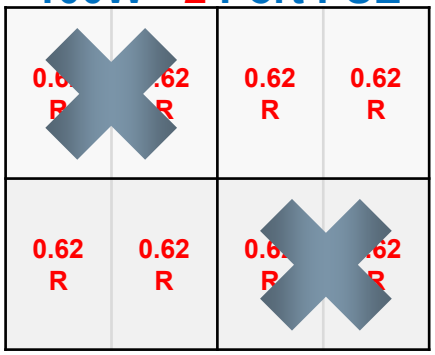
60W - 4 Port PSE

IC Max Power = 2.88R

100W - 4 Port PSE

IC Max Power = 4.96R

100W - 2 Port PSE



IC Max Power = 2.48R

Conclusions

- Based on revised Single Power Channel architecture
  - External FET 1-Power Channel has a 17% cost advantage over 2-Power Channel architecture
- External FET 1-Power Channel architectures have an intrinsic advantage above 51W
  - Modern FET technologies aggressively reduce Θ_{JC}
  - FET technology will remain cheaper / R_{DSON}

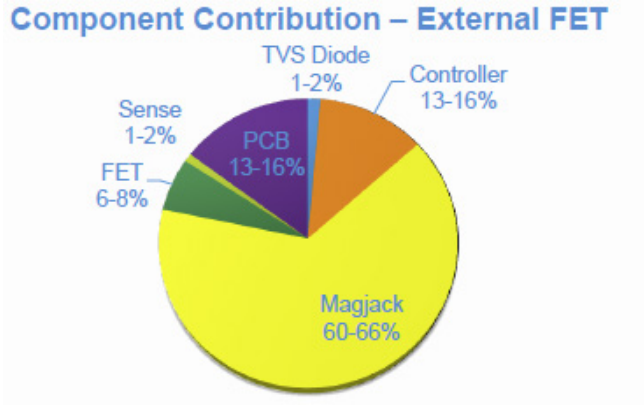
Appendix

Critique

- March 2014 Cost presentation was based on the following premise:

  - The analysis includes components whose cost vary between the 2 implementations
    Common components like Power Supply etc., are not included

- Which resulted in the following weighting



Critique Cont'd

- Carrying this premise forward would result in *only* the Controller and FETs as comparison points
  - These are the components whose costs vary
- The result is the following:

			Dual Power Channel		Single Power Channel	
	Old Weight	New Weight	Increase over AT	Effective Contribution	Increase over AT	Effective Contribution
FET	7%	32.6%	100%	32.6%	25%	8.1%
Controller	14.50%	67.4%	100%	67.4%	20%	13.5%
Total				**100.0%**		**21.6%**

* Cost increase indicated is for a 60W system compared to a 30W AT system.