IEEE802.3bt May 2014 Cable Balance Ad-Hoc Minority Report PSE and PD PI Specifications Rev 1.2

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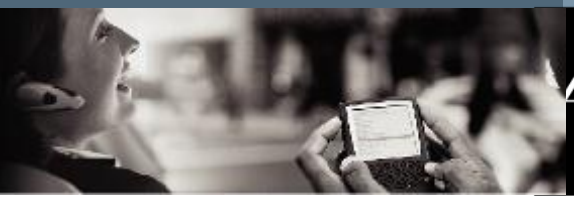

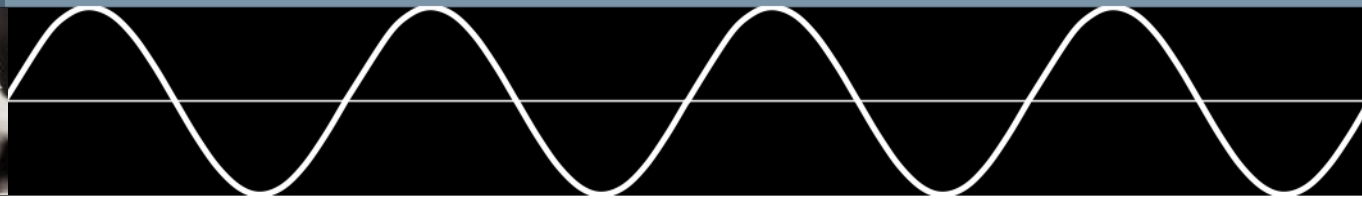

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Goal of this Presentation

- Provide an alternative basis for discussion of the PSE and PD PI specification to facilitate a consensus for a motion in the ‘bt’ task force and creating imbalance specifications for the PSE and PD PI and the channel.
- Good work has been done and continues to be done in the Ad-Hoc based on likely PSE and PD configurations
- Present an alternative product for the Ad-hoc
- Show some interesting link segment information

Where we are

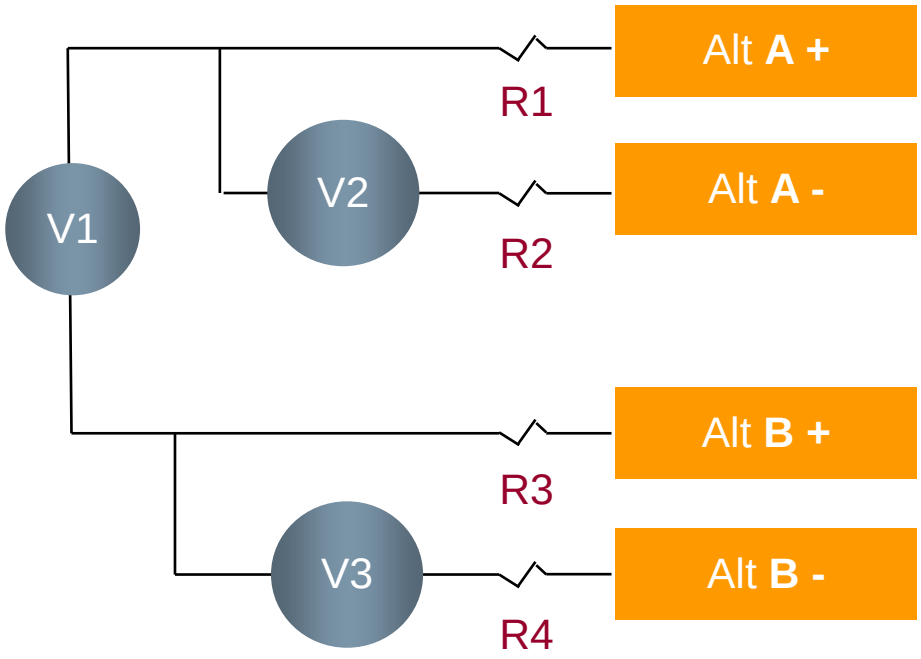
- System simulations are essential
- System simulations are a good way to help create a PI for a the PSE and PI
- The entire ‘link segment’ resistance imbalance has provided by the channel guys. (see below)
  - Not need to create it using cable/connector values

Where we are

- Fix reasonable values for the PSE PI and PD PI based on current PSE design knowledge base
  - We know what it should be
  - Our goal is to prevent wacky implementations
- Simulate all 3 system components with careful selection of worst case values (for the two PIs and the link segment) at multiple current levels.
  - ***Report highest individual pair current vs power level.***
  - ***This is the proposed ad-hoc product.***
    - ***Not a % imbalance number***

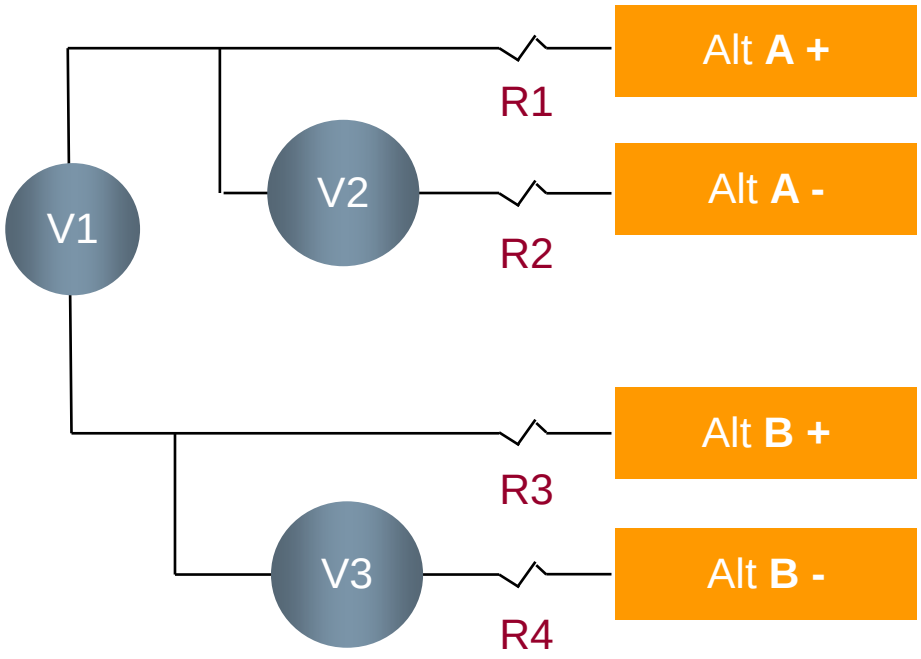
A Necessary and Sufficient PSE PI Model suggestion. Slide 1

- **This is not an implementation centric model, it is a PSE PI centric model.**
- Thinking of a PSE PI without respect to implementation requires these parameters, or equivalent parameters to be specified to ensure interoperability with respect to current imbalance (and perhaps other important interoperability concerns) and safety concerns.
- For SELV, we know that any two of the four outputs (really 8 wires) must never be more than 60V (or 57 in IEEE PoE) measured at 'Alt' pins



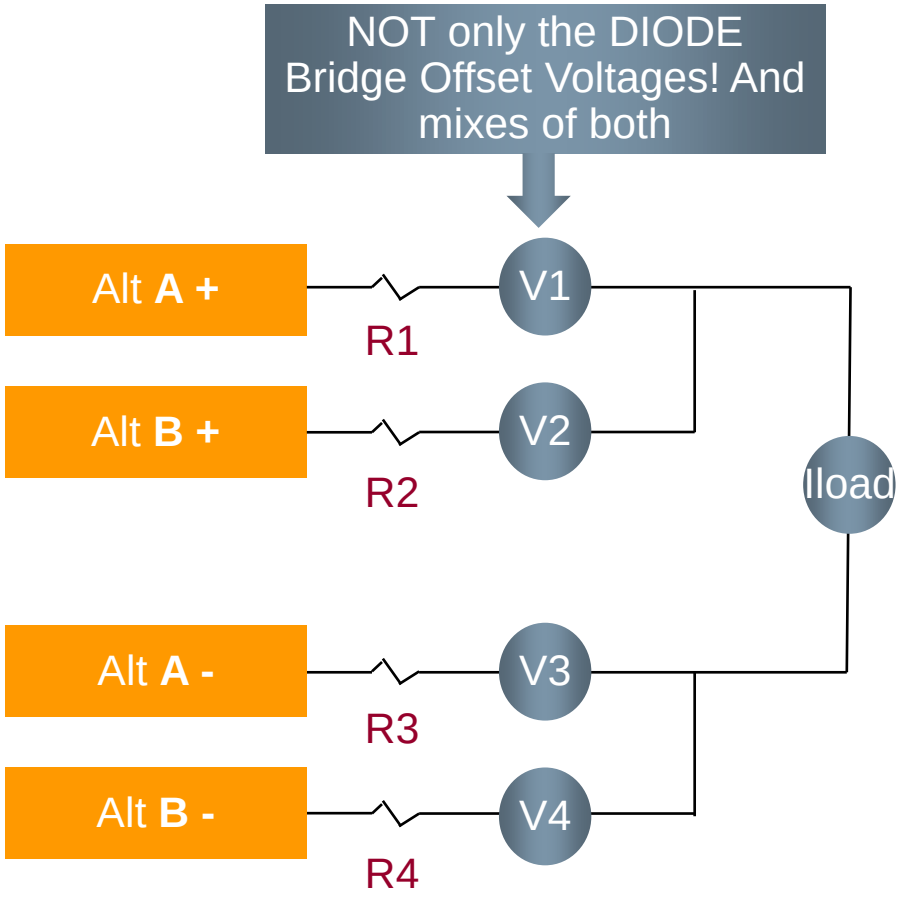
A Necessary and Sufficient PSE PI Model suggestion.

- In this model, a way to specify the PI:
  - R1, R2, R3, and R4 must have a matching specification
  - V1 must be below a specified voltage
  - V2 and V3 must be within a specified delta voltage
- It may be a good idea to specify 8 resistors and create rules to cover single pair imbalance but I am not currently advocating this.



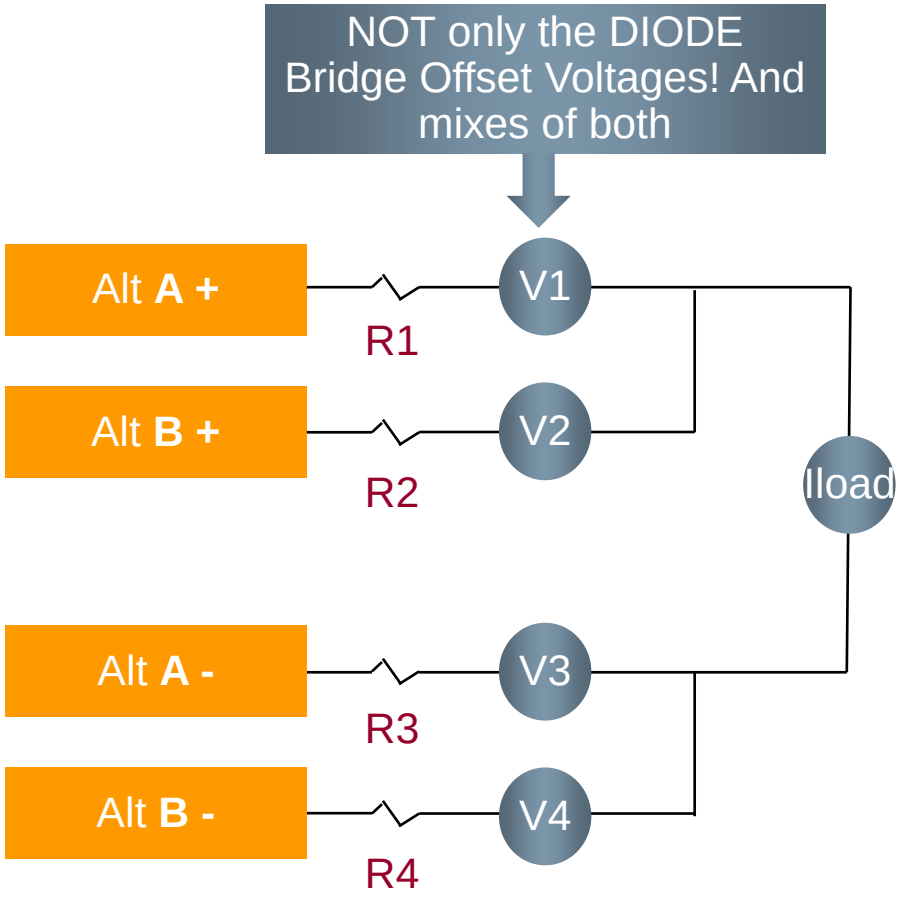
A Necessary and Sufficient PD PI Model Suggestion.

- **This is not an implementation centric model, it is a PSE PI centric model.**
- Thinking of a PD PI without respect to implementation requires these parameters, or equivalent parameters to be specified to ensure interoperability with respect to current imbalance (and perhaps other important interoperability concerns).
- The PD is a power user so SELV is not a problem and may not source voltage/power



A Necessary and Sufficient PD PI Model Suggestion.

- In this model, a way to specify the PI:
  - R1, R2, R3, and R4 must have a matching specification
  - V1 - V2 must be within a specified delta voltage
  - V2 - V3 must be within a specified delta voltage
- It may be a good idea to use 8 resistors and create rules to cover single pair imbalance but I am not currently advocating this.



Suggested method of specifying Current Imbalance - PSE

- PSE PI specification from above
  - Voltage offset and resistance imbalance
- Testing methodology
  - Measure 4 (or 8) Vouts at the PI under DC disconnect current
  - Measure 4 (or 8) Vouts at the PI under PSEs maximum current output
  - Calculate Voltage Offset and Resistance Offset of the PSE PI (using ohms law)

Suggested method of specifying Current Imbalance - PD

- PD PI specification from above
  - Voltage offset and resistance imbalance
- Testing methodology
  - Measure 4 (or 8) Iouts at the PI at minimum PD PI input voltage
  - Measure 4 (or 8) Iouts at the PI at maximum PD PI input voltage
  - Calculate Voltage Offset and Resistance Offset of the PD PI (using ohms law)

Suggested path forward

- Take the channel resistance imbalance numbers to 6% or 200mOhms which ever is greater
- Revisit the model parameters per yesterday's ad-hoc inputs
- Create reasonable numbers for the PSE PI and PD PI using the Voltage Offset and Resistance Offset model for the PI interface
- Simulate for different channel currents from Class 1 to new chosen maximum current
- Provide maximum current in any pair at the PI based on the above simulation.

Suggested Ad-Hoc Product

PSE Output Power Level (W)	Maximum Pair Current (mA)
3.84	xxx
…	…
…	…
…	…
…	…
95	xxx

Temperature effects on the link segment length in theory compensate for increased resistance due to Cu heating

G.3 Allowance for cable temperature

Table G.2 shows the maximum horizontal cable length de-rating at various temperatures assuming a cable insertion loss temperature coefficient specified in clause 6.4.7.

Table G.2 – Maximum horizontal cable length de-rating factor for different temperatures

Temperature (℃ (℉))	Maximum horizontal unscreened cable length (m)	Maximum horizontal screened cable length (m)	Length de-rating (m) (unscreened)	Length de-rating (m) (screened)
20 (68)	90.0	90.0	0	0
25 (77)	89.0	89.5	1.0	0.5
30 (86)	87.0	88.5	3.0	1.5
35 (95)	85.5	87.7	4.5	2.3
40 (104)	84.0	87.0	6.0	3.0
45 (113)	81.7	86.5	8.3	3.5
50 (122)	79.5	85.5	10.5	4.5
55 (131)	77.2	84.7	12.8	5.3
60 (140)	75.0	83.0	15.0	6.0

NOTE - This table assumes that the channel includes 10 meters of patch and equipment cords at 20° C.

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Some observations on the maximum current vs temperature the ad-hoc may choose to report

- 20 degrees C may be the temperature we want to report our results at
- Currently it looks like the worst case maximum current through a transformer is with the longest cable – highest resistance – highest overall current
  - PD is a constant power source
- Resistance does not materially increase with temperature because the link segment is shortened
- Colder temperatures will lower the resistance and therefore current.

CAT5 vs CAT6 Link Segment Resistance

- It came to my attention that the resistivity difference between our CAT5 and CAT6 Link Segments may be small enough that we may choose to treat them equally for power delivery.
- Martin Rossbach – Nexans Cabling Solutions
- Bob Wagner – Panduit
- Dave Hess – Cord Data

Summary 1 – Ad Hoc Suggested Output

- Percent imbalance for the system should be replaced with maximum pair current under worst case conditions vs. currents from the 13W af level, 25.5W at level, 51W level and maximum power ‘bt’ can deliver
  - This has been generally shown to be a the longest cable length but it should be checked at several length as current simulations show not linear behavior

Summary 2 – PI Definitions

- Specify PSE PI as 3 voltage sources and 4 imbalance resistances per above
- Specify PD PI as 4 voltage sources and 4 resistors per above

Summary 3 – CAT6 cable resistance

- Obtain new CAT6 cable resistance numbers as the current ones are based on AWG and do not account for the added actual length of the conductors due to added twist

Summary 4 – Cable resistance imbalance

- Change ‘Channel’ resistance to 6% or 200mOhms which ever is greater