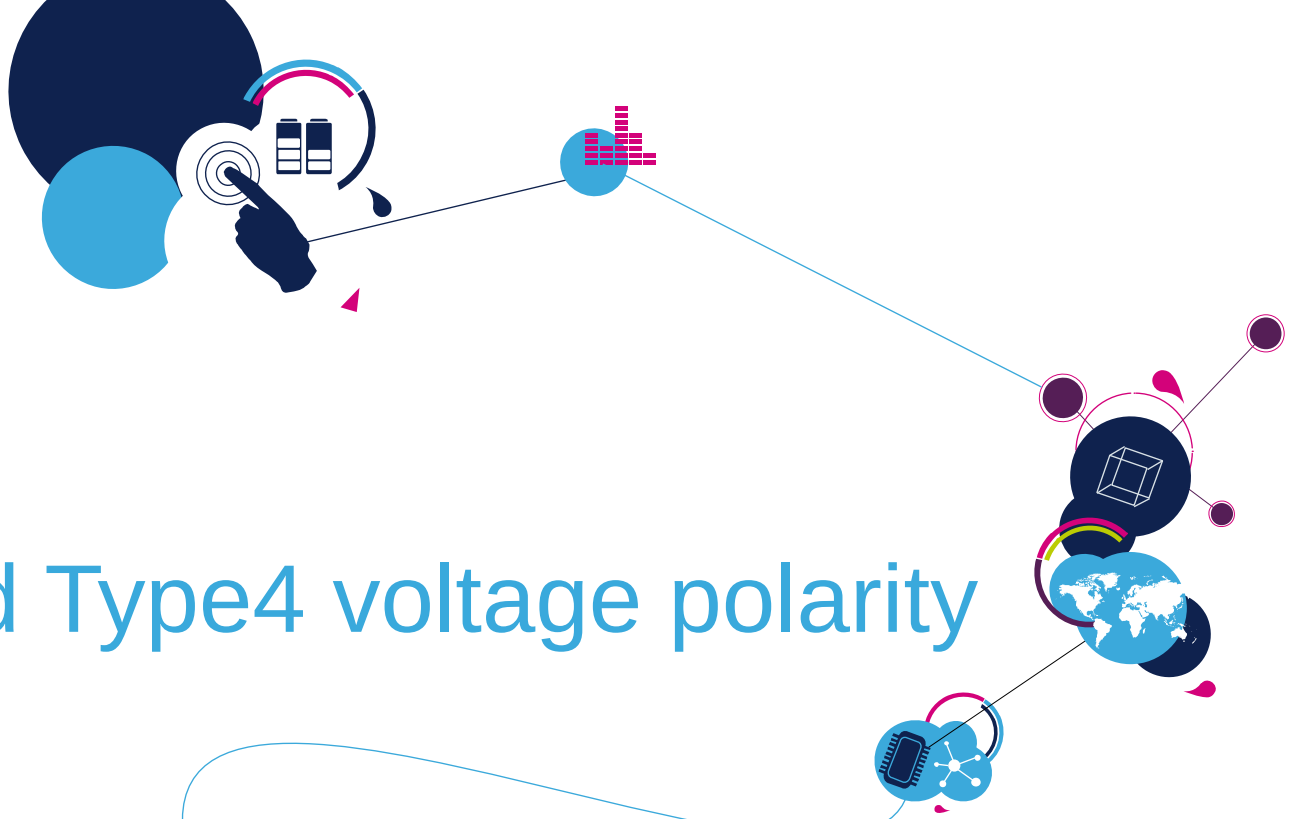

Type3 and Type4 voltage polarity

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Background

- ✓January presentation about the need for PD rectification bridges in 4P systems was very controversial.
- ✓There are two main opinions on the group:
  - ✓The main goal of this Task Force is to make the highest power available for the final PoE users maximizing system efficiency
  - ✓Interoperability with Type 1 and Type2 PSEs must be preserved for Type3 and Type4 PDs
- ✓Both opinions are good and valid. Is it possible to make them coexist?

Diode bridge presence reasons

- Diode bridges at PD input make any PD interoperable with any PSE and cable installation - no worries for cable types – it's "plug & play"
- Calls for failures from the field are expensive for manufacturers
- Non-interoperable systems are a bad advertisement for a standard
- If a negative voltage is wrongly applied to the PD with no protection, some damage may occur

Diode bridge absence reasons

- Diodes are one of the main contributors of losses and current unbalance in a 4P System
- Active bridges are a viable alternative to diodes, but still introduce losses and add system complexity
- If input polarity was known, no diodes would be required*.
  - There is no reason to leave the PSE PI voltage polarity undefined (Auto MDI-X is a data-only feature)
  - The only reason for an undefined voltage polarity at PD PI is the presence in the field of Crossover Cables.
- Crossover cables are less and less useful since Auto MDI-X feature is widely adopted

actually at least one diode is needed for Vbfd, see slide #7 for more details

Power losses estimation

- It is possible to calculate the losses related to input bridge. During the discussion on the reflector, it was proposed an estimation for the losses related to a 51W 4P system*:
- Polarity insensitive solutions:
  - **Schottky diodes**: 2*0.9W (or 4*0.6A*0.75V) = **1.8W** – easy (3.5% efficiency loss)
  - **4-FET Active bridge**: -75% = **0.4W** – more complex (0.8% efficiency loss)
- Fixed polarity solutions:
  - **One-FET** solution: -90% = **0.18W** – easy (0.35% efficiency loss)

**data provided by Jean Picard on 2/12 on the reflector discussion*

New Type Definitions

- It is proposed that in the new standard there will be two types of PSEs and PDs*
- *Type 3, 4-Pair operation, 0- 60W at PSE PI, new MPS*
  - *Can use existing Type 2 cable definitions*
- *Type 4, 4-pair operation, 0 - <100W at PSE PI , new MPS*
  - *New cable definition needed (cable type, bundle size etc.,)*
- In order to allow Type 4 systems to deliver more than 60W, we are going to define new cabling requirements**
- Current installations have to be checked to be compliant with the new requirements in order to be able to run a Type4 system.

**see abramson_01_0514.pdf*
*** as done for Type 2 requiring Class D as min power type (Tab 33-1 and 33.1.4.1).*

Proposal for Type 3 and Type 4

- Since a Type3 system is going to be defined to be compatible with current installation, it is not possible to avoid diode or active bridge at Type3 PD input.
- Type4 PDs will require a new Type4 PSE to provide the max power and an upgraded cabling infrastructure. Why not to disallow crossover cables for such infrastructure?
- Type4 PD would anyway have at least one current-directional element at its inputs for two reasons
  - 1. To avoid any damage from accidental reverse polarity application
  - 2. To comply to backfeed voltage specification (still needed)
  - One element has half losses and lower complexity with respect to a bridge.
- Type4 PD is not precluded to use full bridges at input if needed

FAQs

- I want to design a fixed polarity Type4 PD. Do I need to tell my customer to check their cabling infrastructure?
  - Yes. You have to make sure that they are using CAT6/A or better cables. That they are not tied into a > TBD bundle. And that they are not crossover cables.
- What kind of calls from the field can I expect when selling Type4 PDs?
  - A Type4 system with input bridge installed on existing cabling infrastructure may succeed at startup, but fail under certain load condition for cable overheating (e.g. if the max bundle size exceeds Type4 specs)
  - A Type4 system with no input bridge plugged into a crossover cables won't startup. It's easier to catch. The failure is at time zero. It is safe.
- Any new PD must indicate it's underpowered – how to do it if it's reversed biased?
  - Putting a reverse biased LED (normally off) in parallel at the PD input.
  - When the PD is connected to a reverse voltage PSE (I.e. Type 1-3) it turns on
- How to comply with backfeed voltage spec?
  - A single element per pair (diode or FET) is necessary and sufficient.

Baseline proposal

- In order to allow Type4 PDs to be designed without input bridge a few modifications are required in the text
- 1. To require that at least Type 4 PSEs – but I'm suggesting Type 3 PSEs as well – to implement both Alt-A (MDI-X) and Alt-B
  - Type4 (and Type3) PSEs implementing Alt-A (MDI) shall be specifically disallowed
- 2. To define new Table 33-13A for Type4 PD pinout. Table 33-13 will not be modified, ad it still remain valid for Type1, Type3 and Type3 PDs
- 3. To allow Type 4 PD to accept power with the polarity defined in the new Table33-12A
  - Type4 PDs may optionally be able to accept power as defined by Table 33- 12

Baseline proposed text (1)

- Modify 33.2.3

  A Type 1 or Type 2 PSE shall implement Alternative A, Alternative B, or both, while a Type 3 or Type 4 PSE shall implement both Alternative A (MDI-X) and Alternative B.-Type3 and Type4 PSEs implementing only Alternative A or Alternative B, or implementing both Alternative A (MDI) and Alternative B are specifically disallowed.

  ~~While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the samelink segment simultaneously.~~

Baseline proposed text (2)

- Change Table 33-13 title

Table 33–13– Type 1, Type 2 and Type 3 PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_{P}, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

Baseline proposed text (3)

- Add Table 33-13A table

Table 33-13A – Type 4 PD pinout

Conductor	Mode A	Mode B
1	Negative VPD	
2	Negative VPD	
3	Positive VPD	
4		Positive VPD
5		Positive VPD
6	Positive VPD	
7		Negative VPD
8		Negative VPD

Baseline proposed text (4)

- Modify 33.3.1

  The PD shall be capable of accepting power on either of two sets of PI conductors. The two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 and Table 33-13A illustrates the two power modes.

  A Type 1, Type 2 and Type3 ~~The~~ PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

  A Type 4 PD shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13A. A Type 4 may optionally be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

  ~~NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.~~

  The PD shall not source power on its PI.

Thanks!

Straw poll(1)

- I support a modification of clause 33.2.3 in order to define a fixed voltage polarity at the PSE PI for Type3 and Type4

- Y:__
- N:__
- A:__

Straw poll(2)

- I support a modification of clause 33.3.1 in order to define a fixed voltage polarity at the PD PI for Type4

- Y:__
- N:__
- A:__