Comment #126, Clause **145.2.8.3 Page 159 L24)**
Comment #127, Clause **145.3.8.6 Page 198 L24)**

Comment #126, Clause 145.2.8.3 Page 159 L24

This comment addresses the following text:

[editing marks show missing text that will be addressed in the proposed remedy]
Part 1 of the text:
" A PSE shall maintain an output voltage no less than KTran_lo below VPort_PSE-2P min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 145.2.8.8.

Part 2 of the text:
Transients less than 30 µs in duration may cause the voltage at the PSE PI to fall more than KTran_lo.

Part 3 of the text:
The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145–28, allows a PD to operate for input voltage transients which cause VPD to drop as ***low as 0 V***, lasting less than 30 µs as specified ***in 145.3.8.6.***

Part 4 of the text:
Transients lasting more than 250 µs shall meet the VPort_PSE-2P specification. "

The commenter says:
"The following sentence does not make sense. In reality, the PSE cannot really short the PI voltage, all it can do is temporarily turn off its port (it's only a low side switch after all, with a 0.1uF cap).

Yair Response:
This is incorrect interpretation however needs some modifications.
Analysis:

A) The text doesn't say that that the voltage at the PD PI goes to zero because of active action of the PSE i.e. PSE is shorting the port.

A1) In fact, Part 1 of the text requires PSE to maintain maximum 7.6% voltage drop during transients lasting from 30usec to 250us.

A2) Part 2 of the text says the transient lasting less that 30usec may cause the voltage at the PSE PI to fall more than KTran_lo which means it can go down to zero or below zero. Down to zero is possible and it covered by the spec by part 2 of the text. **DO WE WANT TO ALLOW BELOW ZERO? I DON'T BELIVE SO.**

A3) It is possible that PSE may generate positive transient e.g. changing power supplies that will cause negative transient for less that 30us that goes down to ZERO at the PD PI due to the passive components at the channel and PD input circuitry (e.g. EMI filter) and this a typical case.

A4) It is possible that during voltage drop at the PSE from the same reasons of changing power supplies at the PSE the voltage will drop by 7.6% but will cause at the PD PI larger voltage drop down to zero.

A5) In all those cases when there is no voltage at the PD PI for 30usec, i.e. the voltage drop to zero at the PD PI will cause the voltage drop at Cport (which is now the power source for the PD) to be less than 7.6% so PD can handle this easily.

B) The minimum total PSE and PD capacitance is at least 5uF and not 0.1uF.

Summary for the PSE section:

- Part 1 of the text limits PSE voltage drop to not more that 7.6% from 30usec to 259usec transient duration. THIS IS GOOD.
- Part 2 of the text allows Voltage drop at the PSE PI to go to zero (THIS IS POSSIBLE HENCE IT IS GOOD) and be negative (THIS IS BAD. IT MAY CAUSE DAMAGE TO PDs).

Conclusions:
Add text to limit the PSE Transient lowest voltage at the PSE PI to be above zero or not less zero. The current text addresses the PD in this regard but not the PSE.

Suggested Remedy

Option A:

Make the following changes:

Not part of the baseline
The added text in the PSE section meant to not allow PSE to change polarity during the 30usec transient duration and informatively, does it for the PD PI.

" A PSE shall maintain an output voltage no less than KTran_lo below VPort_PSE-2P min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 145.2.8.8.

Transients less than 30 µs in duration may cause the voltage at the PSE PI to fall more than KTran_lo and shall not cause the voltage at the PSE PI to change polarity.
The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145–28, allows a PD to operate for input voltage transients which cause VPD to drop as low as 0 V, lasting less than 30 µs as specified in 145.3.8.6.
Transients lasting more than 250 µs shall meet the VPort_PSE-2P specification. "

Option B:

Make the following changes:

Not part of the baseline
Delete the part that describes the PD behavior at zero voltage. It belongs to the PD section. *See comment #127 that addresses similar issues in the PD section*

" A PSE shall maintain an output voltage no less than KTran_lo below VPort_PSE-2P min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 145.2.8.8.

Transients less than 30 µs in duration may cause the voltage at the PSE PI to fall more than KTran_lo and shall not cause the voltage at the PSE PI to change polarity.
The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145–28, allows a PD to operate for input voltage transients which cause VPD to drop ~~below~~ more than KTran_lo below VPort_PD-2P min~~as low as 0 V~~, lasting less than 30 µs as specified in 145.3.8.6.
Transients lasting more than 250 µs shall meet the VPort_PSE-2P specification. "

Comment #127, Clause 145.3.8.6 Page 198 L24)

This comment addresses the following text:

"A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 145.2.8.3."

The commenter says:

(1) This sentence does not make sense, since it refers to a transient to 0V at the PI. In reality, the PSE cannot really short the PI voltage, all it can do is temporarily turn off its port (it's only a low side switch after all, with a 0.1uF cap).

Yair Response: As explained in comment #126:

- PSE transients have hard limit between 30usec to 250usec which is a voltage drop not higher than 7.6% so at the PSE PI it never drops to zero.
- PSE transients below 30usec, has no limits as for how down they can go. See Part 2 of the text in comment #126: "Transients less than 30 µs in duration may cause the voltage at the PSE PI to fall more than KTran_lo."
- Voltage may drop to zero and negative values do to passive components exposed to PSE transients and not only when PSE short the port.
- This text only says that "A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 145.2.8.3.".
- The capacitance is 5uF min and not 0.1uF. This is what the PSE sees during POWER_ON state.

(2) Also, if the voltage at the PI goes down to 0V or not, at PSE PI, is purely dependent on the PD configuration (load current, type of input bridge, etc.), and should not be part of the requirement.

Yair Response:

- This statement is not accurate. DO WE WANT TO ALLOW?
  - The PSE voltage polarity as a result of transient could be negative?
  - Laboratory voltage source that quickly changes its voltage polarity (which is not compliant PSE that works only at single polarity after IDLE state) connected to PD that cause quick polarity changes at the PD input voltage to check PD compliance of mode A and mode B at either polarity? This may cause damage to ideal diode bridges and force unnecessary cost burden due to use case that doesn't exists when compliant PSE is used.

See detailed analysis in comment #126.

Suggested Remedy

Make the following changes:

Not part of the baseline
1. *We do need the part "* as defined in 145.2.8.3" in the current text since 145.2.8.3 put limits to PSE voltage behavior during transients and we have to add the reference to it like any other part in the spec. 2. *In addition, we need to add text that PD will meets its transient spec when connected to compliant PSE*

"A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 145.2.8.3 when connected to a voltage source that meets the PSE requirements of this standard."