33.3.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 33–16.

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

33.3.3.2 Constants

The PD state diagram uses the following constants:

V_{Reset_th}
> Reset voltage threshold (see Table 33–17)

V_{Mark_th}
> Mark event voltage threshold (see Table 33–17)

class_sig
> PD classification, one of either 0, 1, 2, 3, or 4 (see Table 33–16)

33.3.3.3 Variables

The PD state diagram uses the following variables:

mdi_power_required
> A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:
>
> FALSE: PD functionality is disabled.
> TRUE: PD functionality is enabled.

pd_ ~~2~~multi-event
> A control variable indicating whether the PD presents a ~~2~~Mulitple-Event class signature.
>
> Values: FALSE: PD does not present a ~~2~~Multiple-Event class signature.
>   TRUE: PD does present a Mulitple~~2~~-Event class signature.

pd_dll_capable
> This variable indicates whether the PD implements Data Link Layer classification.
>
> Values: FALSE: The PD does not implement Data Link Layer classification.
>   TRUE: The PD does implement Data Link Layer classification.

pd_dll_enabled
> A variable indicating whether the Data Link Layer classification mechanism is enabled.
>
> Values: FALSE: Data Link Layer classification is not enabled.
>   TRUE: Data Link Layer classification is enabled.

pd_max_power
> A control variable indicating the max power that the PD may draw from the PSE. See power classifications in Table 33–18.
>
> Values: 0:   PD may draw Class 0 power
>   1:   PD may draw Class 1 power
>   2:   PD may draw Class 2 power
>   3:   PD may draw Class 3 power
>   4:   PD may draw Class 4 power
>   5:   PD may draw Class 5 power
>   6:   PD may draw Class 6 power
>   7:   PD may draw Class 7 power

pd_reset

An implementation-specific control variable that unconditionally resets the PD state diagram to the OFFLINE state.

Values: FALSE: The device has not been reset (default).

TRUE: The device has been reset.

power_received

An indication from the circuitry that power is present on the PD's PI.

Values: FALSE: The input voltage does not meet the requirements of V_{Port_PD} in Table 33–18.

TRUE: The input voltage meets the requirements of V_{Port_PD}.

present_class_sig

Controls presenting the classification signature (see 33.3.5) by the PD.

Values: FALSE: The PD classification signature is not to be applied to the link.

TRUE: The PD classification signature is to be applied to the link.

present_det_sig

Controls presenting the detection signature (see 33.3.4) by the PD.

Values: FALSE: A non-valid PD detection signature is to be applied to the link.

TRUE: A valid PD detection signature is to be applied to the link.

present_mark_sig

Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD.

Values: FALSE: The PD does not present mark event behavior.

TRUE: The PD does present mark event behavior.

present_mps

Controls applying MPS (see 33.3.8) to the PD's PI.

Values: FALSE: The Maintain Power Signature (MPS) is not to be applied to the PD's PI.

TRUE: The MPS is to be applied to the PD's PI.

pse_dll_power_leveltype

A control variable output by the PD power control state diagram (Figure 33–28) that indicates the type of PSE by which the PD is being powered.

Values: 1: The PSE is a Type 1 PSE (default).

2: The PSE is a Type 2 PSE.

3: The PSE is a Type 3 PSE.

4: The PSE is a Type 4 PSE.

pse_power_type

A control variable that indicates to the PD the type of PSE by which it is being powered.Values: 1: The PSE is a Type 1 PSE.

2: The PSE is a Type 2 PSE.

pse_power_level

A control variable that indicates to the PD the level of power the PSE is supplying.

Values: 1: The PSE is delivering the PD's requested power or 15.4W, whichever is less.

2: The PSE is delivering the PD's requested power or 30W, whichever is less.

3: The PSE is delivering the PD's requested power or 60W, whichever is less.

4: The PSE is delivering the PD's requested power or 90W (TBD), whichever is less.

V_{PD}

Voltage at the PD PI as defined in 1.4.

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer

A timer used to prevent the Type 2 PD from drawing more than inrush current during the PSE's inrush period; see T_{delay} in Table 33–18.

33.3.3.5 Functions

do_class_timing

This function is used by a Type 3 or Type 4 PD to evaluate the type of PSE connected to the link by measuring the length of the classification event. The classification event timing requirements are defined in Table 33-10. This function returns the following variable:

Type_3_MPS: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8). the PD should use.
Values: TRUE: The PSE uses Type 3 MPS requirements.
           FALSE: The PSE uses Type 1 MPS requirements.
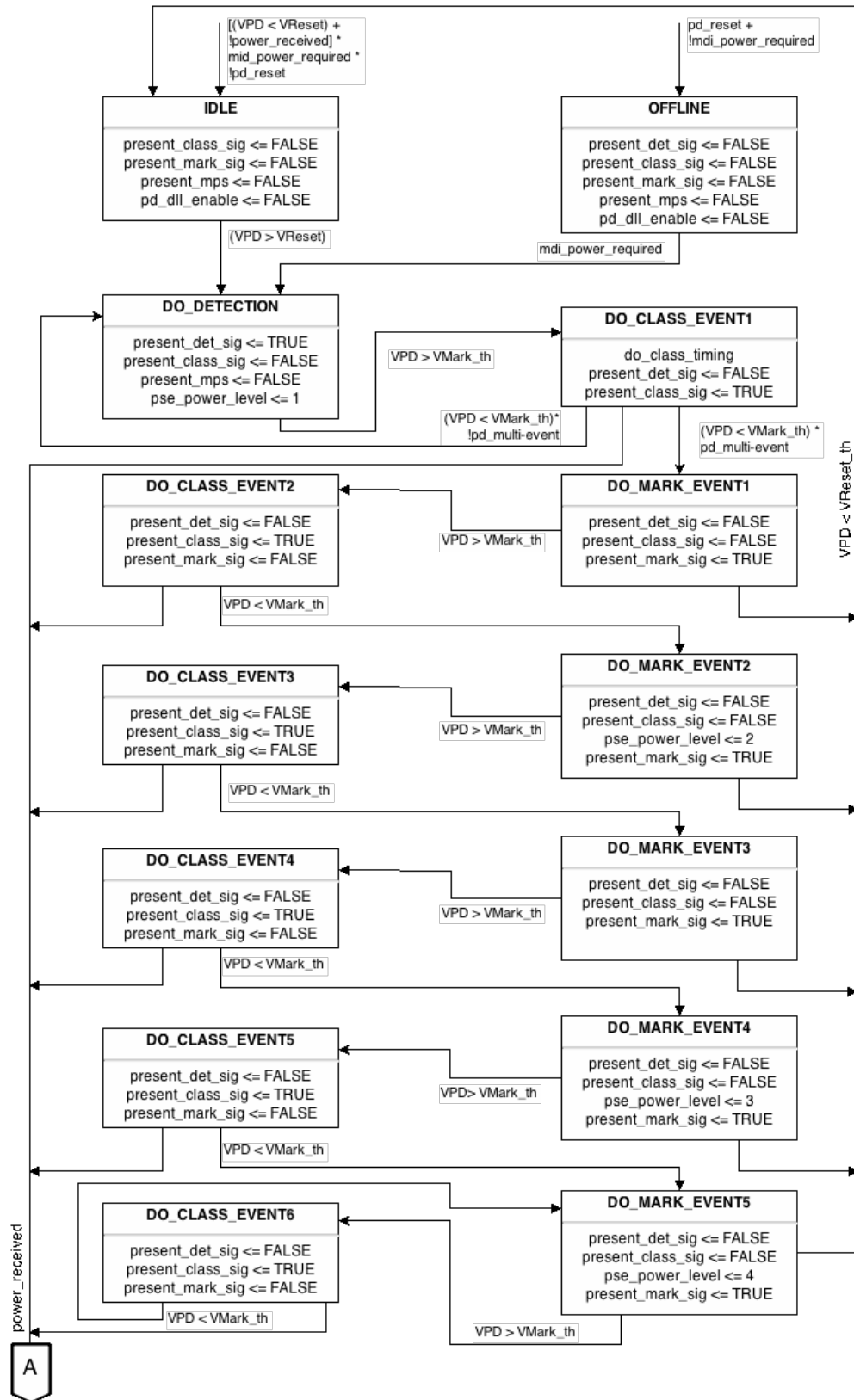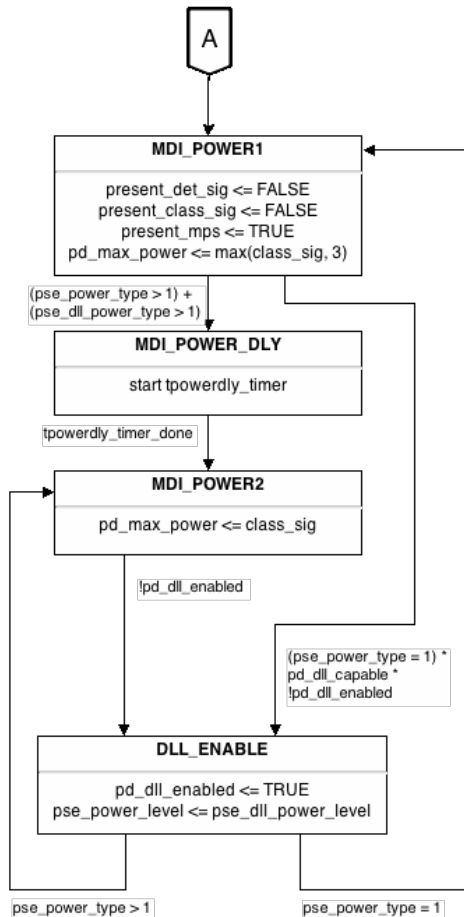
33.3.3.65 State diagrams

Figure 33–16—PD state diagram

Figure 33–16—PD state diagram *(continued)*

NOTE 1—DO_CLASS_EVENT~~36~~ creates a defined behavior for a Type 2, Type 3, or Type 4 PD that is brought into the classification range repeatedly.

NOTE 2—In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than T_{class}.

33.3.5 PD classifications

See 33.2.6 for a general description of classification mechanisms.

A PD may be classified by the PSE based on the Physical Layer classification information, Data Link Layer classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used to establish mutual identification between Type 2, Type 3, and Type 4 PSEs and Type 2, Type3, and Type 4 PDs.

The method of classification depends on the type of the PD and the type of the attached PSE. A PD

shall meet at least one of the allowable classification permutations listed in Table 33–8. A Type 1

PD may implement any of the class signatures in 33.3.5 and 33.6.

Type 2, Type 3, and Type 4 PDs implement both ~~2~~Multiple-Event class signature (see 33.3.5.2) and Data Link

Layer classification (see33.6).

PD classification behavior conforms to the state diagram in Figure 33–16.

33.3.5.1 PD 1-Event class signature

Class 0 is the default for PDs. However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3.

The PD is classified based on power. The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes.

PDs implementing a Mulitple2-Event class signature shall return Class 4 in accordance with the maximum power draw, P_{Class_PD}, as specified in Table 33–18. Since 1-Event classification is a subset of 2Multiple-Event classification, Type 2, Type 3, and Type 4 PDs respond to 1-Event classification with a Class 4 signature. Type 1 PDs may choose to implement a Multiple2-Event class signature and return Class 0, 1, 2, or 3 in accordance with the maximum power draw, P_{Class_PD}. The Type 2, Type 3, and Type 4 PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–16. AType 1 and Type 2 PDs shall present one, and only one, classification signature during classification.

Table 33–16—Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4.00	mA
Current for Class 1	14.5 V to 20.5 V	9.00	12.0	mA
Current for Class 2	14.5 V to 20.5 V	17.0	20.0	mA
Current for Class 3	14.5 V to 20.5 V	26.0	30.0	mA
Current for Class 4	14.5 V to 20.5 V	36.0	44.0	mA

33.3.5.2 PD 2Multiple-Event class signature

PDs implementing Multiple-Event Physical Layer classification shall present one of the series of classification signatures shown in Table 33-TBD. If the number of class events is greater than 5, The PD shall present the same signature it presented during the 5th finger. PDs implementing a 2-Event class signature shall return a Class 4 classification signature in accordance with the maximum power draw, P_{Class_PD}, as specified by Table 33-18. The PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

Table 33–TBDA1—Allowed classification responses to a series of class events

PD Type	Class	Signature during Class Event*				
		CLASS_EV1	CLASS_EV2	CLASS_EV3	CLASS_EV4	CLASS_EV5
1	0	0	0	0	0	0
	1	1	1	1	1	1
	2	2	2	2	2	2
	3	3	3	3	3	3
2	4	4	4	4	4	4
3	1	1	1	1	1	1
	2	2	2	2	2	2
	3	3	3	3	3	3
	4	4	4	4	4	4
	5	4	4	1	1	1
	6	4	4	2	2	2
4	7	4	4	3	3	3

*NOTE: See Table 33-16 for definitions of class signatures 1-4.

Until successful 2Multipile-Event Physical Layer classification or Data Link Layer classification has completed, a Type 2, Type 3, or Type 4 PD's pse_power_leveltype state variable is set to '1.' A Type 2, Type 3, or Type 4 PD shall conform to the electrical requirements as defined by Table 33–18 for the leveltype defined in its pse_power_leveltype state variable.

Table 33–17—Multiple2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class}	V	14.5	20.5	
2	Mark event voltage	V_{Mark}	V	6.90	10.1	
3	Mark event current	I_{Mark}	mA	0.250	4.00	See 33.3.5.2.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 33.3.5.2.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.90	See 33.3.5.2.1
6	Classification reset voltage	V_{Reset}	V	0	2.81	See 33.3.5.2.1

33.3.5.2.1 Mark Event behavior

When the PD is presenting a mark event signature as shown in the state diagram of Figure 33–16, the PD shall draw I_{Mark} as defined in Table 33–17 and present a non-valid detection signature as defined in Table 33–15.

The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark} specification as defined in Table 33–17.

V_{Mark_th} is the PI voltage threshold at which the PD implementing 2Multiple-Event class signature transitions into and out of the DO_CLASS_EVENT1 or DO_CLASS_EVENT2, DO_CLASS_EVENT3, DO_CLASS_EVENT4, or DO_CLASS_EVENT5 states as shown in Figure 33–16.

The PD shall draw I_{Mark} until the PD transitions from a DO_MARK_EVENT state to the IDLE state. V_{Reset_th} is the PI voltage threshold at which the PD implementing 2Multiple-Event class signature transitions from a DO_MARK_EVENT state to the IDLE state as shown in Figure 33–16.

33.3.6 PSE Type identification

A Type 2 PD shall identify the PSE Type as either Type 1 or Type 2 (see Figure 33–16). A Type 3 PD shall identify the PSE Type as either Type 1, Type 2, or Type 3. A Type 4 PD shall identify the PSE Type as either Type 1, Type 2, Type 3, or Type 4.

The default value of pse_power_leveltype is 1. After a successful 2Multiple-Event Physical Layer classification or DataLink Layer classification has completed, the pse_power_leveltype is set to either 2, 3 or 4.

The PD resets the pse_power_leveltype to '1' when the PD enters the DO_DETECTION state.

33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage	V_{Port_PD}	V	37.0	57.0	1	See 33.3.7.1, Table 33–1
				42.5	57.0	2	
2	Transient operating input voltage	V_{Tran_lo}	V	36.0		2	For time duration defined in 33.2.7.2
3	Input voltage range during overload	$V_{Overload}$	V	36.0	57.0	1	See 33.3.7.4, Table 33–1
				41.4	57.0	2	
4	Input average power, Class 0 and Class 3	P_{Class_PD}	W		13.0	1, 3	See 33.3.7.2, Table 33–1
	Input average power, Class 1				3.84	1, 3	
	Input average power, Class 2				6.49	1, 3	
	Input average power, Class 4				25.5	2, 3	
	Input average power, Class 5				TBD	3	
	Input average power, Class 6				TBD	3	
	Input average power, Class 7				TBD	4	
5	Input inrush current	I_{Inrush_PD}	A		0.400	1, 2	Peak value— See 33.3.7.3
6	Inrush to operating state delay	T_{delay}	s	0.080		2	See 33.3.7.3
7	Peak operating power, Class 0 and Class 3	P_{Peak_PD}	W		14.4	1	See 33.3.7.4
	Peak operating power, Class 1				5.00	1	
	Peak operating power, Class 2				8.36	1	
	Peak operating power, Class 4				$1.11 \times P_{Class\_PD}$	2	
8	Input current transient (absolute value)		mA/µs		4.70	1, 2	See 33.3.7.5
9	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		1, 2	See 33.3.7.6, 33.3.7.3

Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
10	Ripple and noise, < 500 Hz		V_{PP}		0.500	1, 2	See 33.3.7.7. Balanced source impedance: R_{Ch}
	Ripple and noise, 500 Hz to 150 kHz				0.200		
	Ripple and noise, 150 kHz to 500 kHz				0.150		
	Ripple and noise, 500 kHz to 1 MHz				0.100		
11	a) PD Power supply turn on voltage	V_{On}	V		42.0	1, 2	See 33.3.7.1
	b) PD power supply turn off voltage	V_{Off}	V	30.0		1, 2	
12	PD classification stability time	T_{class}	s		0.005		See 33.3.7.8
13	Backfeed voltage	V_{bfd}	V		2.80		See 33.3.7.9