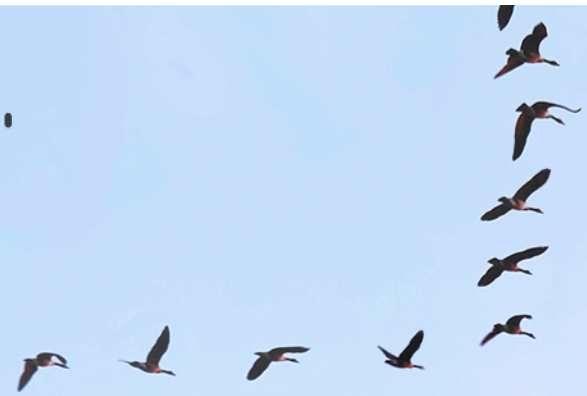

Type 3/Type 4 PSE State Diagram

With Proposed CC & Detection Sequencing & Timing Constraints

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Background

- Mechanism, sequencing, and timing of Connection Check (CC) are left to the reader in D1.2
- Intent has been to provide utmost implementation flexibility
- Increases the complexity of the PSE State Diagram (SD) and the standard in general, and may lead to poor implementations
- Goals:
  - Define enough aspects of CC that implementation flexibility and PSE SD complexity are optimally balanced
  - Motion in Type 3/Type 4 PSE SD for review during D1.3 comment cycle

CC & Detection Sequencing

- Propose to restrict the number of permitted sequences for CC and Detection to **3**

  1) CC → Detection

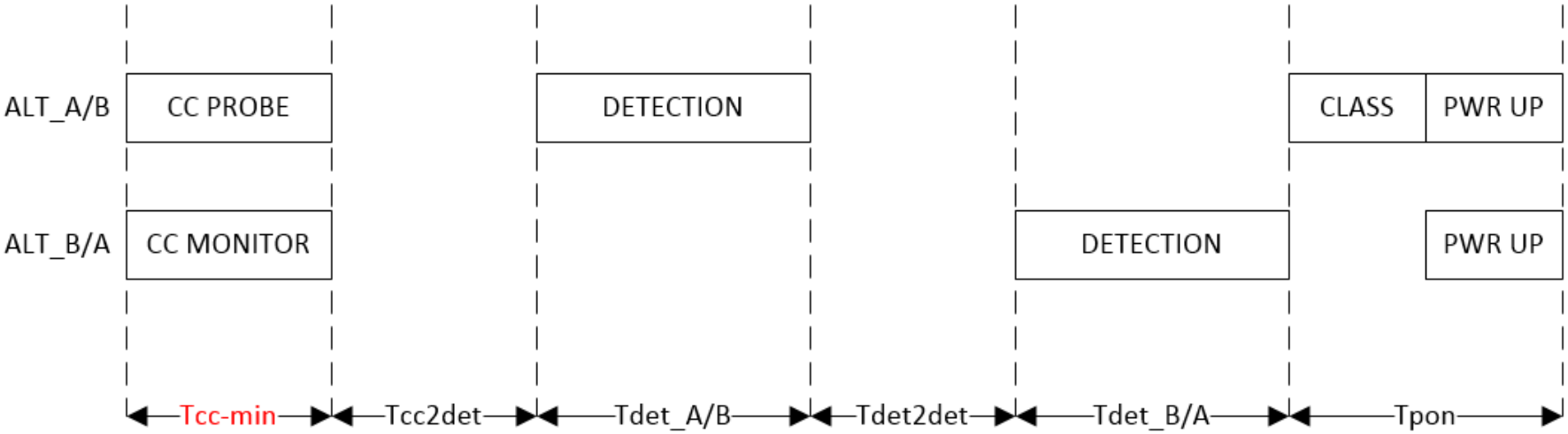
  2) Detection ALT_A/B → CC → Detection ALT_B/A

  3) Simultaneous CC & Detection

❖ Provides several implementation options while reining in PSE SD complexity

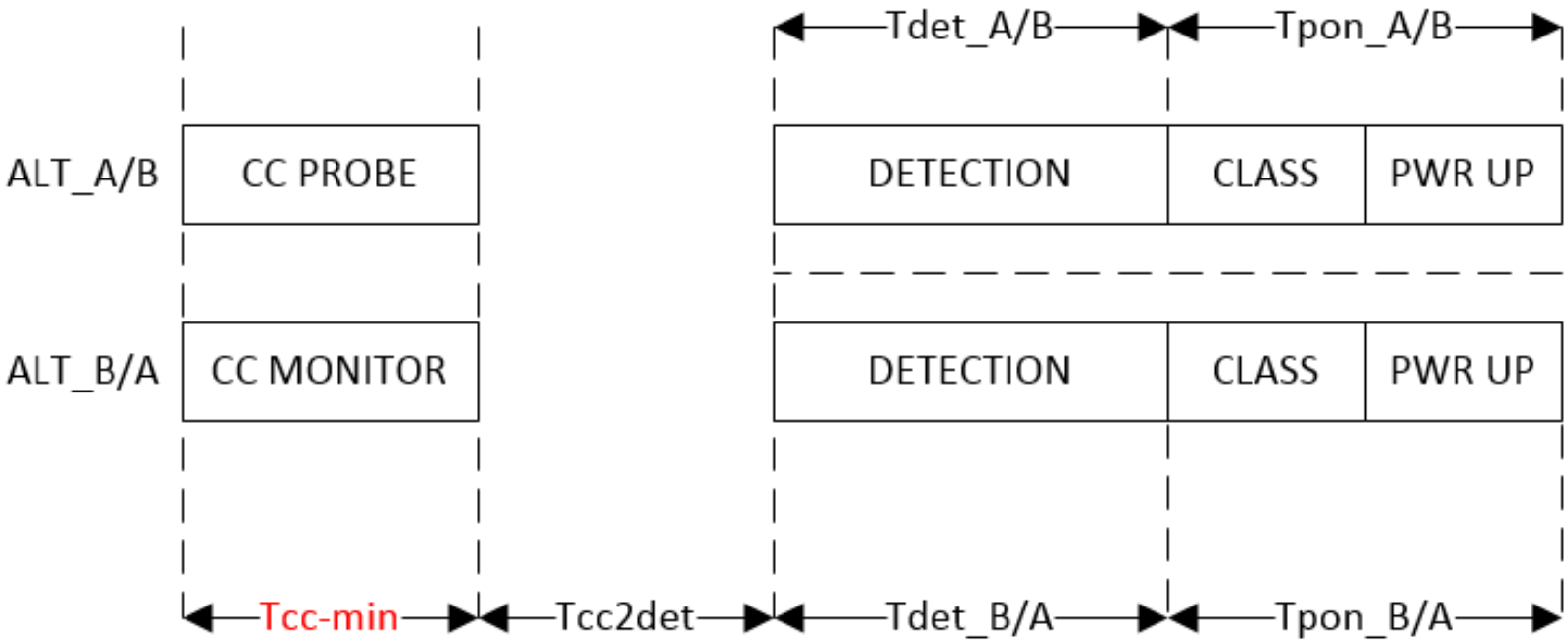
Sequence 1:
CC → Detection

CC → DET (SS PD)

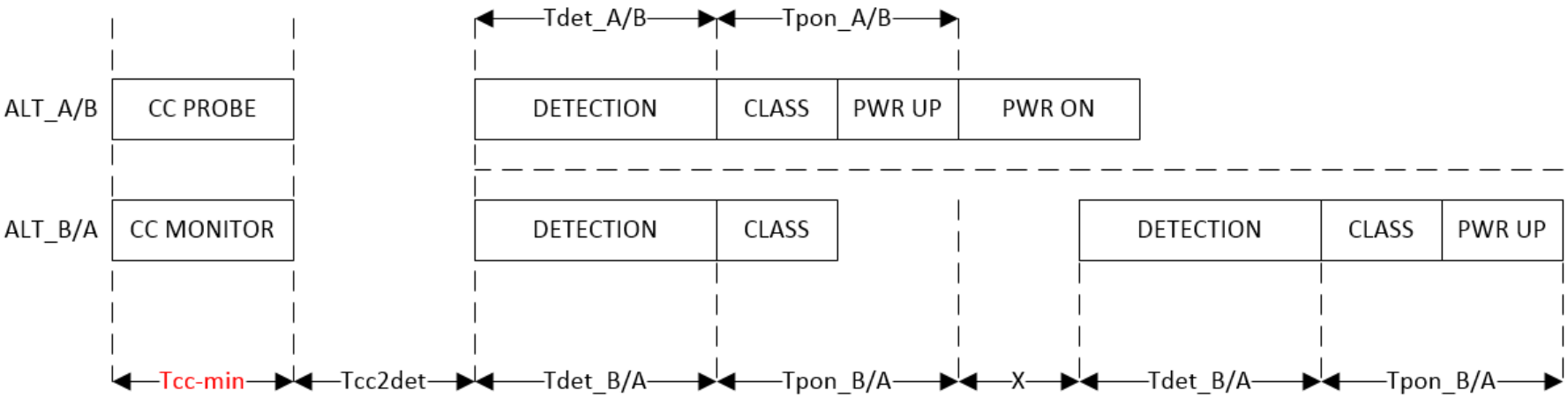


- Tcc-min (>200ms) to circumvent cable-plug issue
- Sequence remains viable and most of the implementation details are left to the reader

CC → DET (Type 3/Type 4 DS PD)

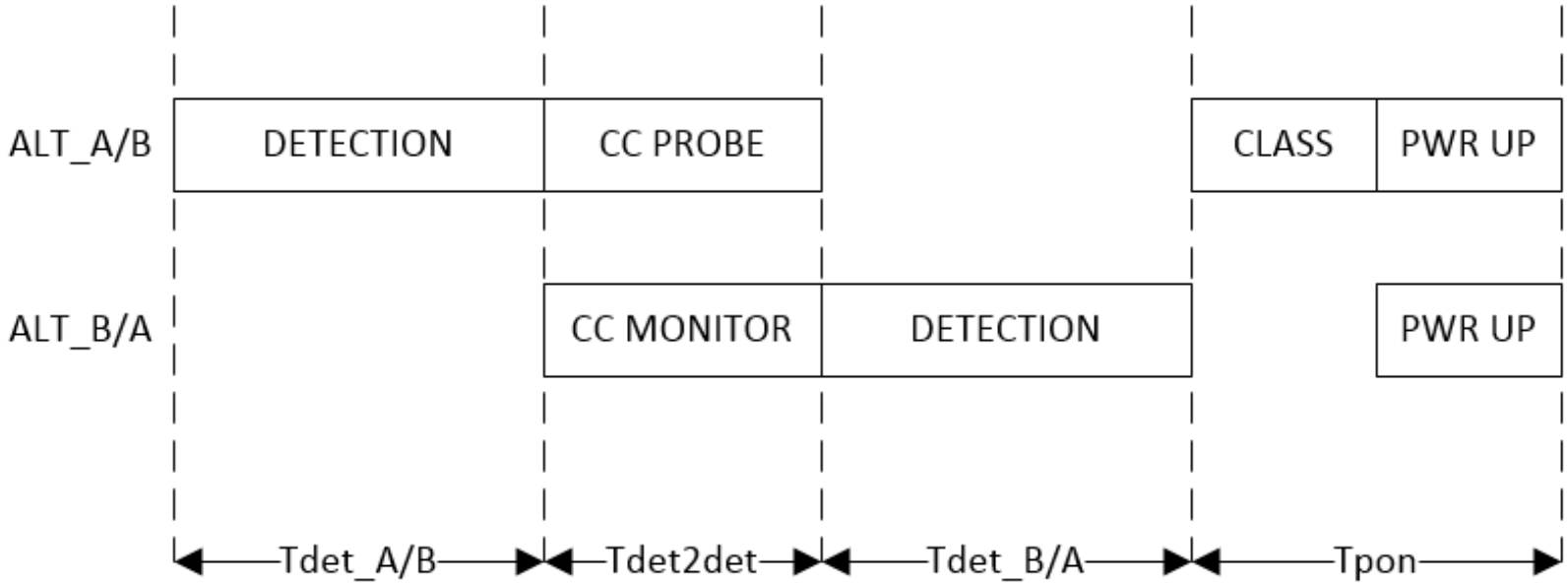


CC → DET (Type 1/Type 2 DS PD)



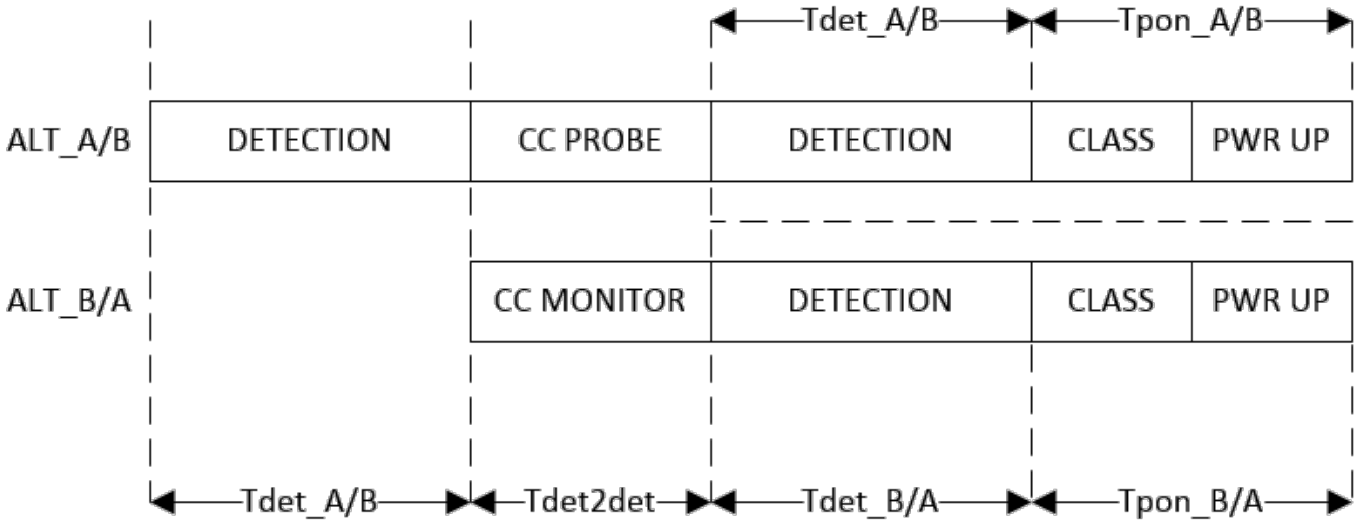
Sequence 2:
Detection ALT_A/B → CC → Detection ALT_B/A

DET → CC → DET (SS PD)



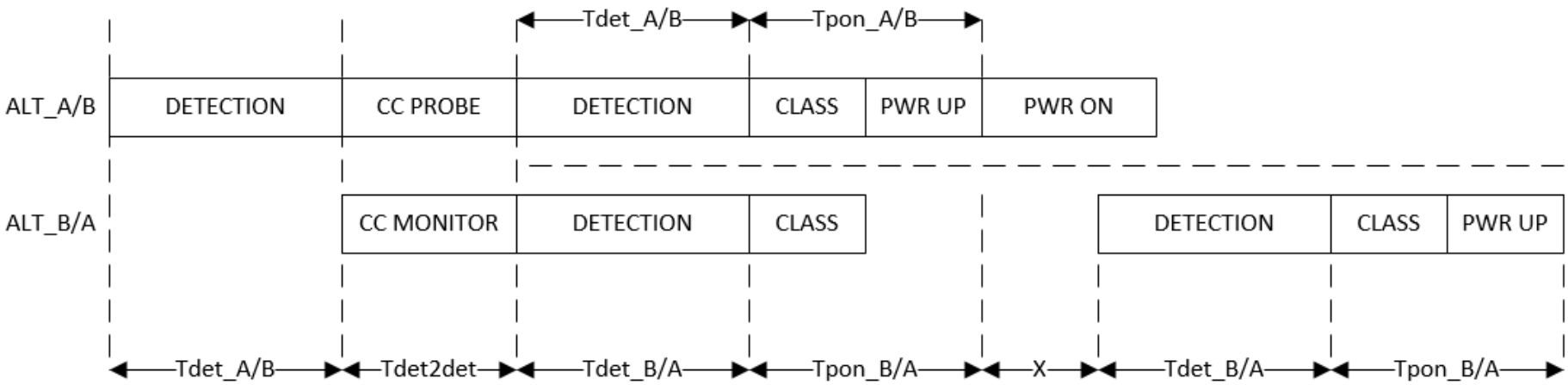
- CC timing is more stringent than for Sequence 1, but still perfectly viable

DET → CC → DET (Type 3/Type 4 DS PD)



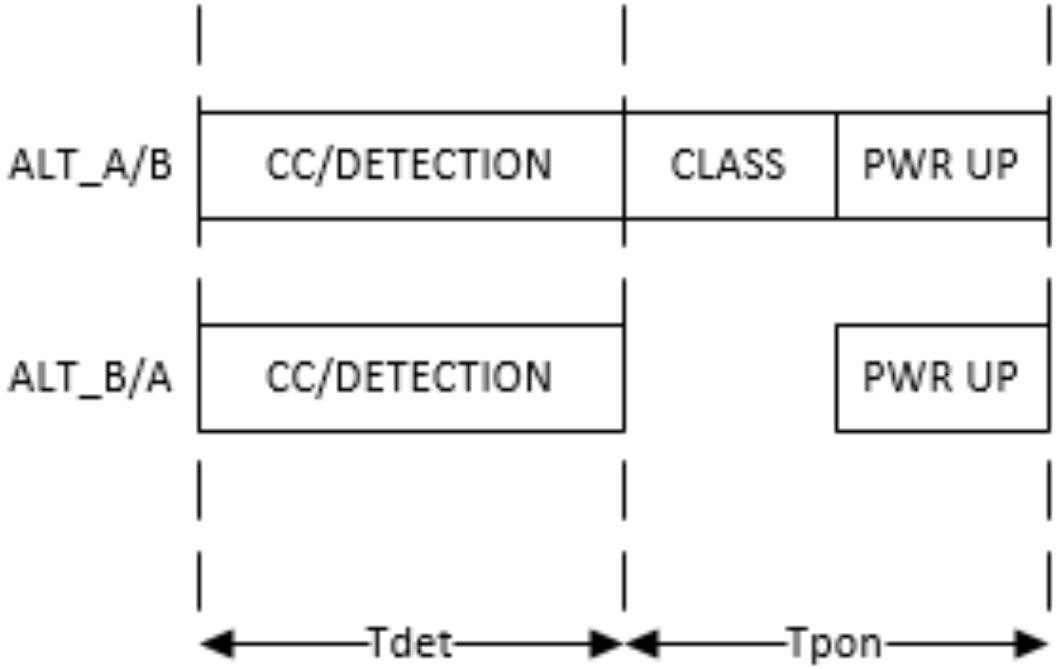
- D1.2 states that Tdet2det "Applies only when connected to a single-signature PD (TBD)."
- Tdet2det always applies for DS PDs with this sequence

DET → CC → DET (Type 1/Type 2 DS PD)

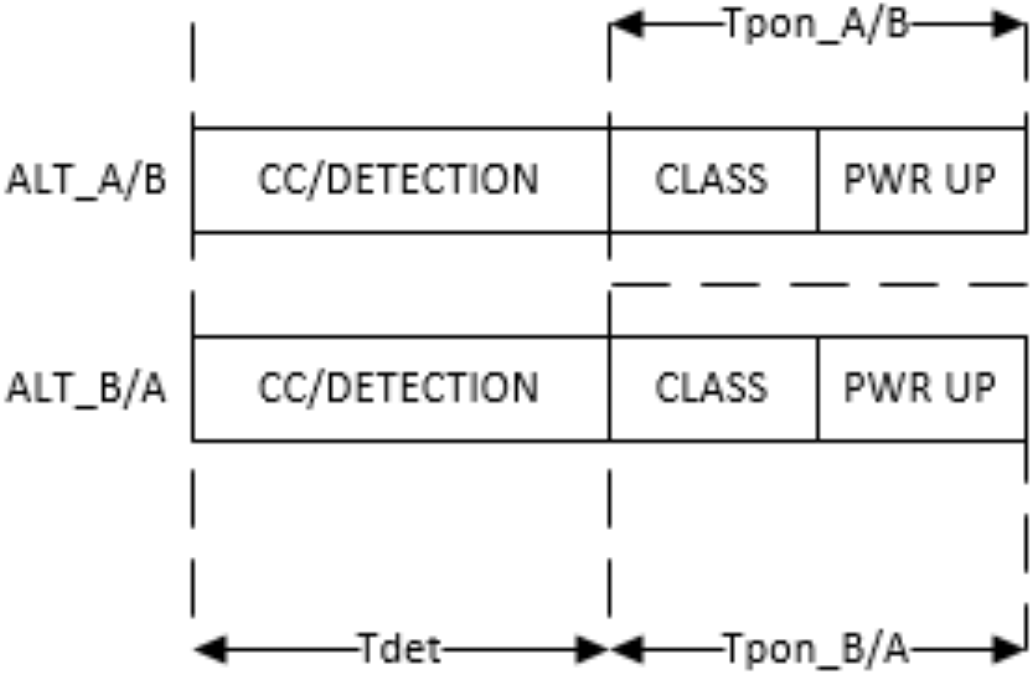


Sequence 3:
Simultaneous CC & Detection

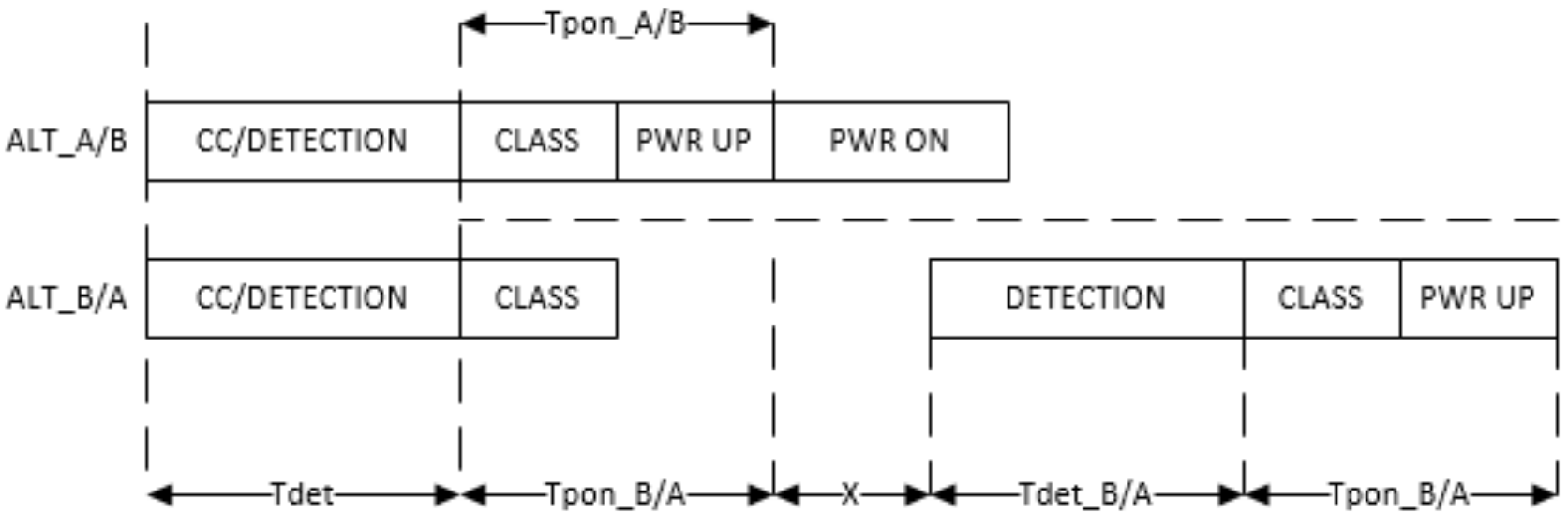
Simul. CC & DET (SS PD)



Simul. CC & DET (Type 3/Type 4 DS PD)



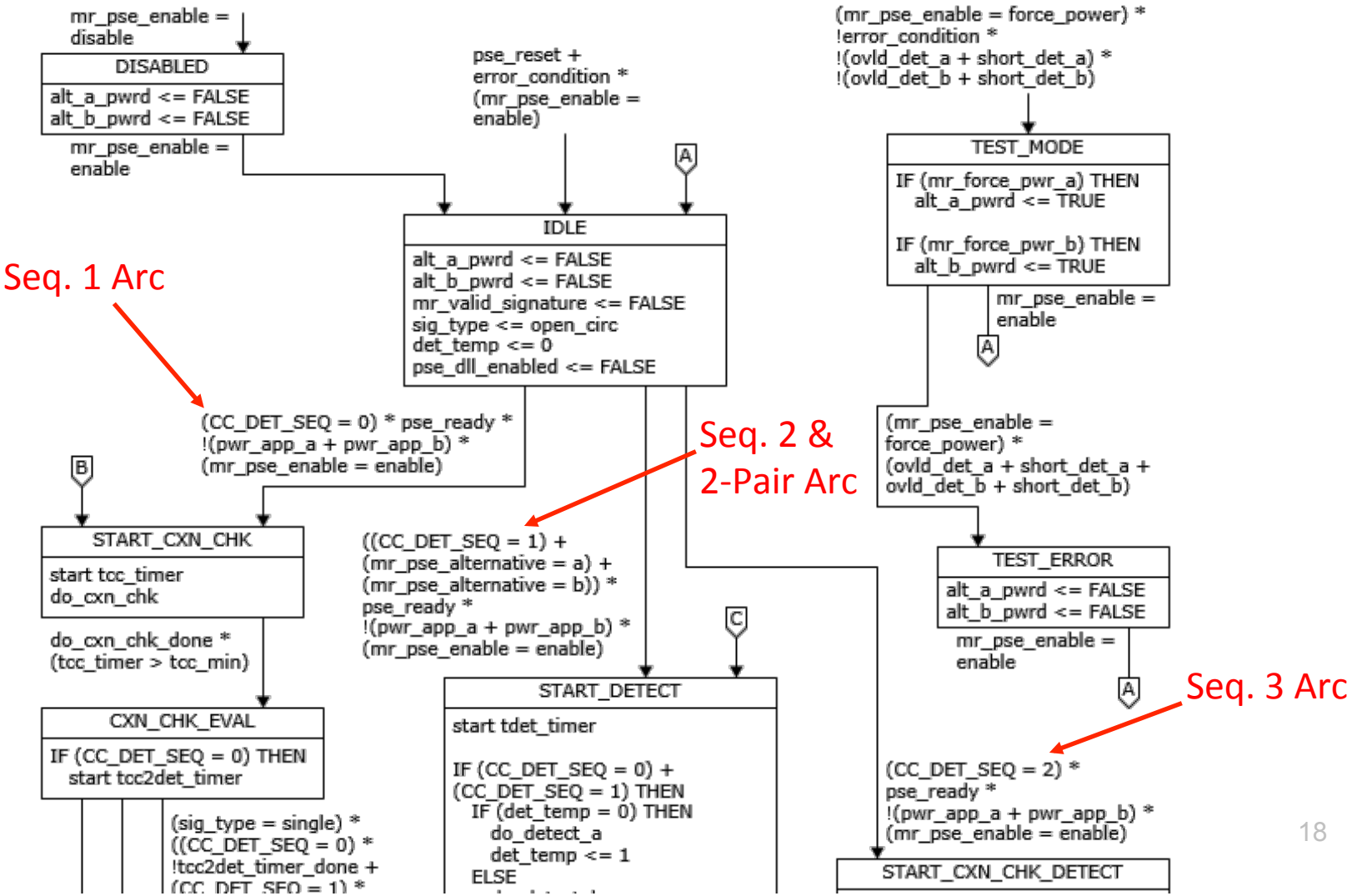
Simul. CC & DET (Type 1/Type 2 DS PD)



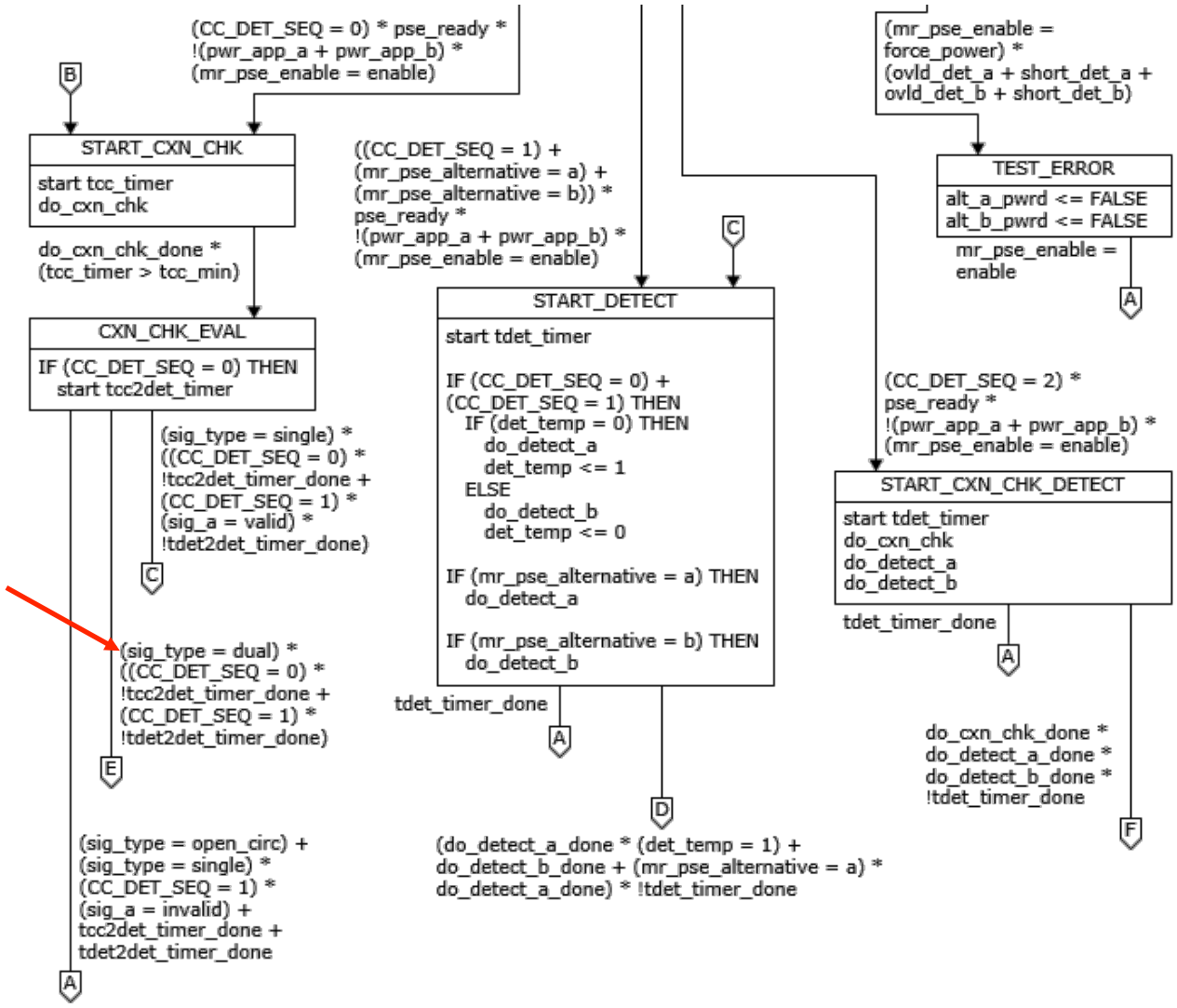
Type 3/Type 4 PSE SD:
Vision & Some Key Points

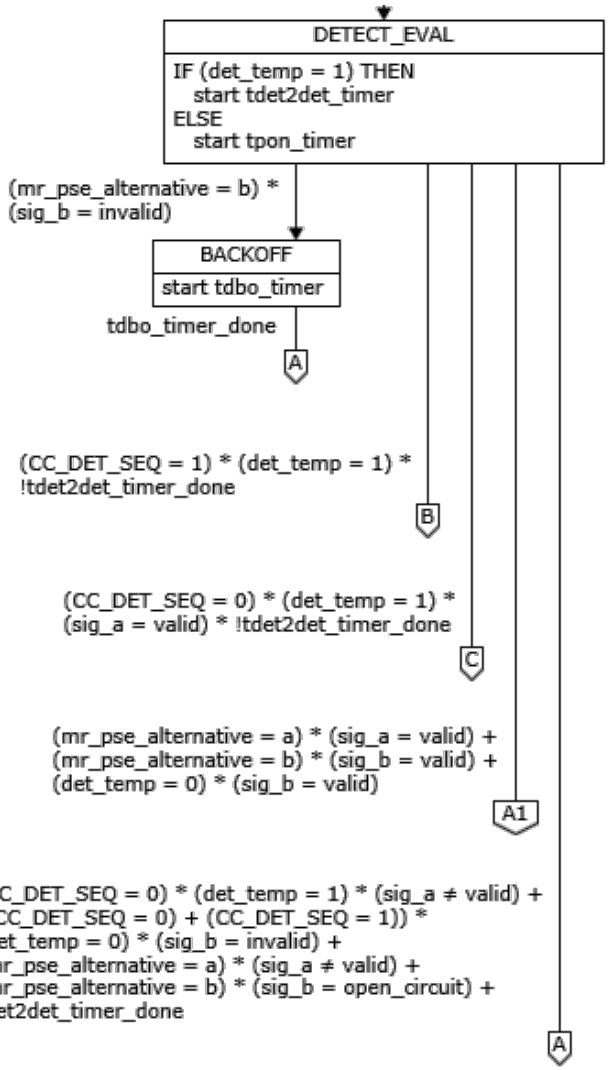
Approach

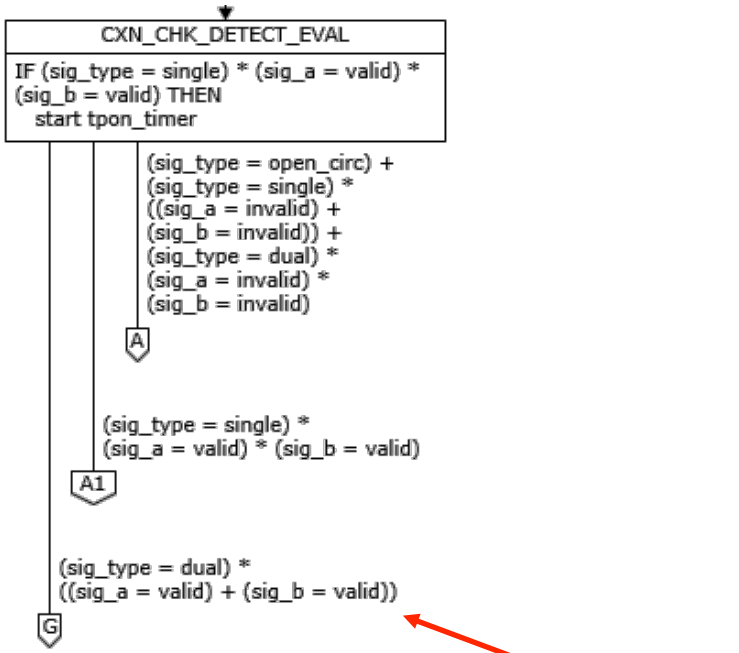
- Keep Type 3/Type 4 PSE SD distinct from existing Type 1/Type 2 SD
  - Ensures that current SD format and functionality are retained
  - Allows for a higher degree of optimization to the new SD
- Create a flat (non-hierarchical) SD
- Support all sequences detailed in this presentation
- Generate new text that defines the states, functions, timers, variables, and constants used


mr_pse_enable = disable
DISABLED
alt_a_pwrd <= FALSE
alt_b_pwrd <= FALSE
mr_pse_enable = enable
pse_reset + error_condition * (mr_pse_enable = enable)
A
IDLE
alt_a_pwrd <= FALSE
alt_b_pwrd <= FALSE
mr_valid_signature <= FALSE
sig_type <= open_circ
det_temp <= 0
pse_dll_enabled <= FALSE
(mr_pse_enable = force_power) * !error_condition * !(ovld_det_a + short_det_a) * !(ovld_det_b + short_det_b)
TEST_MODE
IF (mr_force_pwr_a) THEN alt_a_pwrd <= TRUE
IF (mr_force_pwr_b) THEN alt_b_pwrd <= TRUE
mr_pse_enable = enable
A
Seq. 1 Arc
(CC_DET_SEQ = 0) * pse_ready * !(pwr_app_a + pwr_app_b) * (mr_pse_enable = enable)
B
START_CXN_CHK
start tcc_timer
do_cxn_chk
do_cxn_chk_done * (tcc_timer > tcc_min)
CXN_CHK_EVAL
IF (CC_DET_SEQ = 0) THEN start tcc2det_timer
(sig_type = single) * ((CC_DET_SEQ = 0) * !tcc2det_timer_done +
Seq. 2 & 2-Pair Arc
((CC_DET_SEQ = 1) + (mr_pse_alternative = a) + (mr_pse_alternative = b)) * pse_ready * !(pwr_app_a + pwr_app_b) * (mr_pse_enable = enable)
C
START_DETECT
start tdet_timer
IF (CC_DET_SEQ = 0) + (CC_DET_SEQ = 1) THEN
IF (det_temp = 0) THEN
do_detect_a
det_temp <= 1
ELSE
(mr_pse_enable = force_power) * ovld_det_a + short_det_a + ovld_det_b + short_det_b)
TEST_ERROR
alt_a_pwrd <= FALSE
alt_b_pwrd <= FALSE
mr_pse_enable = enable
A
Seq. 3 Arc
(CC_DET_SEQ = 2) * pse_ready * !(pwr_app_a + pwr_app_b) * (mr_pse_enable = enable)
START_CXN_CHK_DETECT

ALT coordination for 4-pair operation maintained until DS confirmed here



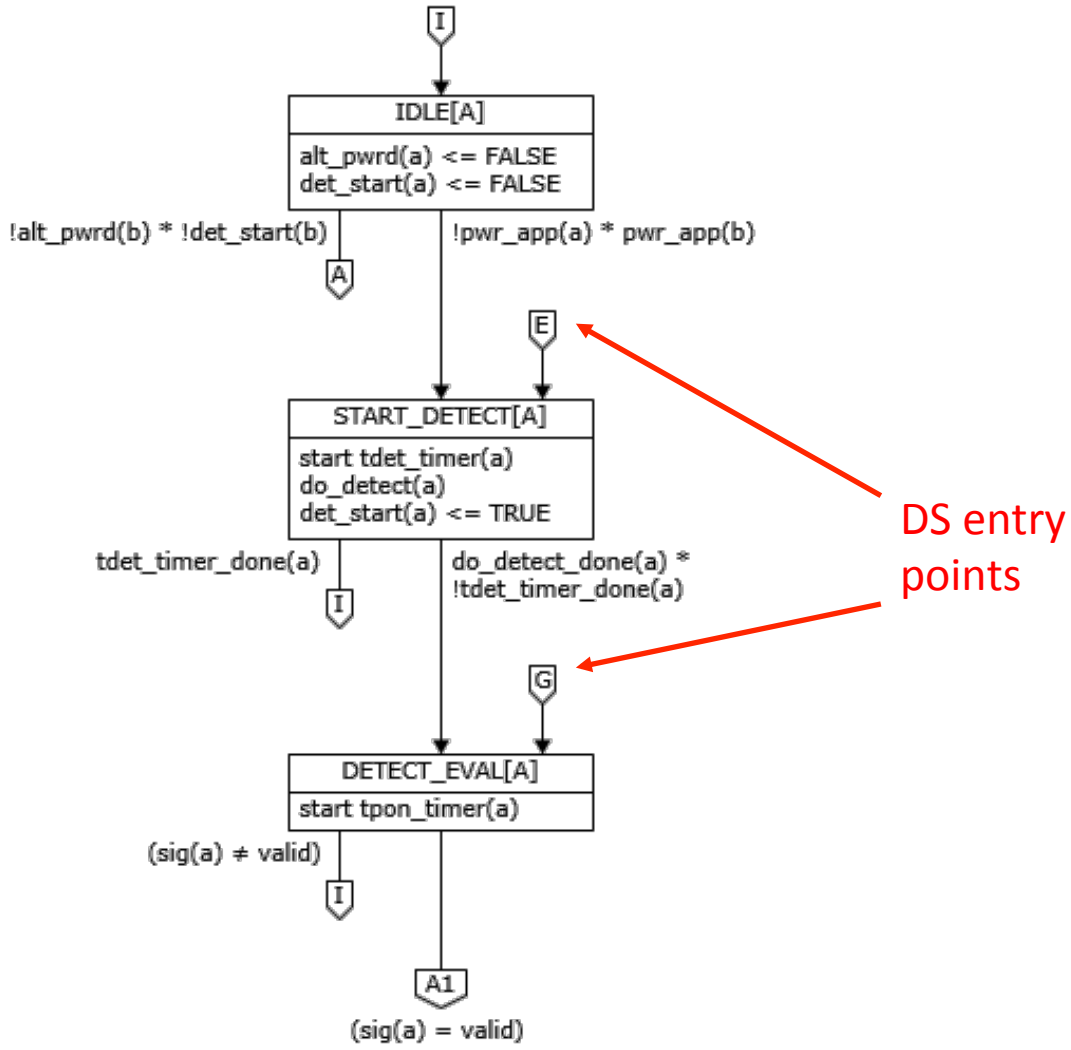

DETECT_EVAL
IF (det_temp = 1) THEN
start tdet2det_timer
ELSE
start tpon_timer
(mr_pse_alternative = b) *
(sig_b = invalid)
BACKOFF
start tdbo_timer
tdbo_timer_done
A
(CC_DET_SEQ = 1) * (det_temp = 1) *
!tdet2det_timer_done
B
(CC_DET_SEQ = 0) * (det_temp = 1) *
(sig_a = valid) * !tdet2det_timer_done
C
(mr_pse_alternative = a) * (sig_a = valid) +
(mr_pse_alternative = b) * (sig_b = valid) +
(det_temp = 0) * (sig_b = valid)
A1
(CC_DET_SEQ = 0) * (det_temp = 1) * (sig_a ≠ valid) +
((CC_DET_SEQ = 0) + (CC_DET_SEQ = 1)) *
(det_temp = 0) * (sig_b = invalid) +
(mr_pse_alternative = a) * (sig_a ≠ valid) +
(mr_pse_alternative = b) * (sig_b = open_circuit) +
tdet2det_timer_done
A


CXN_CHK_DETECT_EVAL
IF (sig_type = single) * (sig_a = valid) *
(sig_b = valid) THEN
start tpon_timer
(sig_type = open_circ) +
(sig_type = single) *
((sig_a = invalid) +
(sig_b = invalid)) +
(sig_type = dual) *
(sig_a = invalid) *
(sig_b = invalid)
A
(sig_type = single) *
(sig_a = valid) * (sig_b = valid)
A1
(sig_type = dual) *
((sig_a = valid) + (sig_b = valid))
G

And here

DS pseudo-independency indicated by:

- [A] or [B] suffix in STATE NAMES
- (a) or (b) suffix for timers, functions, & variables



Type 3/Type 4 PSE SD:
Next Steps

Next Steps

- Modify Classification SD
  - Should describe Type 3/Type 4 behavior only
  - Should include mutual ID
  - Will connect to the PSE SD with unique off-page identifiers
- Incorporate Autoclass
- Continue to iterate per review feedback from the TF

References

References

- http://www.ieee802.org/3/bt/public/jul15/Walker_1_0715_rev_3.pdf
- http://www.ieee802.org/3/bt/public/jun15/abramson_01bt_0615.pdf
- http://www.ieee802.org/3/bt/public/sep14/dwelley_01_0914.pdf