Canova Tech

The Art of Silicon Sculpting

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IEEE 802.3cg

PLCA Burst mode fixes

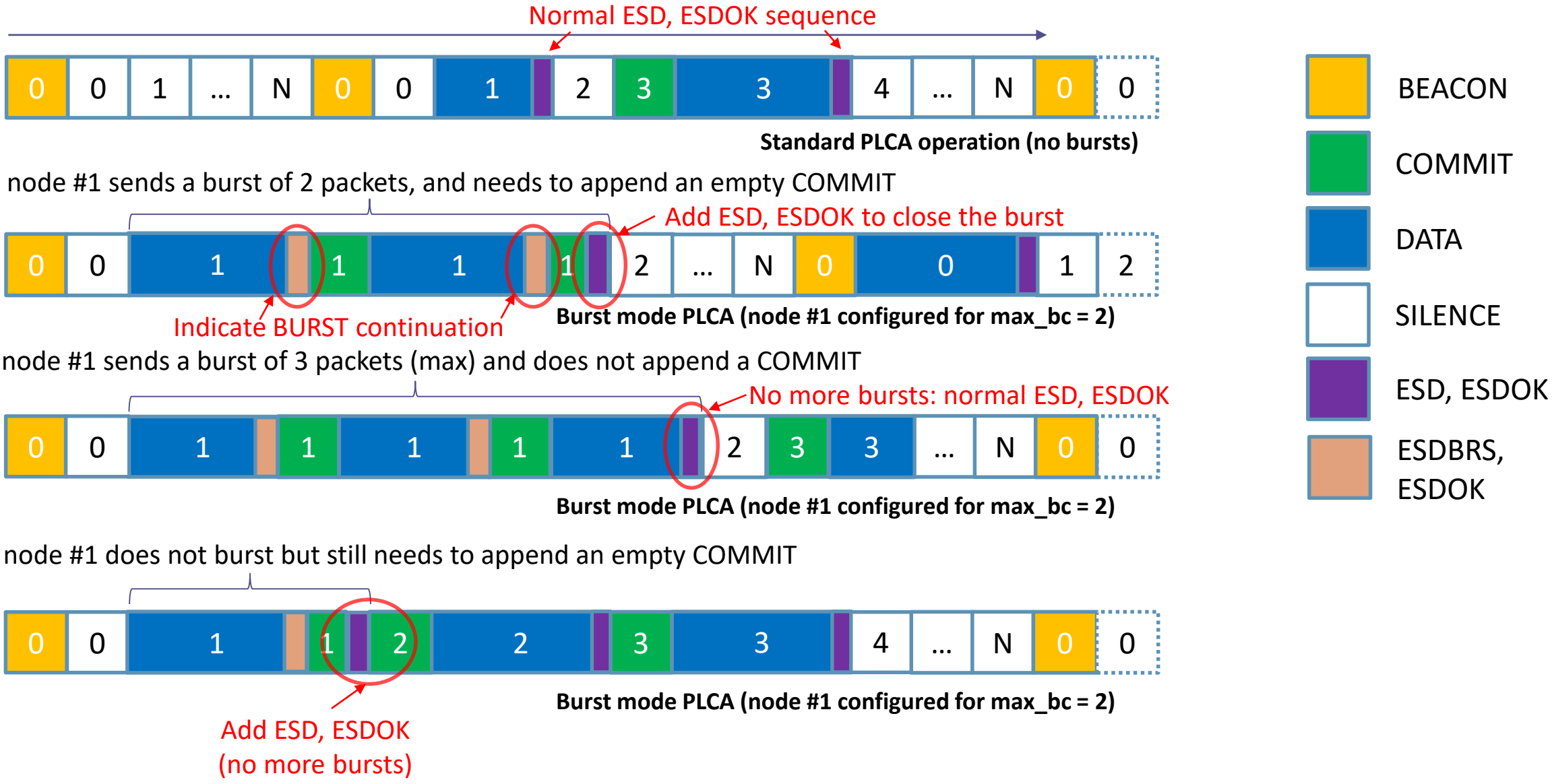
Problem outline

- PLCA burst mode has been added to Clause 148 in draft 2.2 as per http://www.ieee802.org/3/cg/public/Nov2018/beruto_3cg_PLCA_burst_mode_revB%20.pdf.
- The addition of this new feature created a couple of problems in Clause 147
  - A COMMIT (coded as 'J' in 4B/5B) is added at the end of a packet when burst mode is enabled
    - Such COMMIT can be followed by either a packet or **silence**.
    - Detecting **silence** (High-Z) is not reliable as detecting a specific code
    - In the latter case the PCS RX signals a "False carrier" on the MII
      - This is not supposed to happen since it's normal burst mode behavior
  - Likewise, a packet (after ESD, ESDOK/ERR sequence) can be followed by either **silence** or COMMIT
    - Again, detecting **silence** (High-Z) is not reliable as detecting a specific code
- Besides, there was one missing change for Clause 148
  - Depending on implementation (internal delays), PLCA DATA State Diagram could detect a false reception when filling the IPG with idle.

Proposed solution

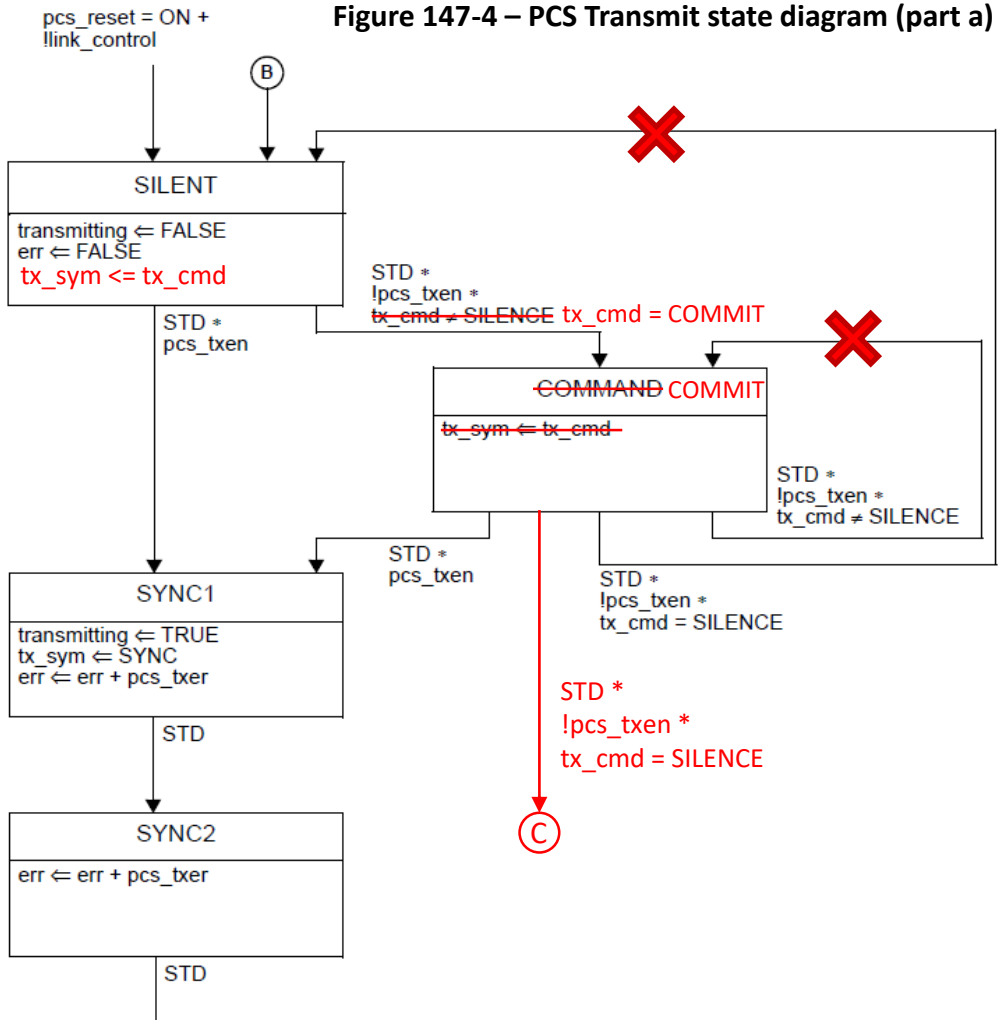
- Use explicit ESD, ESDOK 5B symbol sequence to end a COMMIT request when the MAC has no more packets to send in a burst
  - This also prevents the spurious “FALSE carrier” indication
- Use a different ESD code to terminate a packet when a BURST follows
  - This also simplifies significantly the receiver as ESDOK/ERR is always followed by silence
- Increase minimum DME silence period to guarantee at least one full 5B symbol of silence afterwards
- State diagram fix to Clause 147
  - The number of changes may look significant but the actual –*functional*– modification is very limited
- State diagram fix to Clause 148

Proposed solution



PCS TX state diagram changes

Figure 147-4 – PCS Transmit state diagram (part a)



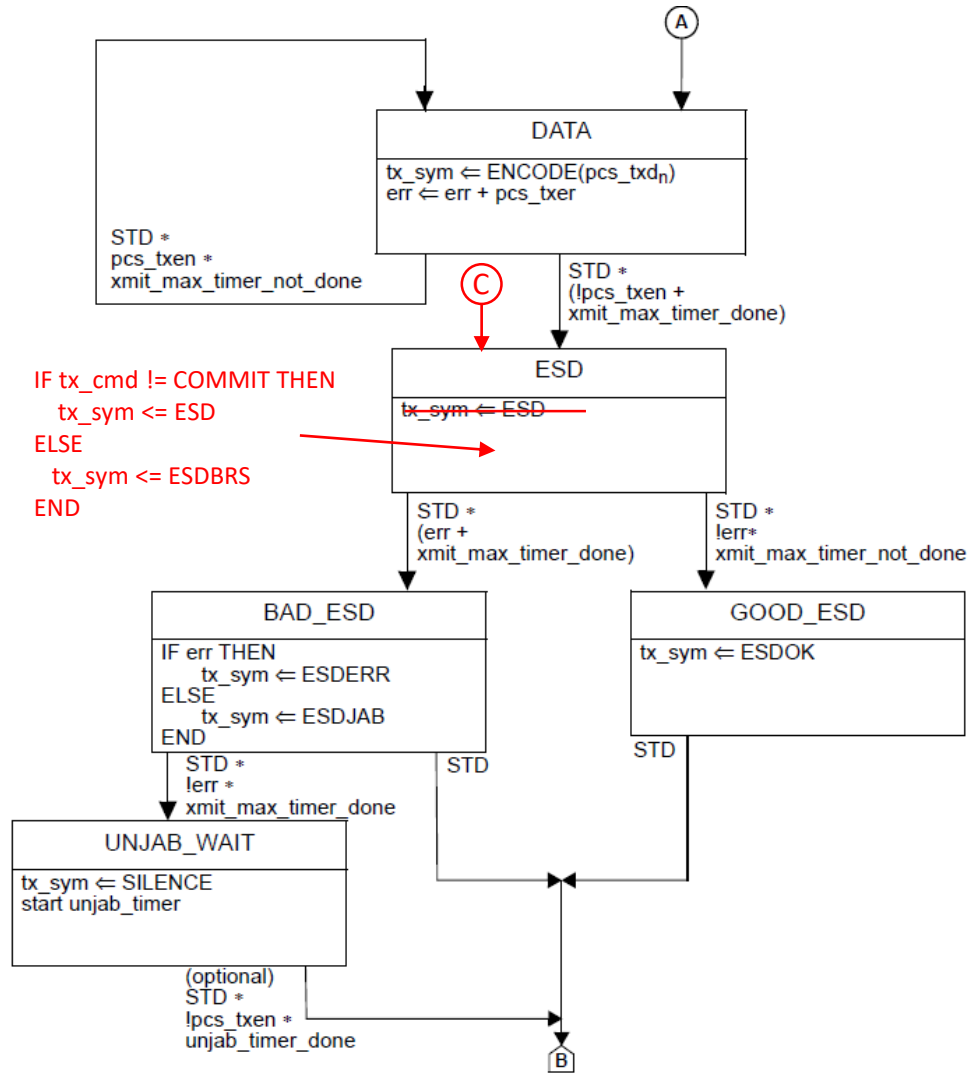


Figure 147–4—PCS Transmit state diagram (part b)

PMA and PCS RX state diagram changes

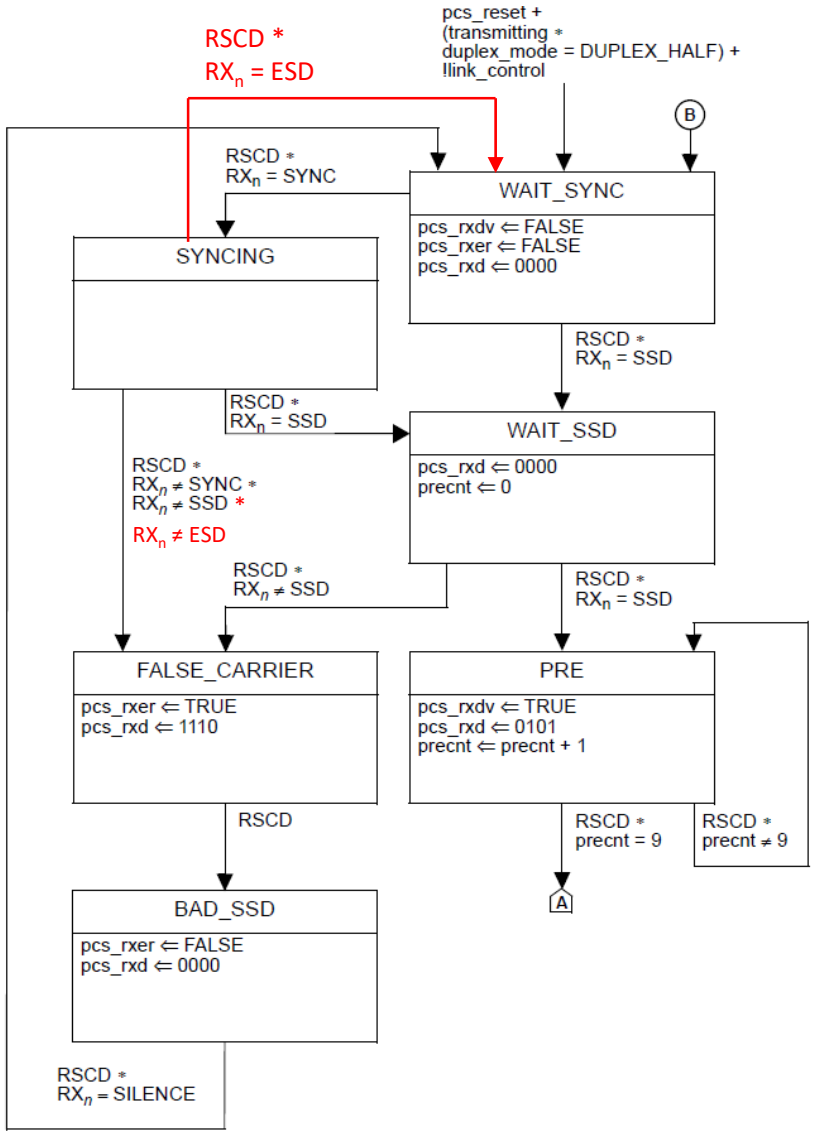


Figure 147–7—PCS Receive state diagram (part a)

Table 147–2—DME Timings

Parameter name	Description	Minimum value	Nominal value	Maximum value	Unit of measure
T1	Delay between transmissions	~~200~~ 480	—	—	ns
T2	Clock transition to clock transition	–100 ppm	80	+100 ppm	ns
T3	Clock transition to data transition (data = 1)	38	40	42	ns

480 ns is one 5B symbol + 1 DME encoded bit

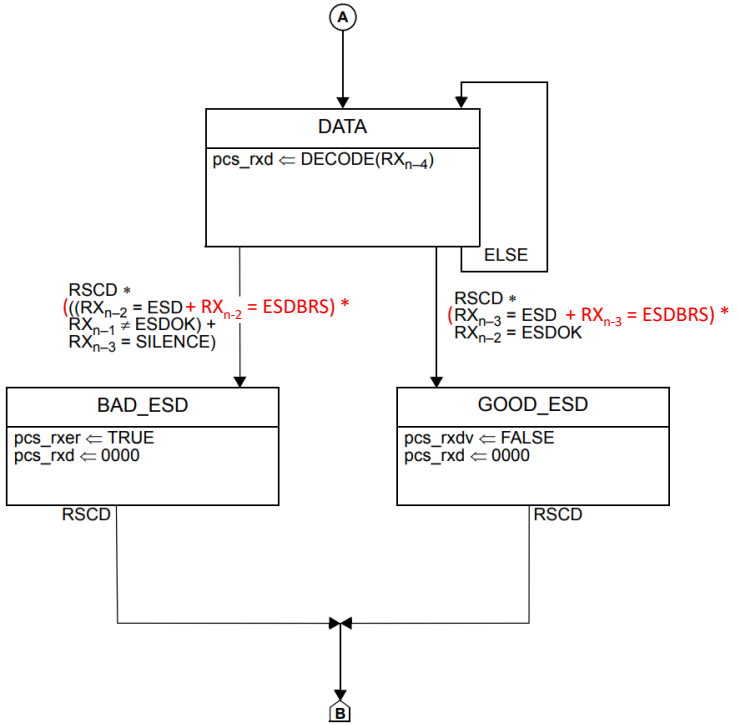


Table 147–1—4B/5B Encoding *(continued)*

Name	4B	5B	Special function
E	1110	11100	—
F	1111	11101	—
I	N/A	11111	SILENCE
J	N/A	11000	SYNC
K	N/A	10001	ESDERR
T	N/A	01101	ESD / HB
R	N/A	00111	ESDOK / ESDBRS
H	N/A	00100	SSD
N	N/A	01000	BEACON
S	N/A	11001	ESDJAB

PLCA DATA state diagram changes

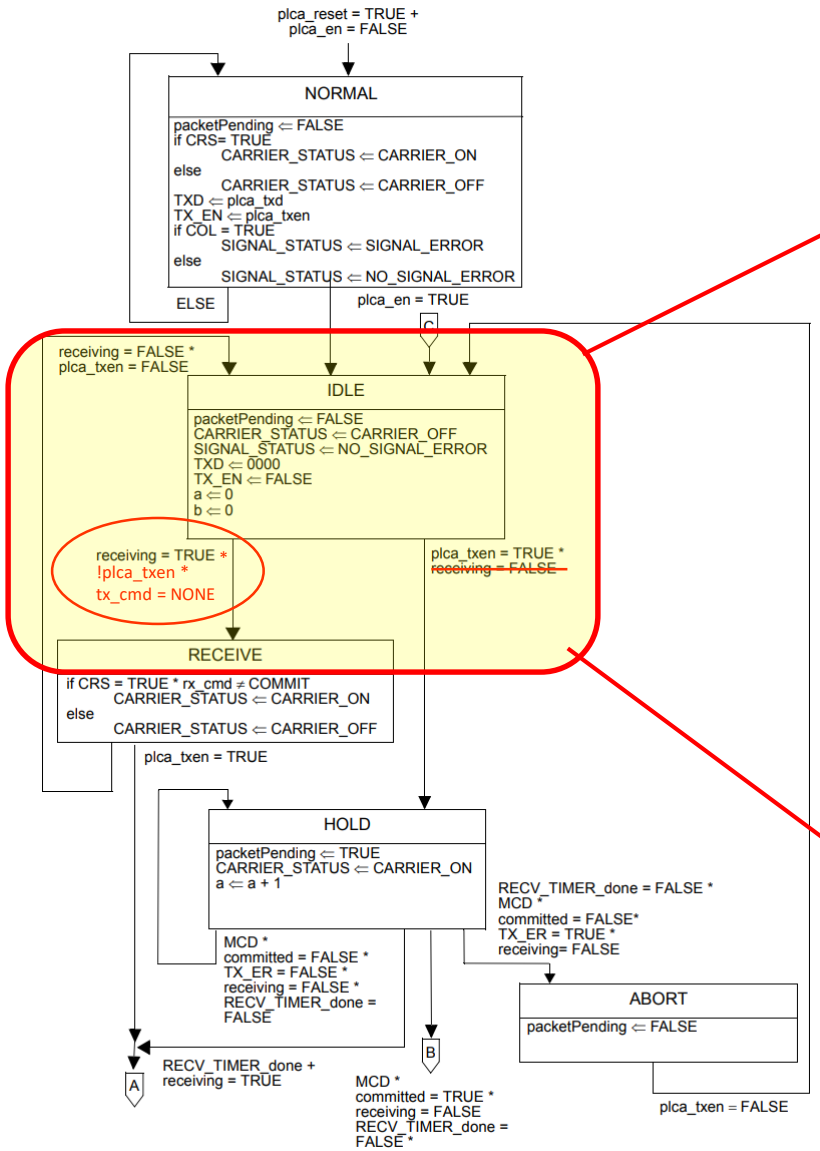
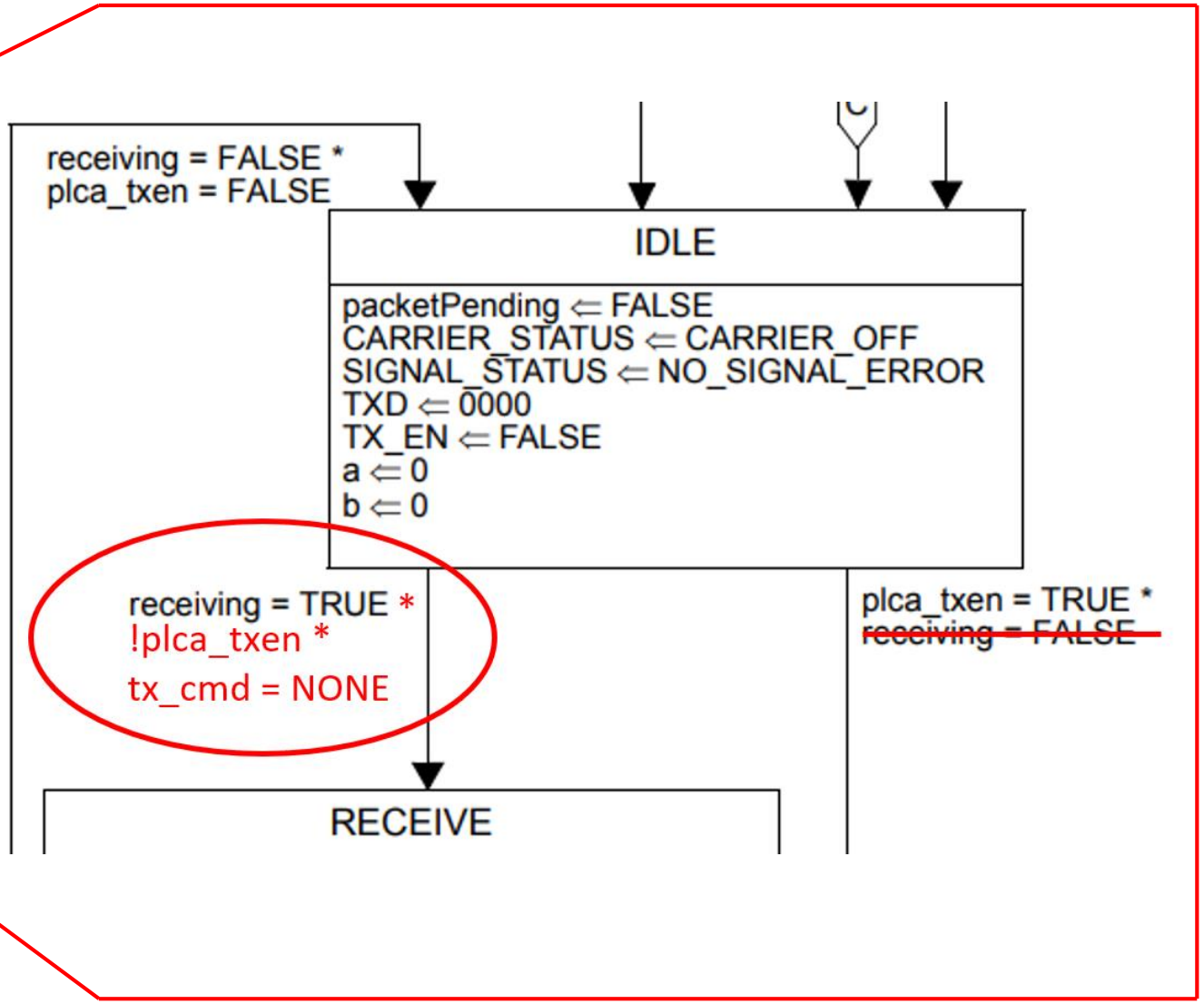


Figure 148–5—PLCA DATA state diagram



THANK YOU!