



Performance comparison study for Rx vs Tx based equalization for C2M links

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Outline

- AWGN theory on Tx vs. Rx equalization
- Simulation results based on realistic channels and SerDes models

Assumptions for Theoretical Model

- Channel amplitude response has linear roll-off in dB
- Infinite length linear equalization
- Zero forcing solution
- Noise modeled as AWGN

Equalization Penalty

■ Rx Linear Equalization Penalty:

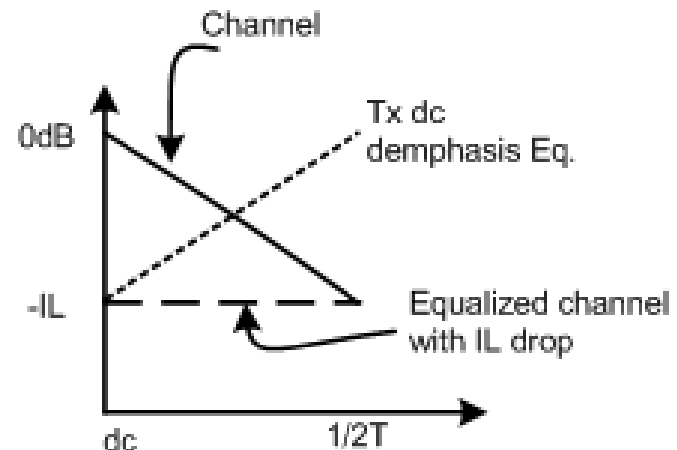
$$Rx_P = 10 \log_{10} \left(T \int_{-1/2T}^{1/2T} 1/|H(f)|^2 df \right)$$

where $|H| = 10^{(-2T*f*IL/20)}$ and IL is the insertion loss at Nyquist.

$$Rx_P = 10 \log_{10} \left(\frac{10^{IL/10} - 1}{IL \cdot \ln(10)/10} \right)$$

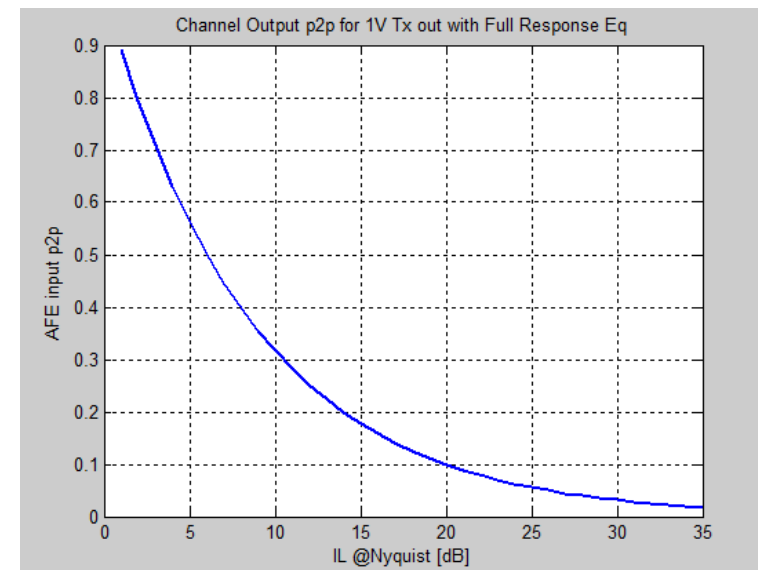
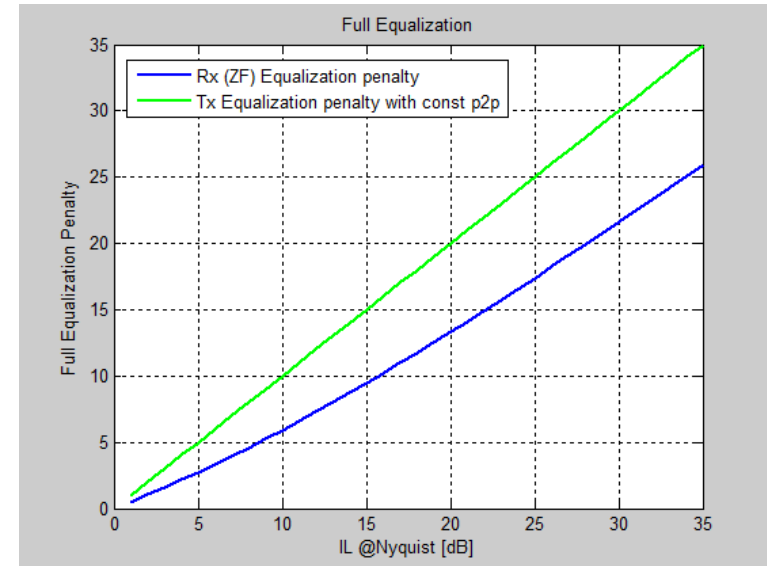
■ Tx Equalization Penalty:

$$Tx_P = IL$$



Theoretical Equalization Penalty Comparison

- Tx equalization is worse than Rx equalization. Rx Eq penalty follows L2-norm of $1/|H|$ and Tx Eq penalty follows Infinite-norm of $1/|H|$.
- At $IL=12\text{dB}$, Tx penalty is 12dB but Rx penalty is 7.3dB. 4.7dB delta.
- With say $IL=12\text{dB}$, with Tx equalization, the Rx input p2p is only 250mvp2p for 1Vp2p @ Tx out.



Specs used for the analysis

	High level specs used for analysis			Comments
	Buad Rate	53.125	Gbuad	
TX	TX Swing	0.8	Vdpp	
	RLM	0.95	-	
	SNDR	33	dB	
	RJ	175	fs rms	
	DJ	400	fs pk-pk	
	FIR	4	Taps	2 Pre
	TX Rise time	6.5	ps	20%-80%
RX	CTLE Boost	10	dB	
	CTLE 2nd Pole	40	GHz	
	Rx Noise	4	mV rms	actual density incorporated
	RJ	175	fs rms	
	DJ	600	fs pk-pk	
	Die CAP	130	fF	

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The diagram illustrates a digital baseband receiver architecture. The process begins with a **PRBS GEN** block, which feeds into a **MAPPER** block. The output of the MAPPER is then processed by a **TX FIR** block. The output of the TX FIR is then split into two paths: one path goes through a **DAC** (Digital-to-Analog Converter) block, which also receives inputs from **Quantizer**, **BW** (Bandwidth), **Noise**, and **Jitter** blocks. The other path goes through a **Thru Channel** block. The output of the Thru Channel is then processed by a **Xtalk (N Channels)** block. The outputs of the DAC and the Xtalk block are then summed at a summation node (Σ). The output of this summation node is then processed by a **Termination** block. The output of the Termination block is then processed by a **CTLE (Peaking, Zero, Pole)** block. The output of the CTLE block is then summed with the output of the **CTLE ORN** (Offset Noise) block at a summation node (Σ). The output of this summation node is then processed by an **AGC1 (BW, Gain, THD)** block. The output of the AGC1 block is then summed with the output of the **AGC ORN** (Offset Noise) block at a summation node (Σ). The output of this summation node is then processed by a **T&H (Jitter)** block. The output of the T&H block is then processed by a **FFE** (Feed-Forward Equalization) block. The output of the FFE block is then summed with the output of the **FFE Noise** block at a summation node (Σ). The output of this summation node is then processed by an **AGC2 (Gain)** block. The output of the AGC2 block is then summed with the output of the **VGA2 Noise** block at a summation node (Σ). The output of this summation node is then processed by a **DFE** (Decision Feedback Equalization) block. The output of the DFE block is then summed with the output of the **Slicer Noise** block at a summation node (Σ). The output of this summation node is then processed by a **Slicers** block. The output of the Slicers block is then processed by a **CDR** (Clock Data Recovery) block. The output of the CDR block is then processed by an **Adaptation Loops** block. The output of the Adaptation Loops block is then processed by a **PRBS Lock** block. The output of the PRBS Lock block is then fed back to the **PRBS GEN** block.

Noise contribution of AFE blocks added at the appropriate location in the link

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Tx and Rx FFE optimization

- Rx FFE is optimized using Minimum Mean Square Error (MMSE) criteria for any given Tx FIR, channel, xtalk etc.
- The Tx FIR is brute force optimized based on the link SNR.

Channels

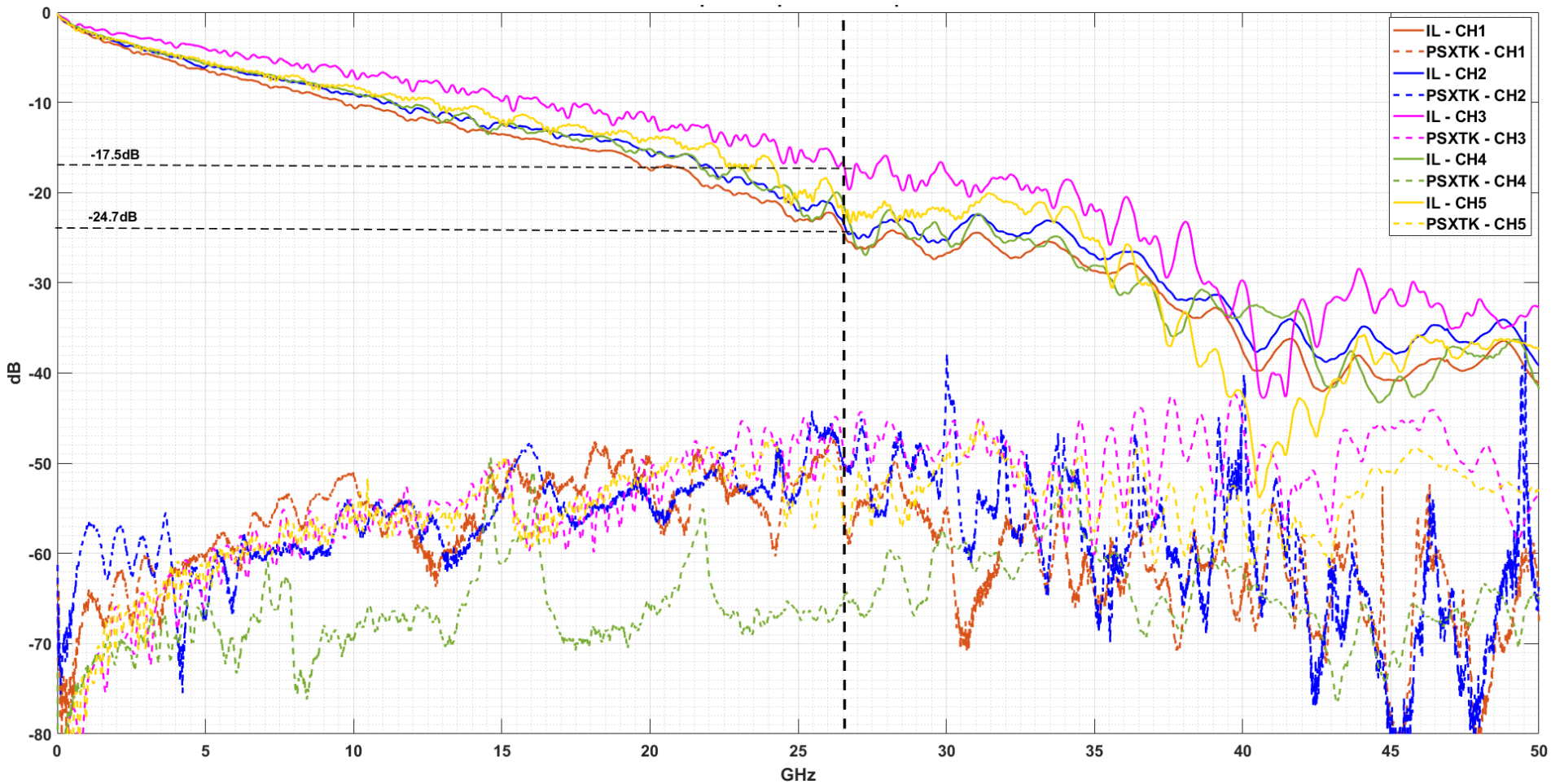
■ 5 channels were selected for the analysis

- 16dB C2M channel contribution from lim_3ck_01_1118 (referred to CH1)
 - Bangkok contribution
- 14dB C2M channel contribution from lim_3ck_01b_0718 (referred to as CH2)
- Customer proprietary channel (referred to as CH3)
- Channel contribution from tracy_100GEL_06_0118 (referred to CH4)
 - OIF Micro-via case
- Channel contribution from mellitz_3ck_02_0518 (referred to CH5)
 - 14dB BC-BOR-N-N-N

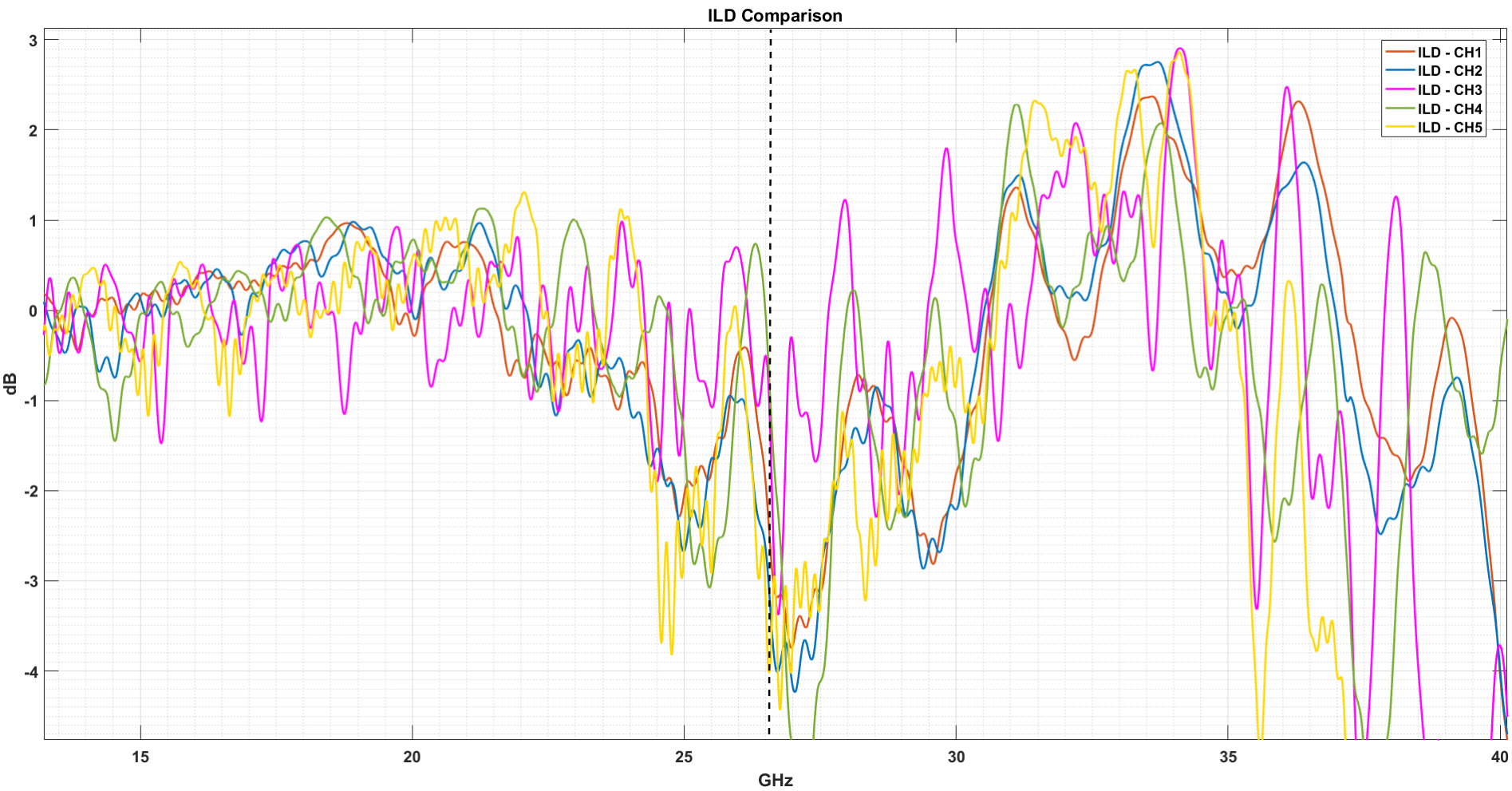
■ Package models and die models

- Channel above include cascade of both PKG and Die models for Thru and Xtalk channels
- No PKG cross-talk is included in the simulations
- Uses a 30mm host package design from current customer
- Uses a 4mm package design from current product indicative of 100G devices
- Uses a ~130fF equivalent load for the die

Bump to bump channel frequency response



ILD Comparison



SNR Simulation Results

				Channel - 1	Channel - 2	Channel - 3	Channel - 4	Channel - 5
			IL @ Nyq (dB)	24.7	23.4	17.2	21.4	22.9
			ILDMax (upto Nyq) dB	4.8	5.2	4.2	4.7	5.5
Architecture		Configuration		SNR (dB)				
11T TX FFE (2Pre) → RX CTLE/VGA → Tail DFE	#Tail DFE	0		19.3	19.8	19.3	18.8	18.7
	#Tail DFE	16		19.7	20.8	21.1	19.5	19.2
4T TX FFE (2Pre) → RX CTLE/VGA → 6T RX FFE (2 Pre) → Tail DFE	#Tail DFE	0		19.4	19.4	21.8	20.5	20.2
	#Tail DFE	16		22.4	23.5	23.8	21.6	22.5

■ Note:

- Rx FFE without DFE has shorter span in the simulations (covers upto 3 post + CTLE), compared to TX FFE case which has upto 8 post taps + CTLE

Summary

- TX FFE heavy architecture shows worse SNR compared to RX FFE
 - The noise at various input blocks of the receiver was included based on analog simulations
 - 20.5dB SNR is not sufficient to close system budgets to account for tolerances, and yield
- Rx FFE based architecture is more robust under the various channels studied (lossy, reflective, etc)
- A detailed implementation of the RX FFE based architecture and TX FFE based architecture shows only a 10% power delta between the 2 cases in 7nm process