C2C COM Simulations

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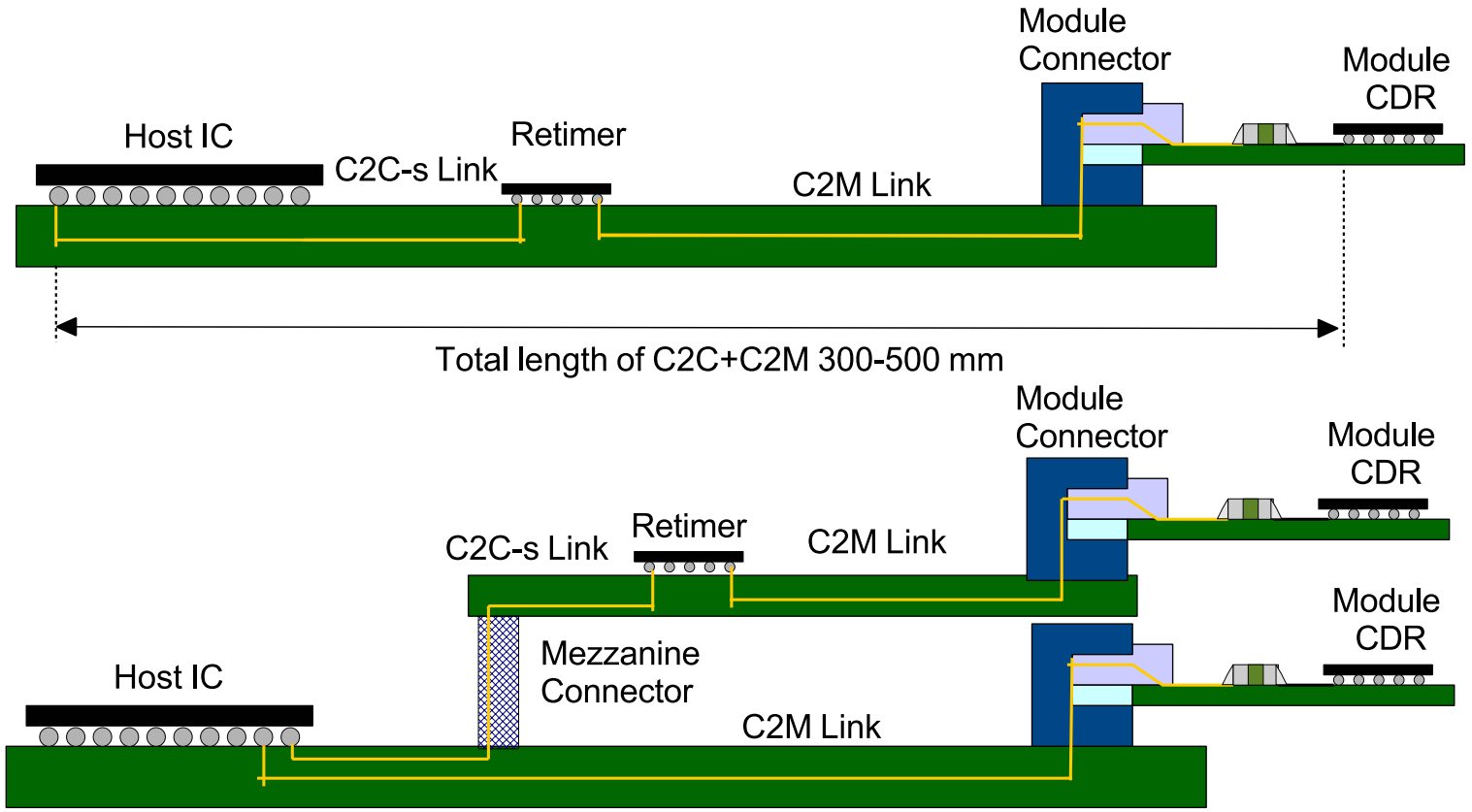
Overview

- **C2C COM analysis**
  - 4 Lim channels between 16.5 to 17.5 dB loss
  - 1 Gore PCB channel with 20 dB loss
  - 1 Gore cabled channel with 20 dB loss
- **Equalizer considered**
  - 8 tap DFE, 5 tap DFE, 4 tap DFE, and 5 tap FFE + 1T DFE
- **Using adopted KR CTLE and T-Coil model**
- **Key consideration for C2C link are:**
  - Operation with end-end FEC where link must operate with acceptable burst error rate
  - The DFE taps are reported for further analysis
  - Given that key application of C2C links are retimers/inverse-gearbox power a low power interface such as ½ the power of KR is desirable.

Two Common C2C-S Applications

- **These two common C2C applications can satisfied with ~300 mm trace and by repurposing 16 dB C2M budget**
  - Connecting to far-side of the ASIC IO may require retimer
  - Modules mounted on mezzanine card.



Overview of C2C Attributes In Comparisons to C2M and KR

- **The key advantage of C2C over KR is operating with end-end FEC and lower power.**

Parameters	C2M	C2C	KR
Chip configuration	ASIC to CDR	ASIC to ASIC	ASIC to ASIC
Link configuration	One Connector	One Connector	2 Connectors
Host PCB Reach (mm)	~225	~360	~500
FEC operation	Pass Through	Pass Through	Terminated
FEC Interleave/Non-Interleave	NA	Same as C2M	TBD for 100G
Back Channel Link Training	NA	Optional	Required
[ASIC, CDR] Trace Lengths (mm)	[30, 8]	[31, 29]	[31, 29]
[ASIC, CDR] Package Losses (dB)	[4, 1]	[4, 4]	[4, 4]
Max channel loss at Nyquist (dB)	16	20 (TBD)*	28
Max Bump-Bump Loss (dB)	~21	~28	~36
* The task force still need to vote on the max channel loss.			

COM 2.7 Table for C2C

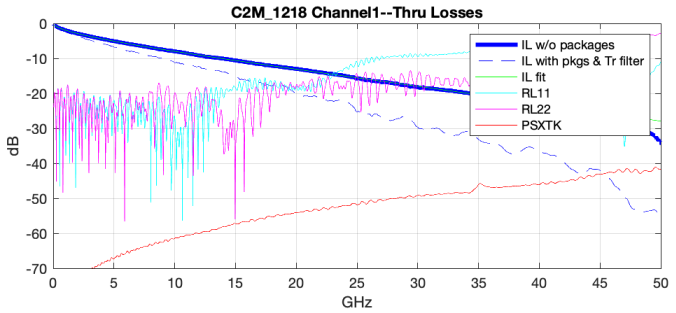
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0.12]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2 3 4]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[13 31 13 31; 1.8 1.8 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[13 31 13 31; 1.8 1.8 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 31 13 31; 1.8 1.8 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	232	mm
z_p (RX)	[7 13 11 29; 1.8 1.8 1.8 1.8]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	232	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	232	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.413	V			TDR and ERL options						
A_fe	0.413	V			TDR	1	logical				
A_ne	0.608	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.54		min		beta_x	1.70E+09					
c(-1)	[-0.34:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.12]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.05:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	5	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-16:1:0]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	21.24	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	21.24	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-4:1:0]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	0.66375	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.35										
ffe_post_tap1_max	0.35										
ffe_tapn_max	0.2										
ffe_backoff	1										

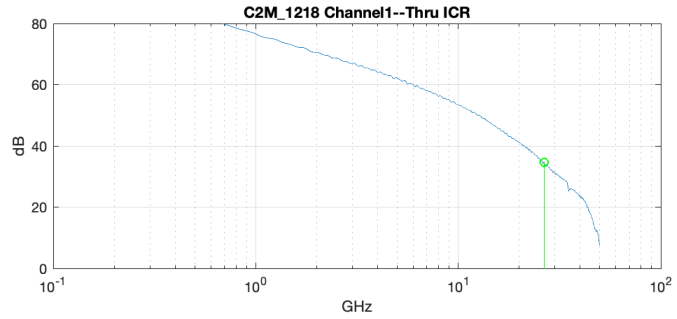
Lim C2C Channels

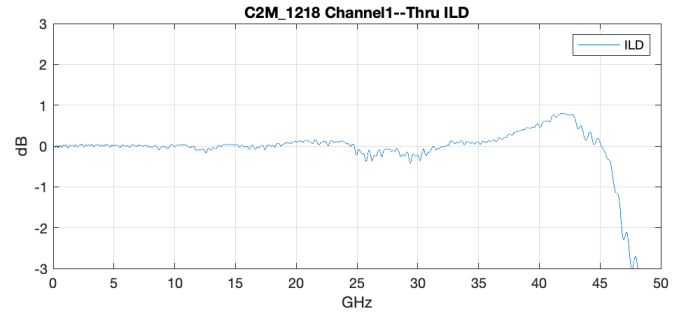
- **Total of 4 channels were built with optimized host ASIC, retimer & mezzanine connector footprint (shallow via breakout). Both shallow and long via are considered at connector and retimer footprint.**
  - Channel 1: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (shallow via breakout) + daughtercard trace 4” + Retimer footprint (shallow via) ; including 2 FEXT & 2 NEXT
  - Channel 2: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (shallow via breakout) + daughtercard trace 4” + Retimer footprint (long via); including 2 FEXT & 2 NEXT
  - Channel 3: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (long via breakout) + daughtercard trace 4” + Retimer footprint (shallow via) ; including 2 FEXT & 2 NEXT
  - Channel 4: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (long via breakout) + daughtercard trace 4” + Retimer footprint (long via) ; including 2 FEXT & 2 NEXT
  - http://www.ieee802.org/3/ck/public/tools/c2c/lim_3ck_05_0719_c2c.zip.

Lim 16.5 C2C Channel1

IL=16.5 dB, ICN=1.67, FOM_ILD=0.07







Package TX=[13, 31] and RX=[7 13] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=4.9 dB, Case II=4.2 dB
DER at 3 dB COM
Case I=2.5e-8, Case II=4e-7

DFE8 Taps=[0.64; max(2-8) 0.13]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=4.2 dB, Case II=3.9 dB
DER at 3 dB COM
Case I=4.1e-7, Case II=1e-6

DFE5 Taps=[0.57;-0.08;0.06;0.04;0.05]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.4 dB, Case II=3.8 dB
DER at 3 dB COM
Case I=3.9e-6, Case II=1.4e-6

DFE4 Taps=[0.42;-0.14;-0.05;-0.02]

5FFE+1DFE B1=0.75
COM Case I=4.1 dB, Case II=4.1 dB
DER at 3 dB COM
Case I=4.8e-7, Case II=4.8e-7

DFE Taps<0.5

Package TX= [13, 31] and RX=[11 29] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=5.4 dB, Case II=5.3 dB
DER at 3 dB COM
Case II=2.2e-9, Case II=6.1e-9

DFE8 Taps=[0.64; max(2-8) 0.19]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=4.5 dB, Case II=5.1 dB
DER at 3 dB COM
Case I=1.2e-7, Case II=1.1e-8

DFE5 Taps=[0.24;-0.05;-0.003;-0.007;0.02]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=4.3 dB, Case II=5.1 dB
DER at 3 dB COM
Case I=2.2e-7, Case II=1.7e-8

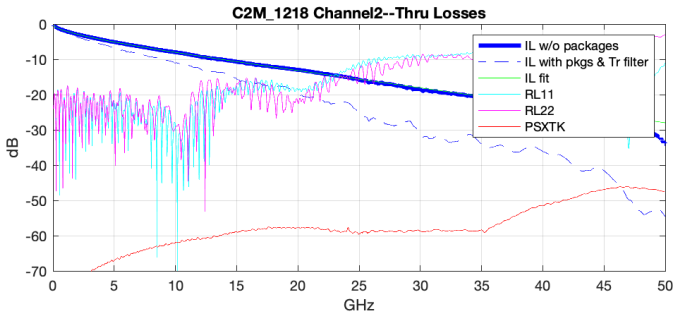
DFE4 Taps=[0.22;-0.11;-0.03;-0.01]

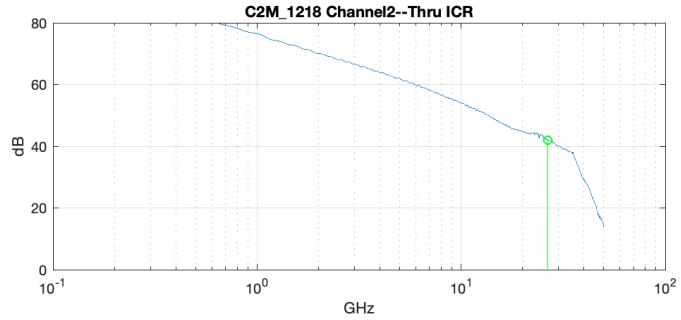
5FFE+1DFE B1(max)=0.75
COM Case I=4.3 dB, Case II=5.1 dB
DER at 3 dB COM
Case I=1.9e-7, Case II=1.6e-8

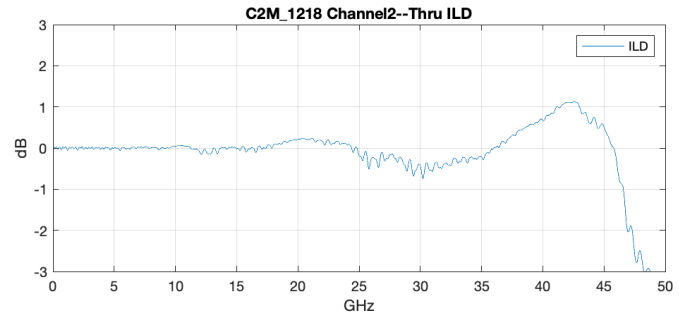
DFE Taps<0.5

Lim 16.8 dB C2C Channel2

IL=16.8 dB, ICN=0.91, FOM_ILD=0.11







Package TX=[13, 31] and RX=[7 13] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=4.7 dB, Case II=4.2 dB
DER at 3 dB COM
Case I=4.3e-8, Case II=3.3e-7

DFE8 Taps=[0.62; max(2-8) 0.2]

DFE5 B=0.75, B[2-5](max)=0.2
COM Case I=4.1 dB, Case II=3.8 dB
DER at 3 dB COM
Case I=4.5e-7, Case II=1.2e-6

DFE5 Taps=[0.42;-0.1;-0.03;-0.02;0.01]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.3 dB, Case II=3.8 dB
DER at 3 dB COM
Case I=4.5e-6, Case II=1.1e-6

DFE4 Taps=[0.48;-0.2;-0.06;-0.05]

FFE5+DFE1 B1=0.75
COM Case I=3.8 dB, Case II=3.9 dB
DER at 3 dB COM
Case I=1.3e-6, Case II=8.2e-7

DFE Taps<0.5

Package TX= [13, 31] and RX=[11 29] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=5.8 dB, Case II=5.5 dB
DER at 3 dB COM
Case I=1.4e-10, Case II=2.3e-9

DFE8 Taps=[0.57; max(2-8) 0.11]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=5.0 dB, Case II=5.4 dB
DER at 3 dB COM
Case I=1.3e-8, Case II=2.1e-9

DFE5 Taps=[0.23;-0.1;-0.01;-0.01;0.02]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=4.9 dB, Case II=5.4 dB
DER at 3 dB COM
Case I=2.6e-8, Case II=2.6e-9

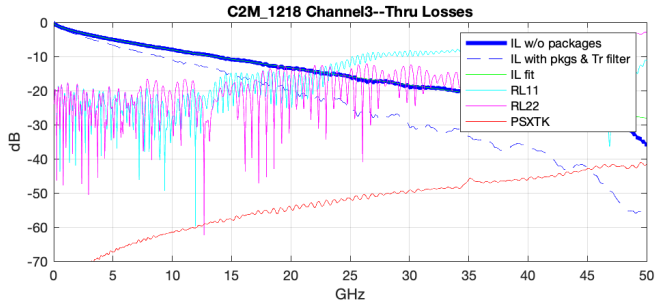
DFE4 Taps=[0.21;-0.16;-0.04;-0.03]

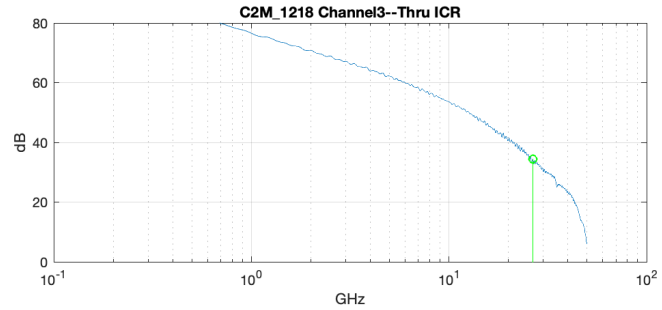
FFE5+DFE1 B1=0.75
COM Case I=4.7 dB, Case II=5.1 dB
DER at 3 dB COM
Case I=4.3e-8, Case II=1.3e-8

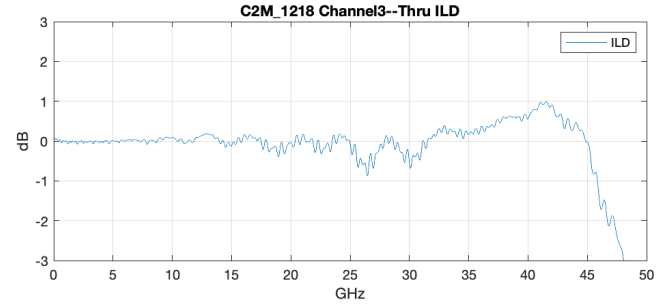
DFE Taps<0.5

Lim 17.4 dB C2C Channel3

IL=17.4 dB, ICN=1.6 mV, FOM_ILD=0.11







Package TX=[13, 31] and RX=[7 13] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=4.5 dB, Case II=3.9 dB
DER at 3 dB COM
Case I=1.2e-7, Case II=1e-6

DFE8 Taps=[0.53; max(2-8) 0.12]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=3.8 dB, Case II=3.6 dB
DER at 3 dB COM
Case I=1.2e-6, Case II=2e-6

DFE5 Taps=[0.52;0.02;0.01;0.02;0.03]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.0 dB, Case II=3.4 dB
DER at 3 dB COM
Case I=1.1e-5, Case II=3.8e-6

DFE4 Taps=[0.49;-0.13;-0.06;-0.02]

FFE5+DFE1 B1=0.75
COM Case I=3.2 dB, Case II=3.7 dB
DER at 3 dB COM
Case I=6.6e-6, Case II=1.4e-6

DFE Taps<0.5

Package TX= [13, 31] and RX=[11 29] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=4.9 dB, Case II=4.8 dB
DER at 3 dB COM
Case I=3e-8, Case II=5.8e-8

DFE8 Taps=[0.49; max(2-8) 0.05]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=4.0 dB, Case II=4.6 dB
DER at 3 dB COM
Case I=6.2e-7, Case II=9.9e-8

DFE5 Taps=[0.31;-0.05;-0.01;0.01;0.02]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.7 dB, Case II=4.2 dB
DER at 3 dB COM
Case I=4e-5, Case II=1.1e-5

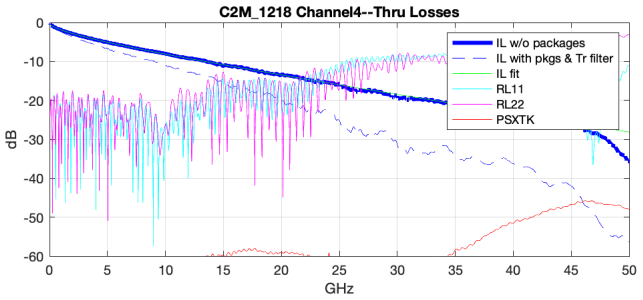
DFE4 Taps=[0.23;-0.15;-0.04;-0.007]

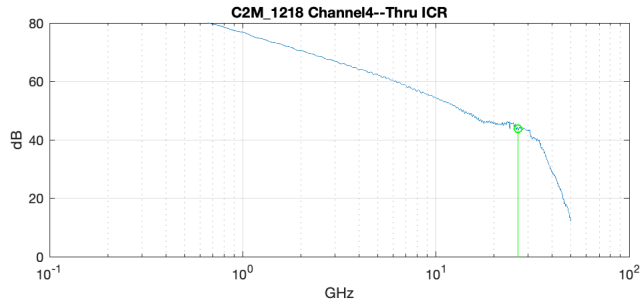
FFE5+DFE1 B1=0.75
COM Case I=4.2 dB, Case II=4.6 dB
DER at 3 dB COM
Case I=2.6e-7, Case II=4.6e-7

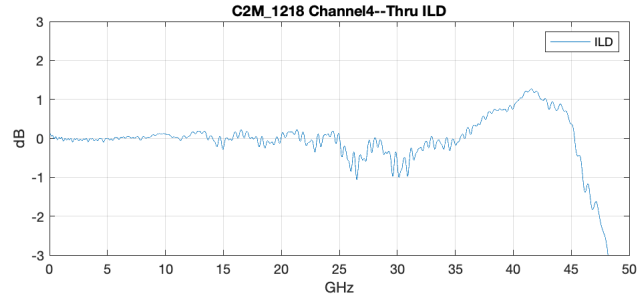
DFE Taps<0.5

Lim 16.8 dB C2C Channel4

IL=16.8 dB, ICN=0.91, FOM_ILD=0.11







Package TX=[13, 31] and RX=[7 13] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=4.5 dB, Case II=3.9 dB
DER at 3 dB COM
Case I=1.2e-7, Case II=8.9e-7

DFE8 Taps=[0.72; max(2-8) 0.2]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=3.9 dB, Case II=3.6 dB
DER at 3 dB COM
Case I=8.e-7, Case II=2e-6

DFE5 Taps=[0.51;-0.033;0.01;0.03;0.04]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.2 dB, Case II=3.4 dB
DER at 3 dB COM
Case I=6.2e-6, Case II=3.4e-6

DFE4 Taps=[0.48;-0.19;-0.07;-0.04]

FFE5+DFE1 B1=0.75
COM Case I=3.8 dB, Case II=3.6 dB
DER at 3 dB COM
Case I=1.2e-6, Case II=2e-6

DFE Taps=0.75

Package TX= [13, 31] and RX=[11 29] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=5.5 dB, Case II=4.9 dB
DER at 3 dB COM
Case I=1.7e-9, Case II=2.8e-8

DFE8 Taps=[0.63; max(2-8) 0.14]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=4.7 dB, Case II=4.8 dB
DER at 3 dB COM
Case I=4.7e-8, Case II=4.5e-8

DFE5 Taps=[0.30;-0.1;-0.02;-0.008;0.02]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=4.5 dB, Case II=4.7 dB
DER at 3 dB COM
Case I=1.3e-7, Case II=7.7e-8

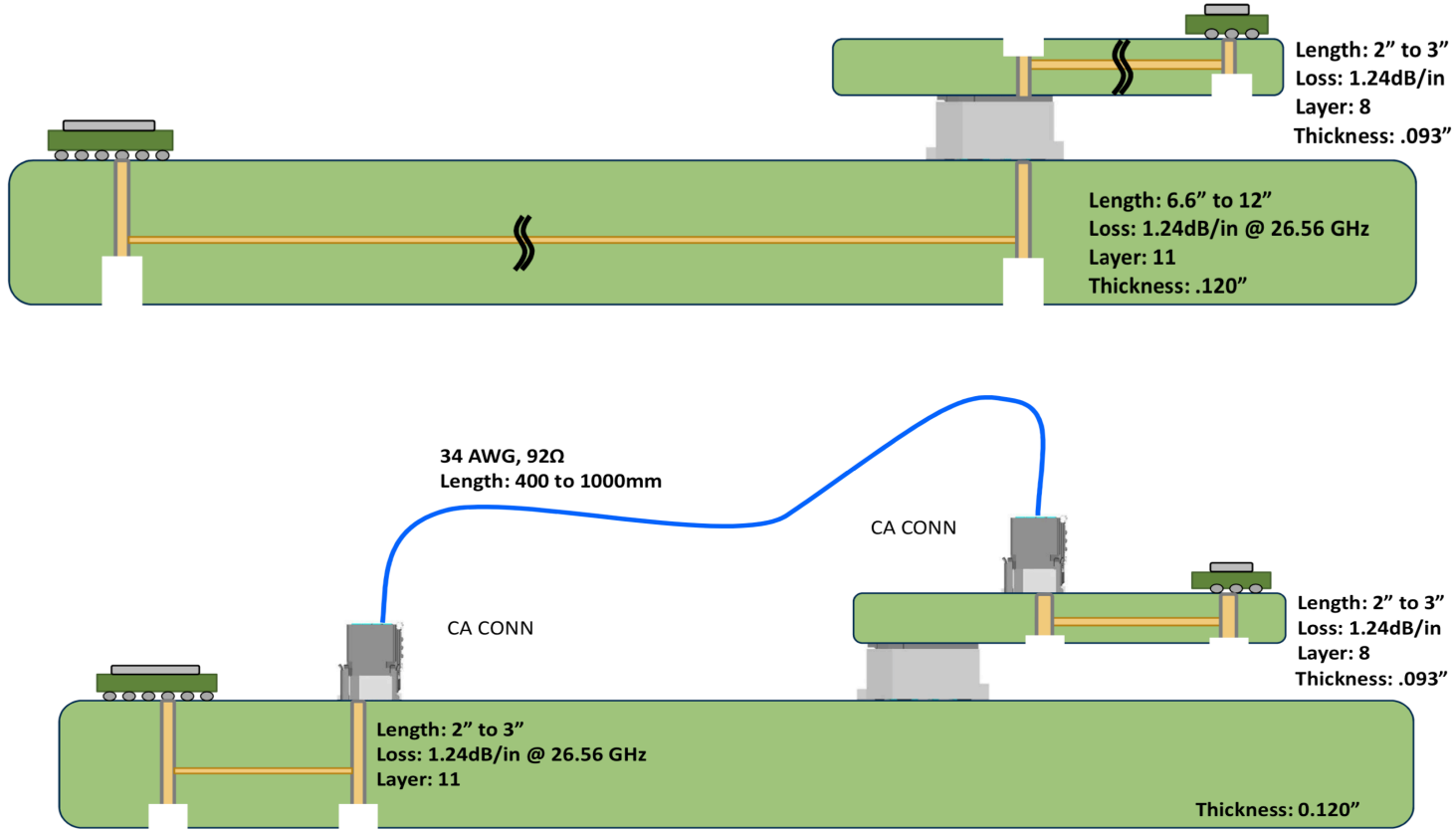
DFE4 Taps=[0.26;-0.13;-0.03;-0.02]

FFE5+DFE1 B1=0.75
COM Case I=4.6 dB, Case II=4.5 dB
DER at 3 dB COM
Case I=1.0e-7, Case II=1.4e-7

DFE Taps=0.75

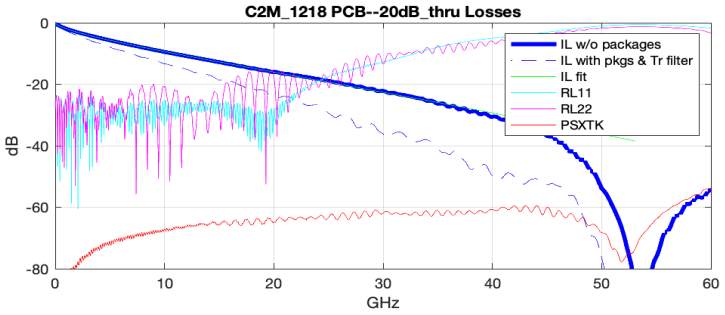
Gore C2C Channels

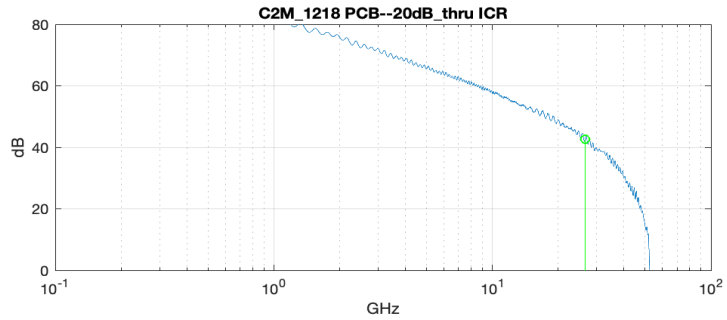
- **Construction of C2C channels based on PCB and cable construction provided by Brandon Gore**
  - http://www.ieee802.org/3/ck/public/19_05/gore_3ck_01a_0519.pdf

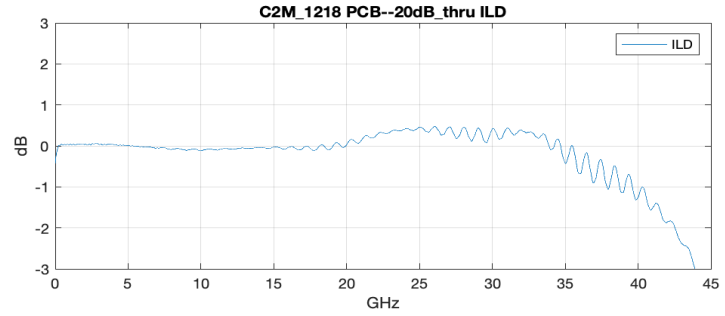


Gore C2C 20 dB PCB Channels

IL=20.1 dB, ICN=0.48 mV, FOM_ILD=0.20







Package TX=[13, 31] and RX=[7 13] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=5.0 dB, Case II=4.7 dB
DER at 3 dB COM
Case I=1.1e-8, Case II=5.3e-8

DFE8 Taps=[0.48; max(2-8) 0.03]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=4.5 dB, Case II=4.67 dB
DER at 3 dB COM
Case I=1.1e-7, Case II=8.5e-8

DFE5 Taps=[0.64;0.02;0.01;0.003;0.05]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.6 dB, Case II=4.3 dB
DER at 3 dB COM
Case I=2.4e-6, Case II=2.9e-7

DFE4 Taps=[0.68;-0.11;-0.07;-0.04]

FFE5+DFE1 B1=0.75
COM Case I=4.2 dB, Case II=4.6 dB
DER at 3 dB COM
Case I=3.6e-7, Case II=1.5e-7

DFE Taps=0.75

Package TX= [13, 31] and RX=[11 29] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=5.9 dB, Case II=5.4 dB
DER at 3 dB COM
Case I=8.5e-11, Case II=1.5e-9

DFE8 Taps=[0.51; max(2-8) 0.03]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=5.4 dB, Case II=5.2 dB
DER at 3 dB COM
Case I=2.5e-9, Case II=4.8e-9

DFE5 Taps=[0.51;-0.01;-0.03;-0.02;0.02]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=5.0 dB, Case II=4.9 dB
DER at 3 dB COM
Case I=2.1e-8, Case II=2.4e-8

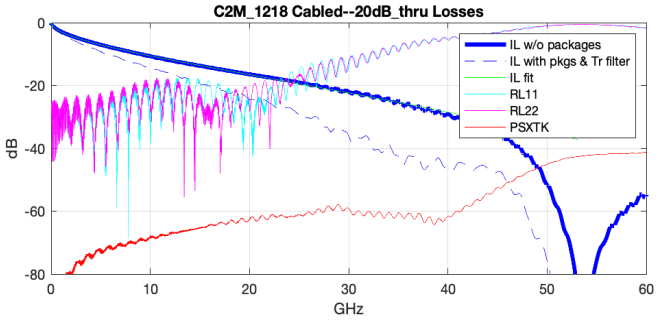
DFE4 Taps=[0.5;-0.02;-0.04;-0.03]

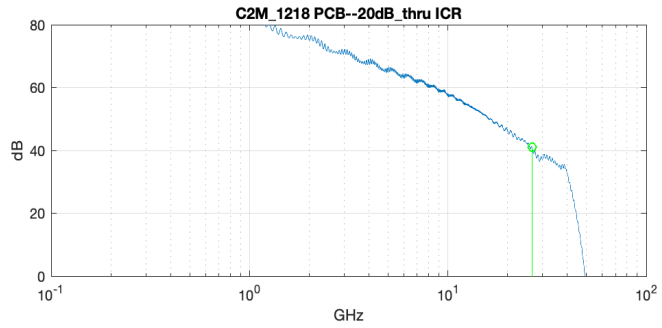
FFE5+DFE1 B1=0.75
COM Case I=5.0 dB, Case II=5.0 dB
DER at 3 dB COM
Case I=1.7e-8, Case II=1.7e-8

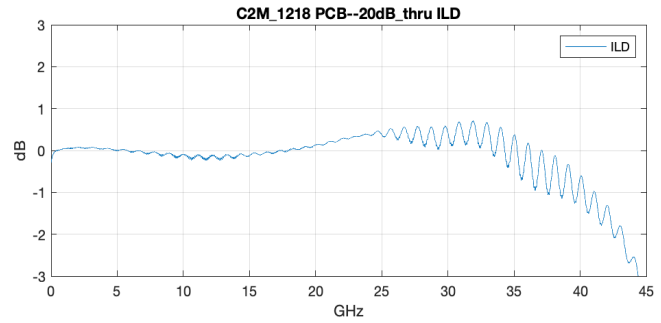
DFE Taps=0.75

Gore C2C 20 dB Cable Channels

IL=19.8 dB, ICN=0.55 mV, FOM_ILD=0.21







Package TX=[13, 31] and RX=[7 13] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=4.7 dB, Case II=4.3 dB
DER at 3 dB COM
Case I=6.8e-8, Case II=2.5e-7

DFE8 Taps=[0.49; max(2-8) 0.1]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=4.3 dB, Case II=4.2 dB
DER at 3 dB COM
Case I=2.7e-7, Case II=3.5e-7

DFE5 Taps=[0.41;-0.06;0.02;0.02;0.01]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=3.9 dB, Case II=4.1 dB
DER at 3 dB COM
Case I=9.2e-7, Case II=4.6e-7

DFE4 Taps=[0.44;-0.12;-0.04;-0.02]

FFE5+DFE1 B1=0.75
COM Case I=4.6 dB, Case II=4.4 dB
DER at 3 dB COM
Case I=8.3e-8, Case II=2e-67

DFE Taps=0.75

Package TX= [13, 31] and RX=[11 29] mm

DFE8 B1=0.75, B[2-8](max)=0.2
COM Case I=5.7 dB, Case II=5.0 dB
DER at 3 dB COM
Case I=4.7e-10, Case II=1.8e-8

DFE8 Taps=[0.45; max(2-8) 0.03]

DFE5 B1=0.75, B[2-5](max)=0.2
COM Case I=5.2 dB, Case II=4.9 dB
DER at 3 dB COM
Case I=6.3e-9, Case II=3.2e-8

DFE5 Taps=[0.45;-0.03;-0.02;-0.005;0.01]

DFE4 B1=0.75, B[2-4](max)=0.2
COM Case I=5.1 dB, Case II=4.7 dB
DER at 3 dB COM
Case I=9.8e-9, Case II=6.8e-8

DFE4 Taps=[0.45;-0.03;-0.02;-0.01]

FFE5+DFE1 B1=0.75
COM Case I=5.2 dB, Case II=4.7 dB
DER at 3 dB COM
Case I=9.3e-9, Case II=6.7e-8

DFE Taps=0.45

Summary

- **COM analysis included both ASIC-ASIC and ASIC-CDR scenarios with following package configurations**
  - ASIC-ASIC [13, 31] mm with 1.8 mm PTH and [11, 29] mm with 1.8 mm PTH
  - ASIC-CDR [13, 31] mm with 1.8 mm PTH and [7, 13] mm no PTH
- **Summary of results and observations:**
  - Both Lim and Core channels have ~ 1 dB lower COM with ASIC-CDR package than ASIC-ASIC package
  - C2M class of equalizer such 4T FFE or 5T FFE+1T DFE is sufficient for C2C
  - The DFE taps reported at glance looks like should satisfy burst error requirements
  - After we agree on the C2C equalizer then tap weight constrain should be implemented in COM
- **C2C loss can be increased to 20 dB with end-end FEC and stay with low power equalizer class where span is ≤5T.**