Embedded PHY parameters for MPCP

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IEEE802.3ah, Edinburgh, May, 2002
IEEE 802.3ah Ethernet in the First Mile

EPON architecture

Variable packet size Ethernet frame

OLT

Upstream: burst mode, variable optical power

Downstream: continuous mode, optical power

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What to consider ....

- MPCP is to be addressed in consideration of available PMD parameters for EPON, as higher layer can adapt to PHY capacity

- Conventional IFG= 96 bits is valid for CSMA/CD, not for EPON using TDM

- Timing model, scheduling cycle, and MPCP parameters including guard time are coupled with PHY parameters, which affect system performance

- Burst mode operation has sensitivity 2dB worse and worse jitter condition than continuous mode operation

- APON based on cell transmission has relatively tight timing spec. while EPON based on packet transmission has less tight spec.
EPON modules for uplink

OLT

Tx
Rx

1490nm
1310nm

WDM

OLT

SMF

ONU

WDM

R x

1490nm

BM  Laser Driver

BM  TIA with dynamic range >25dB

BM  Postamp

CDR

1310nm

BM  Laser Driver
Parameter Definition

- $T_{LD:OFF}$: LD turn off time
- $T_{PB}$: LD prebias time
- $T_{ATC}$: threshold-level recovery time
- $T_{CDR}$: clock recovery time
- $T_{Reset}$: reset time
- $T_{DSR}$: dynamic sensitivity recovery time

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# 1.25Gbps Transceiver parameters

<table>
<thead>
<tr>
<th>OLT Rx</th>
<th>BM Transc. 2R</th>
<th>GE Transc. 2.5Gbps w/ sw</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rise/fall time</strong> (20-80%)</td>
<td>&lt;0.3</td>
<td>&lt;10</td>
</tr>
<tr>
<td><strong>LD prebias time</strong></td>
<td>2 - 12.8</td>
<td>&gt;10</td>
</tr>
<tr>
<td><strong>LD turn off time</strong></td>
<td>1 - 2</td>
<td>&gt;10</td>
</tr>
<tr>
<td><strong>ER</strong></td>
<td>&gt;10</td>
<td>&gt;10</td>
</tr>
<tr>
<td><strong>Threshold-level recovery time</strong></td>
<td>16</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Clock recovery time</strong></td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td><strong>Dyn. sensitivity recovery time</strong></td>
<td>&gt;20 - 24</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ONU Tx</th>
<th>Symbol (unit)</th>
<th>BM Transc. 2R</th>
<th>GE Transc. 2.5Gbps w/ sw</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rise/fall time</strong> (20-80%)</td>
<td>(ns)</td>
<td>&lt;0.3</td>
<td>&lt;0.3</td>
</tr>
<tr>
<td><strong>LD prebias time</strong></td>
<td>T_{PB} (ns)</td>
<td>2 - 12.8</td>
<td>&gt;10</td>
</tr>
<tr>
<td><strong>LD turn off time</strong></td>
<td>T_{LD,OFF} (bit)</td>
<td>1 - 2</td>
<td>&gt;10</td>
</tr>
<tr>
<td><strong>ER</strong></td>
<td>dBA</td>
<td>&gt;10</td>
<td>&gt;10</td>
</tr>
</tbody>
</table>
Implementation

• Bit synch.
  (i) With 2R Rx + legacy Ethernet SERDES chip
    - CDR with current Ethernet chip take 160-200bits (including comma synch.)
    - no change of PHY interface, compatible with existing Ethernet PHY chip
    - need longer guard band

  (ii) With 3R Rx + Ethernet SERDES chip with optional clock interface change
    - need shorter guard band

• PHY layer Overhead is estimated 3-6 bytes by most of FSAN companies (2002, March, EFM PMD track)

• Adapting to OLT, and universal spec for ONUs would be desirable (centralized system)
Most of BM Rx have DSR time longer than (LD:ON + LD:OFF) time

Guard band = $T_{DSR} + T_{ATC} + T_{CDR} + T_d$

$T_d$ is guard band for clock drift due to clock mismatch, RTT change, clock resolution and variable delay

Open issue: Size of IFG? From 96 bits down to 0 bit
Guard band Model

• Fixed GB
  - enough guard band to cover available PMD device capabilities

• Configurable GB
  - depends on consisting PMD device capabilities
  - OLT determines GB as a total of its DSR, ATC, CDR time plus extra guard time for clock drift
    (if (LD:ON +LD:OFF) time > DSR time, replace DSR with fixed, enough (LD:ON +LD:OFF) time)
    (not configurable with ONUs’ capabilities, which is multi-instance-based and adds complexity)
  - OLT capabilities (ATC, CDR time) report to ONUs in REGISTRATION message
  - OLT cap. Echo from ONUs in REGISTRATION_ACK message
  - ONU MAC signals PMD to turn on the LD at (prebias+ATC+CDR time) ahead of Slot Start and to turn off the LD at (Slot Start +sum of Transmitted packet length)
802.3z GbE timing-related spec.

### 1000BASE-SX/LX Jitter Budget

<table>
<thead>
<tr>
<th>Compliance point</th>
<th>Total Jitter</th>
<th>Deterministic Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>UI</td>
<td>ps</td>
</tr>
<tr>
<td>TP1</td>
<td>0.240</td>
<td>192</td>
</tr>
<tr>
<td>TP1 to TP2</td>
<td>0.284</td>
<td>227</td>
</tr>
<tr>
<td>TP2</td>
<td>0.431</td>
<td>345</td>
</tr>
<tr>
<td>TP2 to TP3</td>
<td>0.170</td>
<td>136</td>
</tr>
<tr>
<td>TP3</td>
<td>0.510</td>
<td>408</td>
</tr>
<tr>
<td>TP3 to TP4</td>
<td>0.332</td>
<td>266</td>
</tr>
<tr>
<td>TP4</td>
<td>0.749</td>
<td>599</td>
</tr>
</tbody>
</table>

**Signaling Speed:** 1.25 ± 100 ppm (GBd)
**Trise/fall (20-80%):** 0.26 ns

1) Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.

2) Measured with a conformance test signal at TP3 set to an average optical power 0.5 dB greater than the stressed receive sensitivity from receive characteristics.
Clock drift and Jitter

- EPON has a global system clock
- Clock synchronization is instance-based, as local clock is set at the point of every GATE reception
  - robust to clock drift
- Tolerable clock drift is +/- 100ppm when using GE Transc.
  for Rsv. Window size =2msec, Td = 400nsec
  when clock drift is +/- 40ppm, Td = 160nsec (25 Octets)
  for 8000byte Grant_Length allocated to ONU,
    IFG=12 Octet, and GB=50 Octets
    BW Utilization = 0.709 (min. packet size) - 0.977 (max. packet size)

- Clock drift due to RTT change
  - with extended temperature optics -40 to 85°C
    RTT change coeff. is about 7ppm/°C, which is forgiving within the Rsv. window
    If (OLT clock-ONU clock ) > (threshold for clock mismatch) occurs over several consecutive windows , rerange the ONU for RTT calibration.

- guard band for 16bit clock resolution is 4 octets

- Jitter budget for EPON would be 0.749UI above 637kHz, and jitter tolerance, jitter transfer and generation are TBD according to device capability.
BW utility

802.3

3R Rx + PHY with interface change

2R Rx + legacy Ethernet PHY

$U_{\text{max. Packet Size}}$

$U_{\text{min. Packet Size}}$

IFG=12 Octets

8000byte BW Grant

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Summary

• Issues of embedded PHY parameters for MPCP

• Need to gather from vendors standard data for PMD timing parameters for modeling and performance evaluation

• Configurable with OLT’s capability and universal spec for ONUs’ capabilities for system scalability and centralized management