IEEE P802.3ae MDC/MDIO

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Presentation purpose

- Explain what the MDIO interface is
  - For those not familiar with 802.3
- Explain what we have changed and added to the MDIO interface in 802.3ae
  - For those who are familiar with 802.3 but have not been participating in 802.3ae
- Explain how MDIO fits with 802.3ae link status and fault reporting

What is MDIO for ?

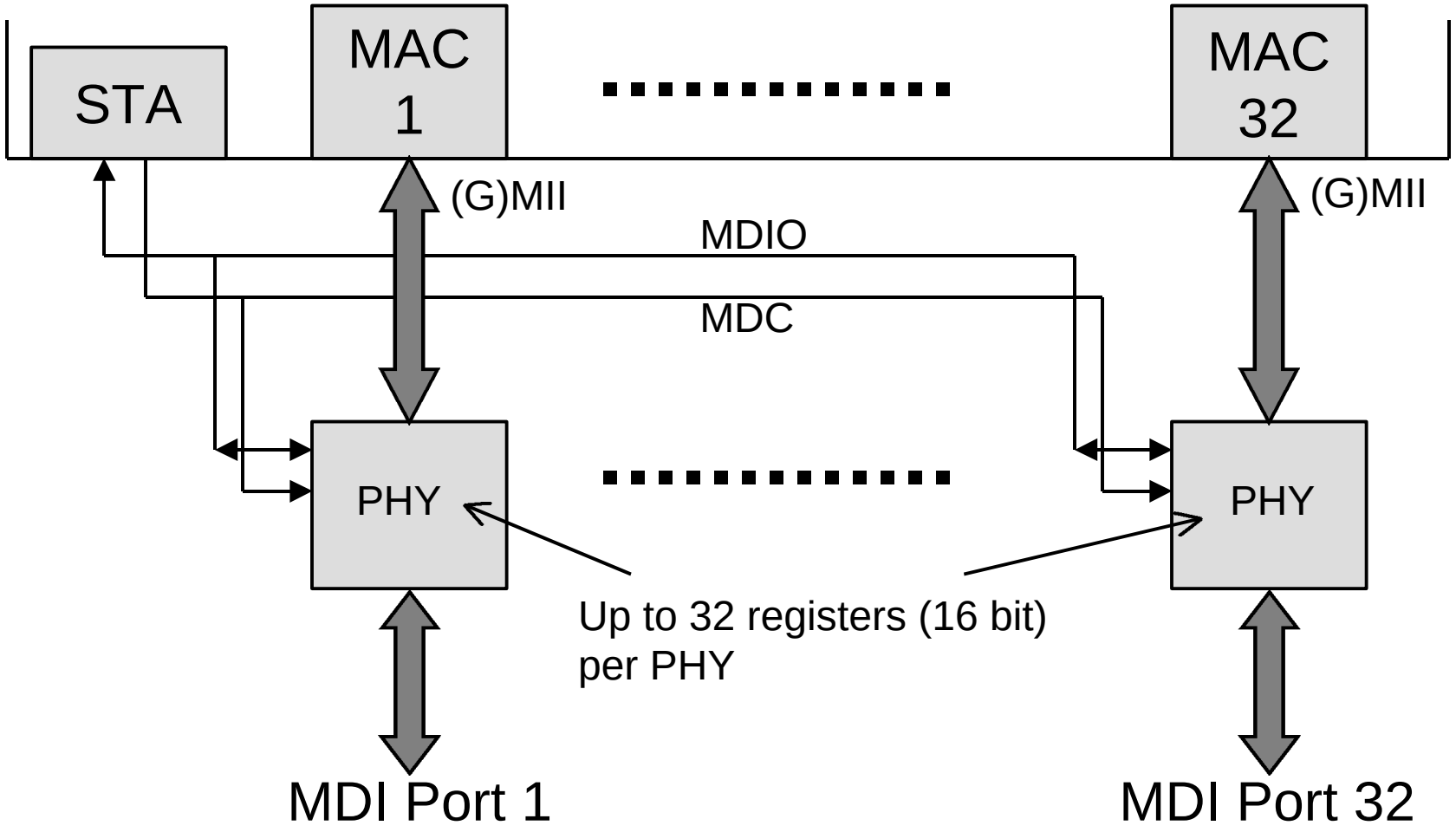
‘..a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY.’

(Clause 22.2.4)

MDIO signals

- MDC (Management Data Clock) sourced continuously from STA (station management entity)
- MDIO (Management Data Input/Output) bi-directional multi-drop bus

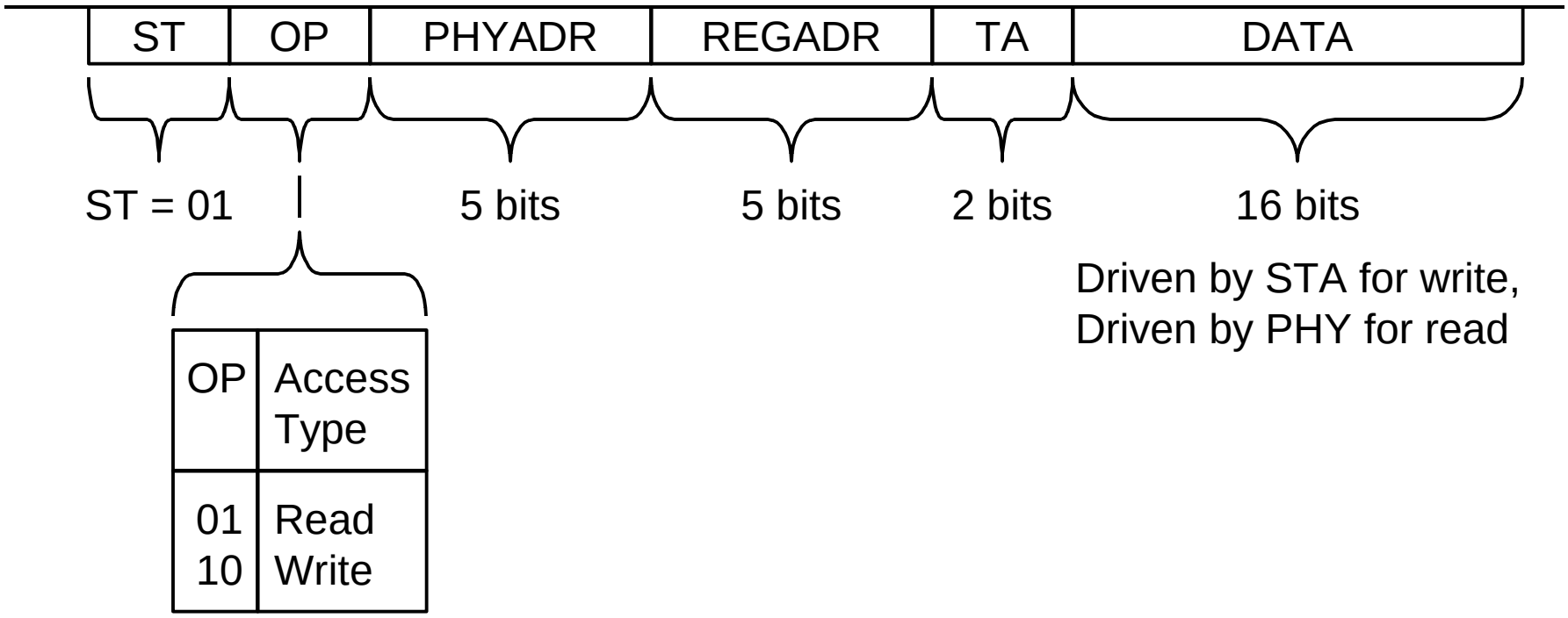
Clause 22 MDIO : Up to 32 PHYs



Clause 22 MDIO

- PHY status and control
  - Link status
  - Speed ability and selection
  - Power down for low power consumption
  - Duplex mode (full / half)
  - Control of auto-negotiation
  - Fault signalling
  - Loopback
- 2.5MHz MDC speed
  - 39 000 registers per second

MDIO frame format



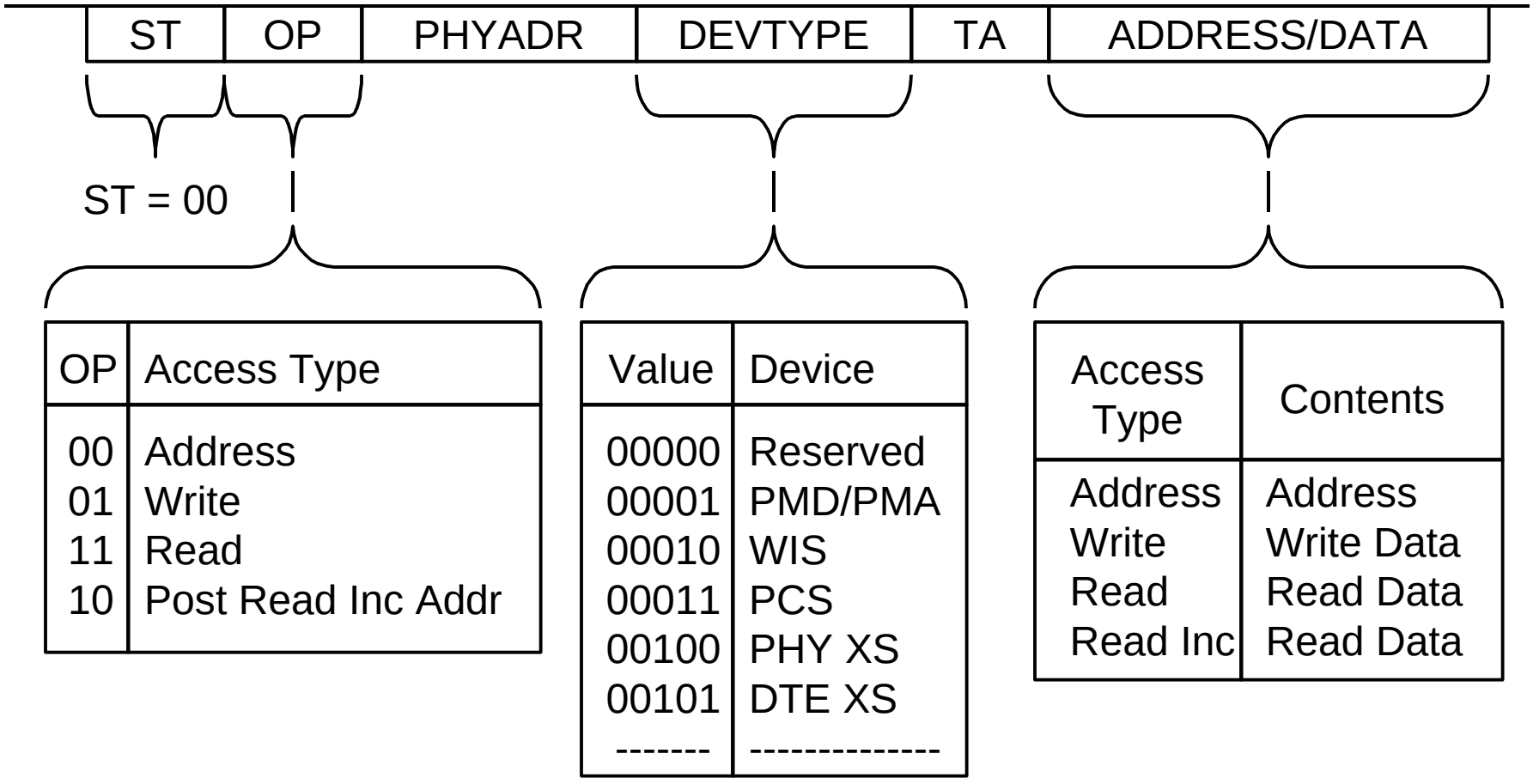
Issues with Clause 22 MDIO

- Not enough registers for future use
  - Only 4 left unallocated
- Electrical interface requires 5V tolerance
- Does not cater for multi-device PHYs

10GbE adopted proposal

- Use spare ST (start of frame) code (00)
  - Define new indirect addressing register access
  - Applicable to ST code 00 only
  - Access consists of a Address cycle followed by a Read or Write cycle
- Provides many more registers
  - 32 ports as at present
  - 32 MMDs per port (MDIO Manageable Device)
  - 65 536 registers per device

10GbE indirect addressing



OP	Access Type
00	Address
01	Write
11	Read
10	Post Read Inc Addr

Value	Device
00000	Reserved
00001	PMD/PMA
00010	WIS
00011	PCS
00100	PHY XS
00101	DTE XS
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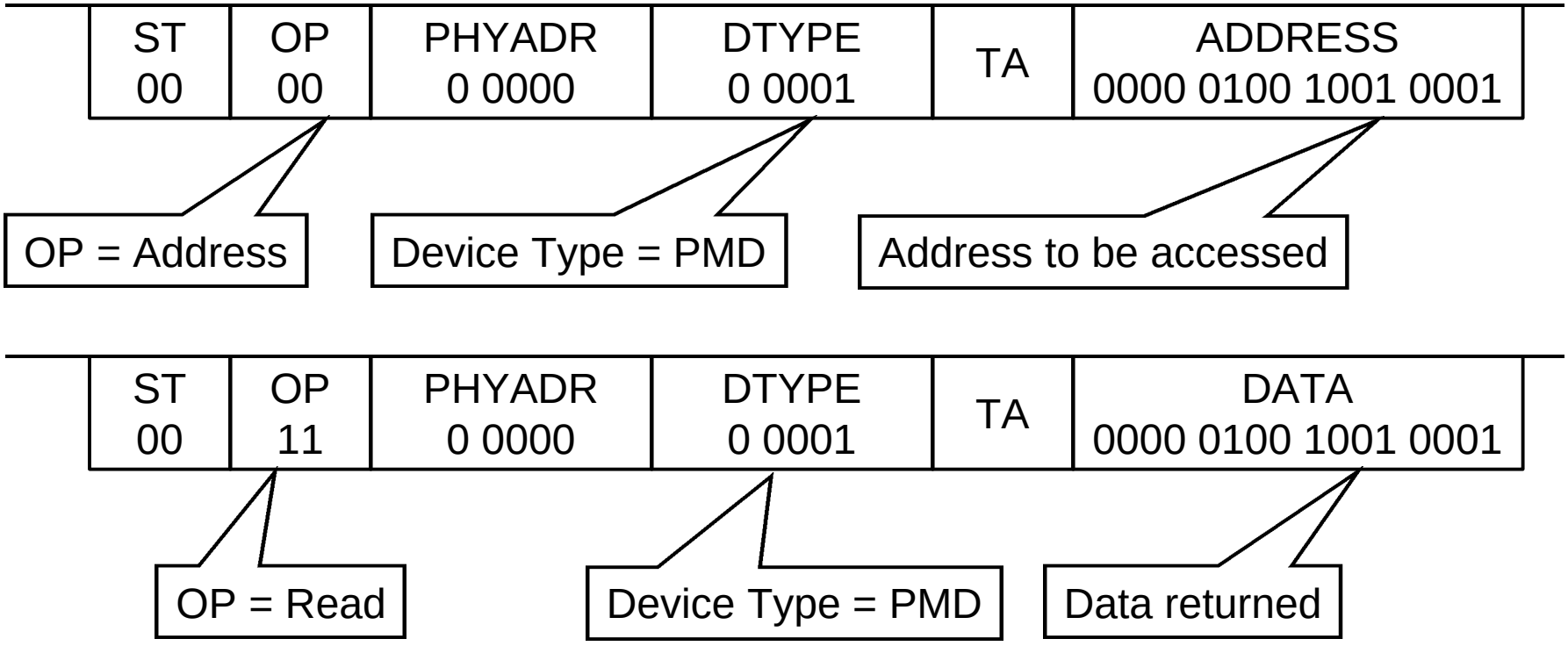
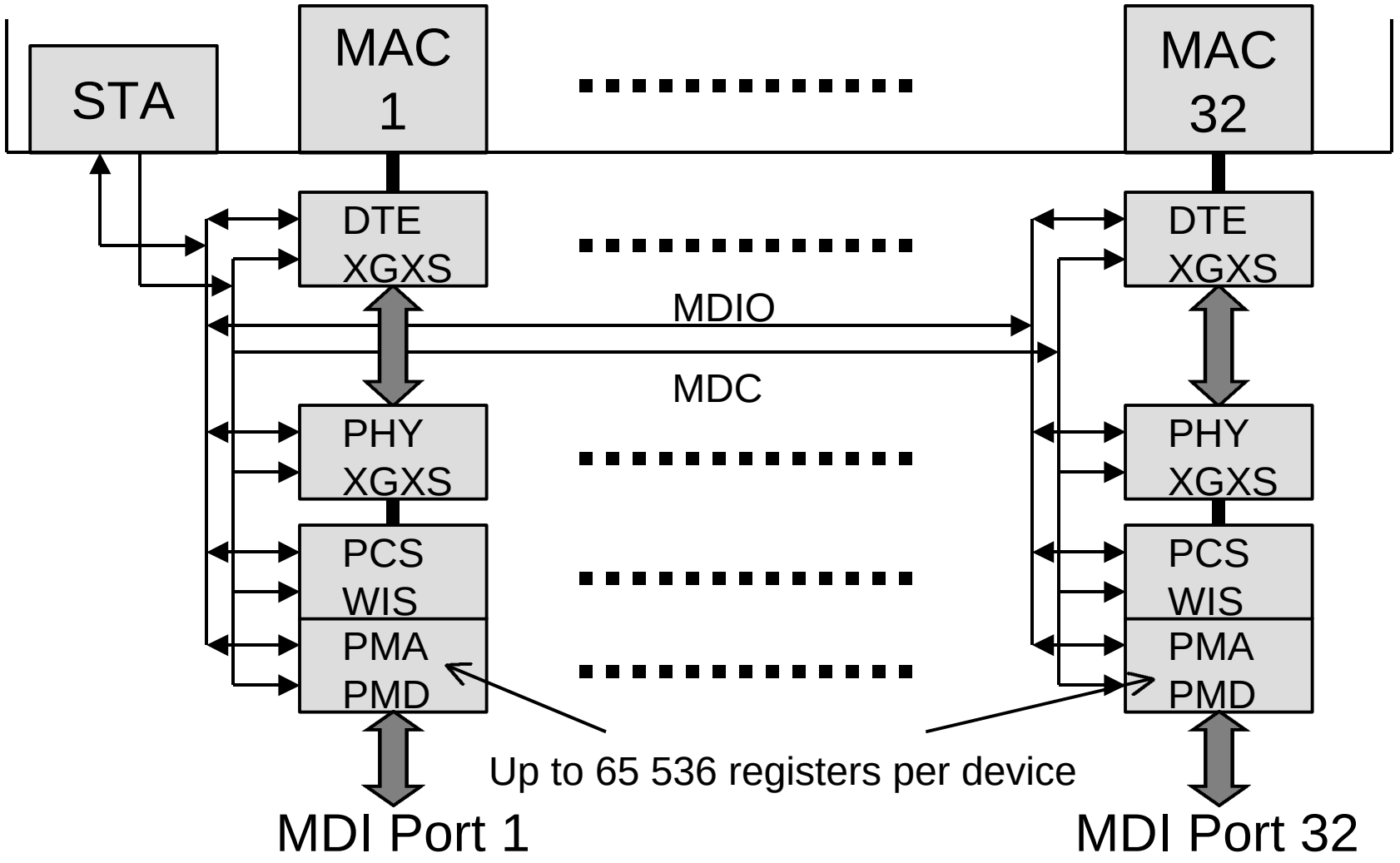
Access Type	Contents
Address	Address
Write	Write Data
Read	Read Data
Read Inc	Read Data

10GbE indirect addressing example



10GbE MDIO devices



What can the registers do ?

- All status and control
  - Link status, speed, power down, fault, loopback
  - PMD capabilities (wavelength, loopback)
  - WIS registers
  - PCS error counters, test patterns
  - XGXS status and control (XAUI)

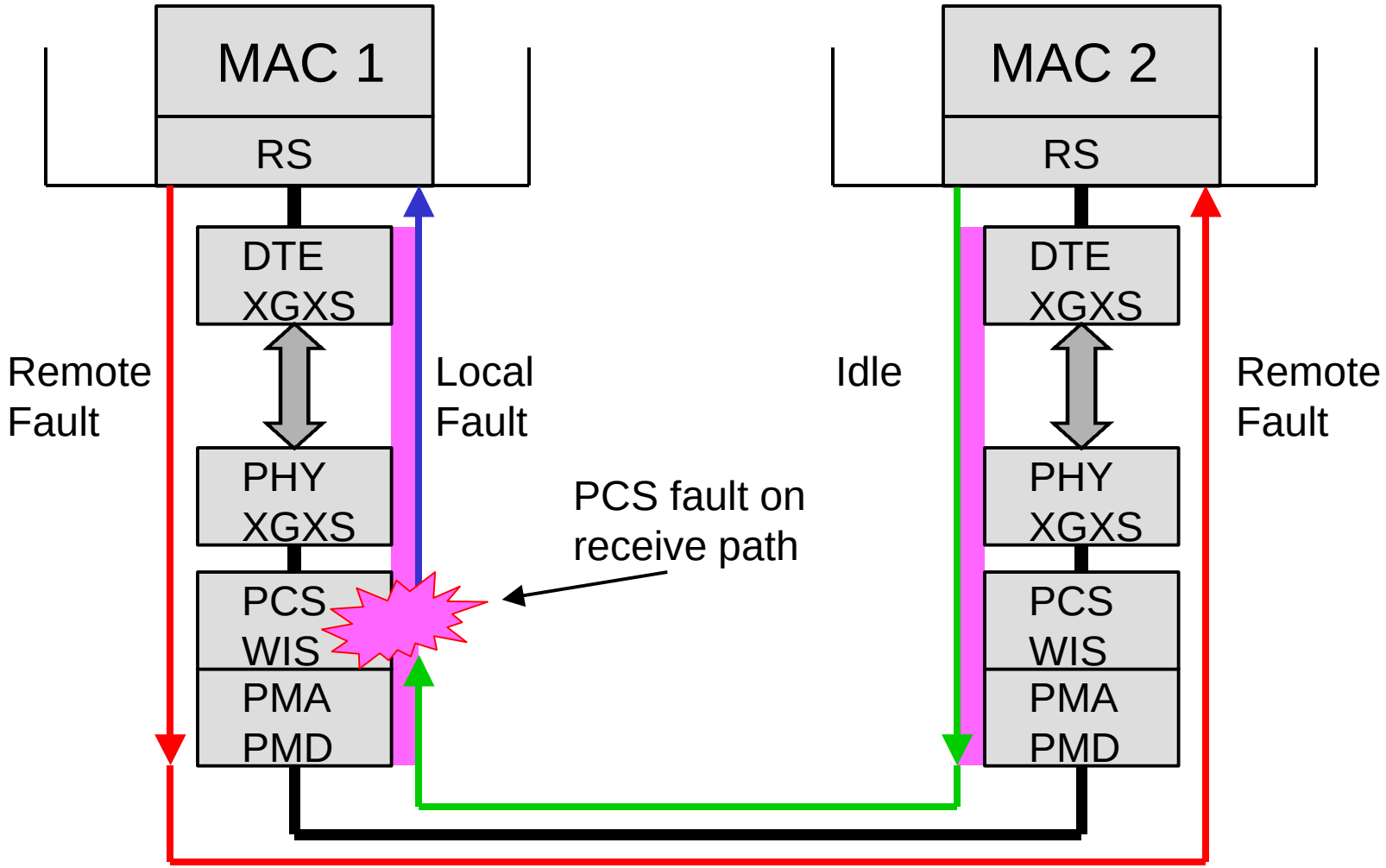
Fault signalling and link status

- Logic in the previously logic-free RS
  - http://www.ieee802.org/3/ae/public/nov00/taborek_2_1100.pdf
- Only the RS can generate RF codes
- Other devices in the link can generate LF codes and must propagate LF codes or RF codes
  - A LF condition overrides a received RF code
- An RS that receives an LF code generates an RF code on the transmit path
- An RS that receives an RF code generates IDLE on the transmit path

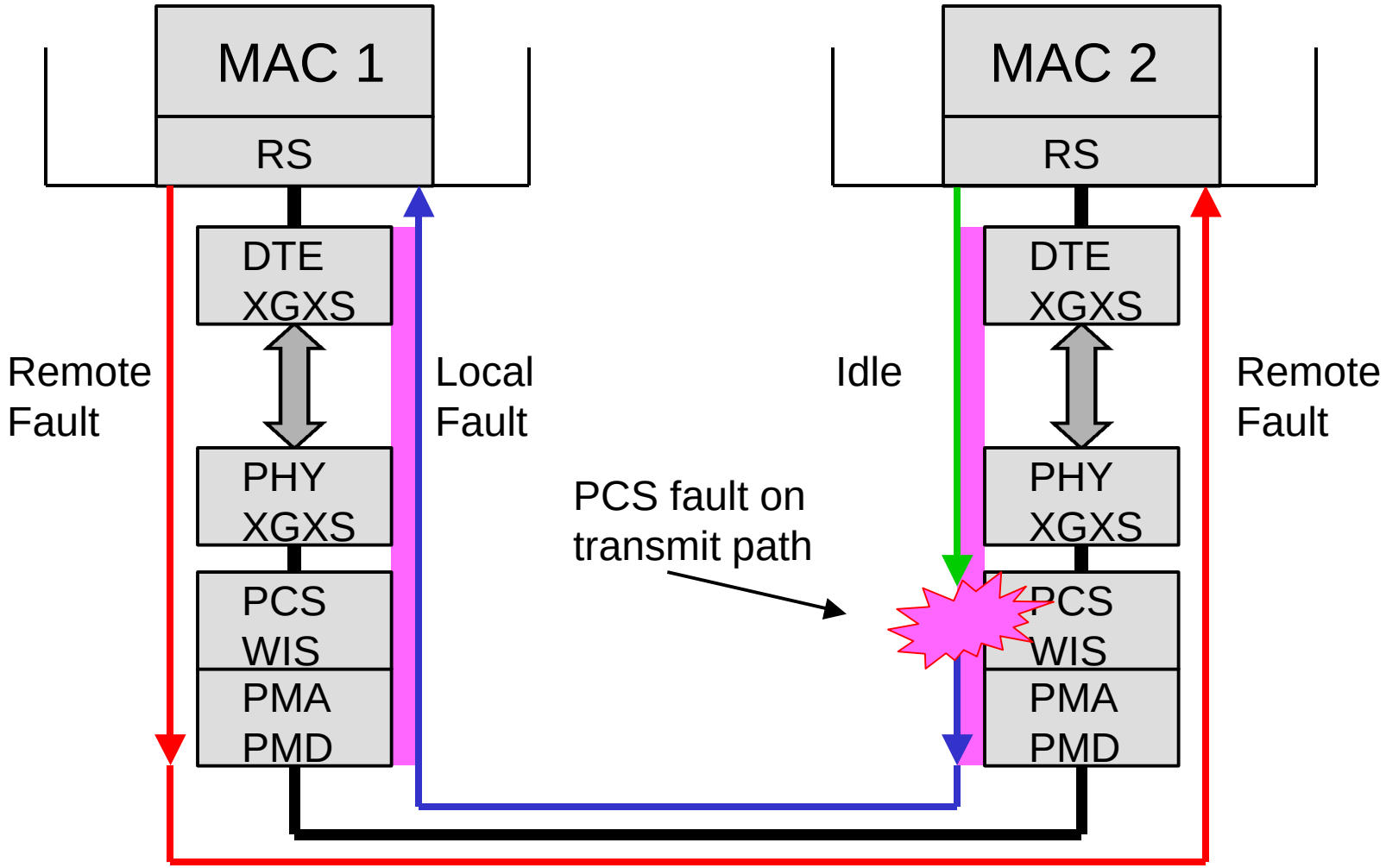
Fault signalling and link status

- MDIO used to interrogate devices when an RF code or LF code is received by the RS
  - Check transmit path for a received RF
  - Check receive path for a received LF
- Can only interrogate local devices !
  - Transmission of RF code will trigger a far end interrogation
- Link status can also be checked on a device-by- device basis

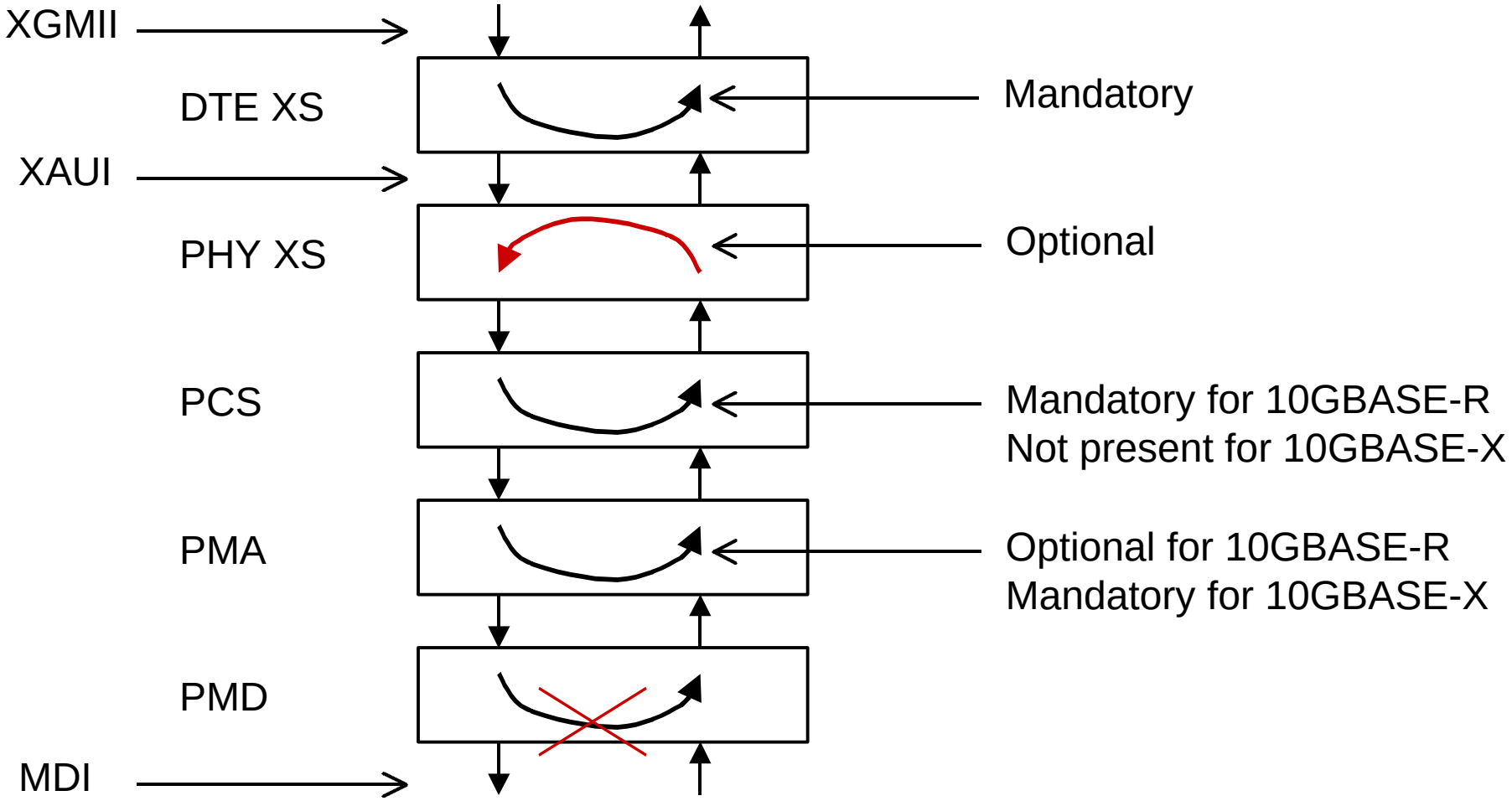
Fault signalling example



Fault signalling example



10GbE loopbacks



10GbE electrical specification

- V_{DD} = 1.2V typical
- Possible to use open drain drivers

Parameter	Minimum	Maximum
V_I	-0.3V	1.5V
V_{IH}	0.84V	
V_{IL}		0.36V
V_{OH}	1.0V	1.5V
V_{OL}	-0.3V	0.2V
I_O	4mA	

10GbE MDIO

- Backwards compatibility
  - Possible to integrate a Clause 22 PHY into a Clause 45 MMD and use the new electrical interface with the old frame format
- Optional
  - Not mandatory to implement MDIO – could provide access to registers using another interface

Summary

- New Indirect Address register access defined for 10GbE
- Opens up many more registers
  - 32 Ports
  - 32 MMDs per port
  - 65 536 Registers per MMD
- End-to-end fault signalling
  - Detailed diagnosis via register accesses
- Multiple loopback points defined
- New low voltage electrical specification