

IEEE P802.3cv D0p1 4-Pair PoE Maintenance 1st Task Force review comments

Cl 1 SC 1.4.502 P22 L4 # 4

Anslow, Pete Ciena
 Comment Type E Comment Status D

IEEE Std 802.3bt-2018 deleted definitions for VPD (1.4.502) and VPSE (1.4.503). This leaves unresolved cross references to the definition for VPSE in 33.2.6 and 33.2.7.4 and to the definition for VPD in 33.3.3.3.

SuggestedRemedy

Provide replacement wording for "as defined in 1.4.515" in the explanation of VPSE in 33.2.6 and 33.2.7.4
 Provide replacement wording for "as defined in 1.4.514" in the explanation of VPD in 33.3.3.3.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This definitions were already moved to 33.1.4 in CQ (page 18, lines 6-12).

We need to remove the references from the rest of Clause 33 or replace them with text that points to 33.1.4. This should be done in CQ.

TFTD

Cl 30 SC 30.9.2 P42 L2 # 3

Anslow, Pete Ciena
 Comment Type E Comment Status D

IEEE Std 802.3bt-2018 made changes to Clause 30 that deleted 30.9.2 "PD managed object class"
 Figure 30-3 there is a box containing "oPD 30.9.2" where 30.9.2 is a cross-reference to the deleted subclause.

SuggestedRemedy

Remove this box and its contents from Figure 30-3.
 Note that IEEE Std 802.3cg-20xx is making changes to Figure 30-3.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.6.3.3 P75 L4 # 1

Anslow, Pete Ciena
 Comment Type T Comment Status X

IEEE Std 802.3bt-2018 made changes to Clause 79 that deleted Equation (79-1) and Equation (79-2).
 In 33.6.3.3, there are four cross-references to Equation (79-1) and three cross-references to Equation (79-2).
 In 33.6.3.4, there is one cross-reference to Equation (79-1) and one cross-reference to Equation (79-2)

SuggestedRemedy

Replace the nine cross references with text defining how the values are derived.

Proposed Response Response Status W

TFTD

Cl 79 SC 79.3.2 P80 L4 # 5

Yseboodt, Lennart Signify
 Comment Type T Comment Status X Pres: Yseboodt2

A Type 3 and Type 4 device sending a Power via MDI TLV is required to send the Type 3 and Type 4 extensions. Many implementations (Type 1/2) incorrectly ignore fields that have an unexpected length.

We should permit new devices to fall back to the Type 1/2 field length in certain cases.

SuggestedRemedy

Adopt yseboodt_0919_02_lldp.pdf

Proposed Response Response Status W

TFTD

WFP

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Cl 79 SC 79.3.8.1 P93 L2 # 2

Anslow, Pete Ciena
 Comment Type T Comment Status D

Footnote a to Table 79-8a has an external cross-reference to "33.3.8.1", which does not exist.
 145.3.8.1 is "Input voltage" and the equivalent in Clause 33 is 33.3.7.1, so this may be what is meant, but there is no reference to VPort_PD-2P there.

SuggestedRemedy

Replace the external cross-reference to "33.3.8.1" with an external cross-reference to something that exists.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

We need to change the pointer and clarify that Vport_PD is in Clause 33 (not -2p)

Change to "The valid range of this field extends beyond the allowed operating range of Vport_PD or VPort_PD-2P; see 33.3.7.1 and 145.3.8.1."

Cl 145 SC 145.2.5.1 P118 L3 # 6

Yseboodt, Lennart Signify
 Comment Type T Comment Status D

"When this occurs, the PSE shall back off for at least T dbo as defined in Table 145-16 before attempting another detection, except in the case of an open circuit as defined in 145.2.6.5. During this backoff, the PSE shall not apply a voltage greater than V Off to the PI."

These two requirements only mean something when parsed together, it makes no sense for this to be two separate requirements as discovered when writing a test plan for this specification.

SuggestedRemedy

Replace two sentences by:
 "When this occurs, the PSE shall not apply a voltage greater than V Off to the PI for at least T dbo as defined in Table 145-16 before attempting another detection, except in the case of an open circuit as defined in 145.2.6.5."
 Update PICS.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 145 SC 145.2.5.1 P118 L4 # 7

Yseboodt, Lennart Signify
 Comment Type E Comment Status D

There are three instances of "Connection Check" capitalized thus.

SuggestedRemedy

Change to "Connection check" or "connection check" as appropriate on
 - page 118, bottom
 - page 120, CC_DET_SEQ, value 0
 - page 135, do_cxn_chk, first sentence

Proposed Response Response Status W

PROPOSED ACCEPT.

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Cl 145 SC 145.2.5.7 P142 L4 # 8

Yseboodt, Lennart Signify
 Comment Type T Comment Status X
 Comment by David Law.

Assuming the other necessary conditions are present, both the Figure 145-14 'PSE Autoclass state diagram' and the Figure 145-41 'PSE DLL Autoclass control state diagram' transition from IDLE_ACS to MEASURE_ACS_DLL and from IDLE to MEASURE respectively as a result of MirroredPDAutoclassRequest becoming true.

The exit condition from the state MEASURE in Figure 145-41 is do_autoclass_measure_done. According to subclause 145.2.5.6 'Functions' 'The variable formed by the function name appended with "_done" is used to indicate when the function has completed.'. More importantly it then state 'This variable is set to FALSE when the function is called and is set to TRUE once the function is complete and its output variables are valid.'. I will assume this applies to all functions in IEEE P802.3bt. Based on that do_autoclass_measure_done is TRUE until the MEASURE_ACS_DLL state is entered in Figure 145-14 where the do_autoclass_measure function is called.

And this is where the race condition exists since we assume all transitions are instantaneous. The variable do_autoclass_measure_done is TRUE, at some point MirroredPDAutoclassRequest becomes TRUE. At that instant Figure 145-41 transitions to MEASURE and tests the do_autoclass_measure_done viable to see if it is TRUE, at that same instant Figure 145-14 transitions to MEASURE_ACS_DLL, calls the do_autoclass_measure function which sets the do_autoclass_measure_done viable FALSE. It isn't clear to me what state the do_autoclass_measure_done viable is in when tested by the Figure 145-41 state diagram. If it were to see it TRUE, Figure 145-41 will then signal to the PD that the autoclass is complete, even though it hasn't even started.

SuggestedRemedy

Problem confirmed, resolution to be provided at the meeting.
 (aka. I don't know how to fix it right now)

Proposed Response Response Status W
 TFTD

Cl 145 SC 145.2.5.7 P143 L1 # 9

Yseboodt, Lennart Signify
 Comment Type T Comment Status X
 Comment from David Law.

I noted an issue when I ran a simulation of a dual signature PD connected to a PSE, where the PSE has sufficient power for primary Alternate (Alternate A), but not for secondary Alternate (Alternate B). As a result the PSE denies power on secondary Alternative. After denying power on the secondary Alternate, the PSE cycles through IDLE_SEC however PD remains stuck in the DO_MARK_EVENT3 state on Mode B. As a result the PSE detects an invalid signature on the secondary Alternate, and then cycles through IDLE_SEC, START_DETECT_SEC and DETECT_EVAL_SEC continually while the PD remains in the DO_MARK_EVENT3 state.

The reason for this is that the PD is not seeing a voltage to take it out of classification on Alternative B. Now I note that subclause 145.2.10.11 'Turn off voltage' states that 'The voltage at the PI shall be equal or less than VOff, as defined in Table 145-16, when the PSE is in DISABLED, IDLE, BACKOFF, or ERROR_DELAY. The voltage at the corresponding pairset shall be equal or less than VOff, as defined in Table 145-16, when the PSE is in IDLE_PRI, WAIT_PRI, ERROR_DELAY_PRI, IDLE_SEC, WAIT_SEC, or ERROR_DELAY_SEC.' however the duration in the IDLE_SEC state isn't sufficient for the VPSE to reach VOff (less than or equal to 2.8V) which would bring the PD back to the IDLE state on the secondary Alternative.

I wondered why I hadn't seen a similar issue with a single signature PD, but the reason for this is an additional requirement to subclause 145.2.10.11 found in subclause 145.2.8.1 'PSE Multiple-Event Physical Layer classification' that reads 'If the PSE returns to IDLE, it shall maintain the PI voltage in the range of VReset for a period of at least TReset min before starting a new detection cycle.'. The time delay TReset ensure that VPSE reaches and remains at VReset (less than or equal to 2.8V) for a sufficient time to return the PD back to the IDLE state.

It is not clear to me if the 145.2.10.11 'Turn off voltage' requirement that the voltage at the PI shall be equal or less than VOff for the listed states means that the state cannot be exited until that voltage is reached at the PSE PI. And even if that is the requirement, if the PSE PI isn't held at that voltage for a period of time, reaching VOff and then immediately starting to increase again, as would occur on exit from IDLE_SEC to START_DETECT_PRI, may not result in a transition below the classification reset voltage VReset_PD.

As an aside I also noted that there isn't an equivalent to pse_ready (an implementation-dependent manner to probe the link segment) for the individual PSE Alternates. As a result, in this particular situation, the dual-signature semi-independent PSE state diagrams require the PSE to continue to perform detection and classification on the secondary Alternate even though the PSE has just denied power on that Alternative because it has insufficient power.

Lennart: issue confirmed.

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SuggestedRemedy

What we're missing is a requirement to reset the pairset whenever the state machine goes through the dual-sig IDLE states.

After the sentence "If the PSE returns to IDLE, it shall maintain the PI voltage in the range of V Reset for a period of at least T Reset min before starting a new detection cycle." on page 162, add the following:
 "If the PSE returns to IDLE_PRI or IDLE_SEC, it shall maintain the PI voltage on the corresponding pairset in the range of V Reset for a period of at least T Reset min before starting a new detection cycle."

We are now describing state diagram behavior in text, this requires at least introduction of pse_ready_pri and pse_ready_sec to make this work.

Add both of those variables to 145.2.5.4 with appropriate text copied from pse_ready.

Further, change the condition from IDLE_PRI to START_DETECT_PRI to read:
 pse_ready_pri * !pwr_app_pri * pwr_app_sec

And from IDLE_SEC to START_DETECT_SEC:
 pse_ready_sec * (!pwr_app_sec * pwr_app_pri) + (option_probe_alt_sec * !det_start_pri * !det_once_sec * !alt_pwrd_pri)

Proposed Response *Response Status* **W**
 TFTD

Cl 145 **SC 145.2.8.1** **P157** **L3** # **10**

Yseboodt, Lennart Signify
Comment Type **T** *Comment Status* **X** *Pres:* Yseboodt1

When we designed the Autoclass mechanism that allows a PSE to learn about the maximum required power budget I forgot to deal with an important corner case that makes it impossible for a PD to draw the maximum power as it is required to. Currently this would result in a Class 1 power allocation.

SuggestedRemedy

Adopt yseboodt_0919_01_autoclass.pdf

Proposed Response *Response Status* **W**
 TFTD

WFP

Cl 145 **SC 145.2.8.1** **P157** **L4** # **11**

Yseboodt, Lennart Signify

Comment Type **T** *Comment Status* **D**

There is a type in Equation 145-4, "VPort_PSE-2p min" where "-2P" should be capitalized.

SuggestedRemedy

Fix.

Proposed Response *Response Status* **W**
 PROPOSED ACCEPT.

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Cl 145 SC 145.2.8.1 P159 L3 # 12

Yseboodt, Lennart Signify
 Comment Type T Comment Status D

Comment from David Law.

I note that subclause 145.2.8.1 'PSE Multiple-Event Physical Layer classification' includes the statement that 'If any measured IClass is equal to or greater than IClass_LIM min, a PSE shall return to IDLE.'

Since IClass_LIM min is defined as 0.051 mA, this implies no margin, if IClass is 0.051 ma - 1nA the PSE shall not return to IDLE, if IClass is 0.051 ma + 1nA the PSE shall return to IDLE.

Table 145-13 'Class signatures evaluated at the PSE PI' however defines > 45 mA and < 51 mA as 'Either class signature 4 or invalid class signature' and iclass_lim_det, iclass_lim_det_pri and iclass_lim_det_sec which are 'open arrow' entries to their respective state diagrams are defined as 'A variable indicating if any IClass measured by the PSE during do_classification is invalid or equal to or greater than IClass_LIM min'. As a result there appear to be some differences between PSE operation when connected to a single signature PD compared to when connected to a dual signature PD in respect to IClass limits when connected to a single signature PD compared to when connected to a dual signature PD.

For a PSE connected to a single signature PD, once the chosen threshold between > 45 mA and < 51 mA for Iclass is exceeded, iclass_lim_det is set TRUE forcing the open arrow entry in to the Figure 145-13 IDLE state. Since this threshold is < 51 mA, if Iclass then reaches 51 mA the subclause 145.2.8.1 requirement to return to IDLE are already met. Hence reaching or exceeding 51 mA does not result in different behaviours when the PSE is connected to a single signature PD.

For a PSE connected to a dual signature PD, once the chosen threshold between > 45 mA and < 51 mA for Iclass is exceeded on a particular alternative either iclass_lim_det_pri or iclass_lim_det_sec will be set TRUE. This will then force an open arrow entry in either Figure 145-15 or Figure 145-16 in to the IDLE_PRI or IDLE_SEC state respectively. But this will not result Figure 145-13 entering the IDLE state. Nor will it prevent the other alternative from powering up, assuming correct behaviour on that alternative.

If however Iclass reaches exactly 51 mA (with no margin) on a particular alternative, the subclause 145.2.8.1 requirement means that Figure 145-13 has to return to the IDLE state. This will cause sism to be set to FALSE resulting in both Figure 145-15 and Figure 145-16 returning them to the IDLE_PRI and IDLE_SEC states respectively. Hence reaching or exceeding 51 mA does result in different behaviours when the PSE is connected to a dual signature PD.

SuggestedRemedy

This made my head hurt.
 These conflicts are the result of us describing state diagram behavior in the text.

The desired behavior is already fully encoded in the state diagram, we do not need a conflicting text requirement.

On page 162, change the following text:
 "If any measured I Class is equal to or greater than I Class_LIM min, a PSE shall return to IDLE. The PSE shall limit class event currents to I Class_LIM and shall limit mark event currents to I Mark_LIM ."

to read:
 "If any measured I Class is equal to or greater than I Class_LIM min, a PSE returns to IDLE, IDLE_PRI, or IDLE_SEC as appropriate.
 The PSE shall limit class event currents to I Class_LIM and shall limit mark event currents to I Mark_LIM ."

Update PICS.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

Cl 145 SC 145.3.3.3.5 P187 L2 # 13

Yseboodt, Lennart Signify
 Comment Type T Comment Status D

An Autoclass enabled PD, when connected to a Type 1/2 PSE is still bound by all the Autoclass rules when in POWER_ON, even though the PSE does not know what Autoclass is. There is no need for this, in this case the PD should be allowed to simply forget about Autoclass.

SuggestedRemedy

In Figure 145-25, state DO_CLASS_EVENT_AUTO, change the statement "pd_acs_req <= True" to read:
 "pd_acs_req <= long_class_event".

Note: that statement is correct, but takes a bit to figure out. Reason to use this in stead of a more readable IF statement is not to have to redraw a substantial portion of this state diagram. Trust me: it's cramped.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

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Cl 145 SC 145.3.3.4.5 P194 L2 # 14

Yseboodt, Lennart Signify
 Comment Type T Comment Status D

Comment by David Law.

There is a typo in the dual-sig PD state diagram in Figure 145-27.
 In the POWERED state, in the assignment $pd_max_power_mode(X) \leq \min(pse_assigned_class(X), pd_req_class_mode(X))$. I assume that $pse_assigned_class(X)$ is a typo and should be $pse_assigned_class_mode(X)$.

SuggestedRemedy

Change:
 - in Figure 145-27, POWERED STATE, change the first statement to read:
 $pd_max_power_mode(X) \leq \min(pse_assigned_class_mode(X), pd_req_class_mode(X))$

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

Cl 145 SC 145.5.3.2.5 P234 L4 # 15

Yseboodt, Lennart Signify
 Comment Type T Comment Status D

Comment by David Law.

I noticed a couple of typos in relation to Figure 145-42 'PSE power control state diagram for dual-signature PDs in 4-pair mode'

On the transition from PSE_POWER_REVIEW to RUNNING the equation is
 $(pse_new_value_alt(X) \geq PSEAllocatedPowerValue_alt(X)) * (PSEAllocatedPowerValue_alt() [?] MirroredPSEAllocatedPowerValueEcho_alt(X))$. I assume that $(PSEAllocatedPowerValue_alt())$ is a typo and should be $(PSEAllocatedPowerValue_alt(X))$.

SuggestedRemedy

Change:
 - in Figure 145-42, from PSE_POWER_REVIEW to RUNNING, change to:
 $(pse_new_value_alt(X) \geq PSEAllocatedPowerValue_alt(X)) * (PSEAllocatedPowerValue_alt(X) \neq MirroredPSEAllocatedPowerValueEcho_alt(X))$

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

Cl 145C SC 145C.3 P288 L2 # 16

Yseboodt, Lennart Signify
 Comment Type T Comment Status X

Comment by Jason Tuenge.

This unbalance current requirement applies at the PSE PI connector (jack) when mated with a specified balanced cabling connector (plug).

[...]

The unbalance current requirements for PDs apply at the PD PI connector (jack) when mated with a specified balanced cabling connector (plug).

[...]

145C.3 Direct current resistance (DCR)

The maximum conductor DCR of 12.5 O in Figure 145C-1 and Figure 145C-3 is derived from a cabling topology consisting of:

- 90 meters of 24 AWG horizontal cable (0.0938 O/m),
- 10 meters of 26 AWG patch cord (0.14 O/m),
- four inline connectors (0.3 O per connector).

Would your understanding be that this assumes two cords (and two connections), or four cords (and four connections)?

If the latter, seems "connector" and "connection" are being used interchangeably... And in any case, the above math would yield 11 O (not 12.5 O).

SuggestedRemedy

Input needed from mr. Diminico, at the very least the math indeed does not check out.

Proposed Response Response Status W
 TFTD