IEEE 802.3 Interpretations Report

July 21st, 2005
San Francisco, CA

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Interpretations Status

- Interpretations Ad Hoc met Wednesday
- 3 interpretations considered

  1-07/05 - DTE Power via MDI Isolation

  2-07/05 - Auto-Negotiation

  3-07/05 - PME Aggregation restrictions

  Available on Interpretations area of web site

  HTTP://www.ieee802.org/3/interp/index.html

IEEE-SA Standards Companion Text on interpretations

- Interpretations are a unique form of commentary on the standard. They are not statements of what the standard should have done or meant to say. Interpretations cannot change the meaning of a standard as it currently stands. Even if the request points out an error in the standard, the interpretation cannot fix that error. The interpretation can suggest that this will be brought up for consideration in a revision or amendment (or, depending on the nature of the error, an errata sheet might be issued).

- However, an interpretation has no authority to do any of this. It can only discuss, address, and clarify what the standard currently says. The challenge for the interpreters is to distinguish between their expertise on what 'should be,' their interests in what they 'would like the standard to be,' and what the standard says. Interpretations are often valuable, though, because the request will point out problems that might otherwise have gone unaddressed.

- http://standards.ieee.org/guides/companion/part2.html#interpret

Request 1-07/05

I have some problems to understand the meaning of clause 33.4.1 (Isolation) of IEEE802.3af-2003.

Example:

There is a six port switch including a PSE to provide power via MDI and an inband management (IP) for configurations and status informations. The entire device has only one connector for external power supply (48Vdc) and six twisted pair ports for the ethernet.

Q1:
Where is the isolation required?

Q2:
Must the CPU and the switch inside the device isolated from the PSE controller?

Q3:
What is the meaning of "PI device circuits"? Does it means only the 48V power supply, the PSE controller and the FET´s?

Q4:
How do I isolate the PI leads from the PI device circuits like the PSE controller? The PI leads are directly connected to the FET and the PSE controller.

Request 1-07/05 (cont)

33.4.1 Isolation

The PSE shall provide electrical isolation between the PI device circuits, including frame ground (if any), and all PI leads.

1-07/05 proposed responses

Q1: **Unambiguous**

The standard states in the first paragraph of subclause 33.4.1 'Isolation' that ‘The PSE shall provide electrical isolation between the PI device circuits, including frame ground (if any), and all PI leads.’.

Q2, 3 and 4: **Not request for interpretation**

These items of the request are being returned to you because they do not constitute a request for interpretation but rather a request for consultation advice. Generally, an interpretation request is submitted when the wording of a specific Clause or portion of the standard is ambiguous or incomplete. The request should state the two or more possible interpretations or the lack of completeness of the text.

The definition of PI devices circuits is ambiguous and a corrigendum project has been requested to address this area of the IEEE Std 802.3 standard [add URL].

Request 2-07/05

Interpretation Request

I am debating with a colleague the validity of configuring a 10/100/1000 Ethernet port for fixed 1000Mb full-duplex operation. Is this permissible? I have seen interpretations that it is permissible to configure a port for fixed 1000Mbps operation and interpretations that if auto-negotiation is disabled, fixed speed can only be set to 100Mbps or 10Mbps.

Standard: IEEE Std 802.3(tm)-2002
Section(s): 37 and 40.5.1 Support for Auto-Negotiation
Conditions: A physical Ethernet port is capable of operation at 10Mbps, 100Mbps, or 1000Mbps. Full-duplex operation is possible at all speeds. Half-duplex operation is available at 10 and 100Mbps. It is also possible to configure the port for auto-negotiation.

The question is, Is it permissible to configure a 10/100/1000 capable port for fixed, full-duplex operation at 1000Mbps when auto-negotiation is disabled?

2-07/05 proposed response - Unambiguous

This interpretation is asking two specific questions, one pertaining to 1000BASE-X operation and one pertaining to 1000BASE-T operation.

Duplex configuration during 1000BASE-X operation can be handled either through Auto-Negotiation or through manual selection using the defined registers in clause 22. If manual configuration is used by disabling Auto-Negotiation in MII register 0.12, the duplex operation mode would be selected by bit 0.8. If Auto-Negotiation is enabled duplex configuration is controlled by the exchange of /C/ ordered sets. By definition speed selection is not possible through Auto-negotiation in 1000BASE-X operation.

Speed, Duplex, and MASTER/SLAVE configuration during 1000BASE-T operation, are determined through the Auto-Negotiation process. Clause 40.5.1 states:

“All 1000BASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE. Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for the following two primary purposes for 1000BASE-T:

a) To negotiate that the PHY is capable of supporting 1000BASE-T half duplex or full duplex transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.
This relationship is necessary for establishing the timing control of each PHY. The 1000BASE-T MASTER PHY is clocked from a local source. The SLAVE PHY uses loop timing where the clock is recovered from the received data stream."

Clause 40.5.2 MASTER/SLAVE states that the MASTER/SLAVE relationship shall be determined using Auto-Negotiation:

"The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–13.)"

This indicates that although operating speed is allowed to be manually selected by disabling Auto-Negotiation in Control Register 0, selecting 1000BASE-T mode of operation still requires that Auto-Negotiation be used. This can be accomplished by continuing to use Auto-Negotiation while limiting the advertising to 1000BASE-T capabilities.

Request 3-07/05

Interpretation Request

Standard: Std 802.3ah-2004
Section: 61.2.2.5: PME Aggregation Restrictions

Question:
The above section defines the term "differential latency" as the number of bits, N , that can be sent across the fast link in the time it takes one "maxFragmentSize" fragment to be sent across the slow link. In the next page it says that "maxFragmentSize"=512 octets, and that the maximum ratio between any tow links is 4. Combine it with the above statement, you get the value of 4*512=2048 octets = 16K bits for the maximal possible value of "differential latency". But in the next page, it says that the maximum value of "differential latency" should be 15000. How come?

Request 3-07/05 (cont)

3-07/05 proposed response - Unambiguous

There's no ambiguity in the text. The requirement for differential latency is 15000 bits.

IEEE 802.3 Motion

IEEE 802.3 approves the proposed Interpretation responses to Interpretation requests 1-07/05, 2-07/05 and 3-07/05 as presented without the need for a 30 day letter ballot.

M: Law S: Thaler Tech 75%/~~Proc 50%~~

PASSED/FAILED Date:

Y: 86 N: 0 A: 10 Time: