Proposal for 2.4-GHz PHY
July 1998 Update

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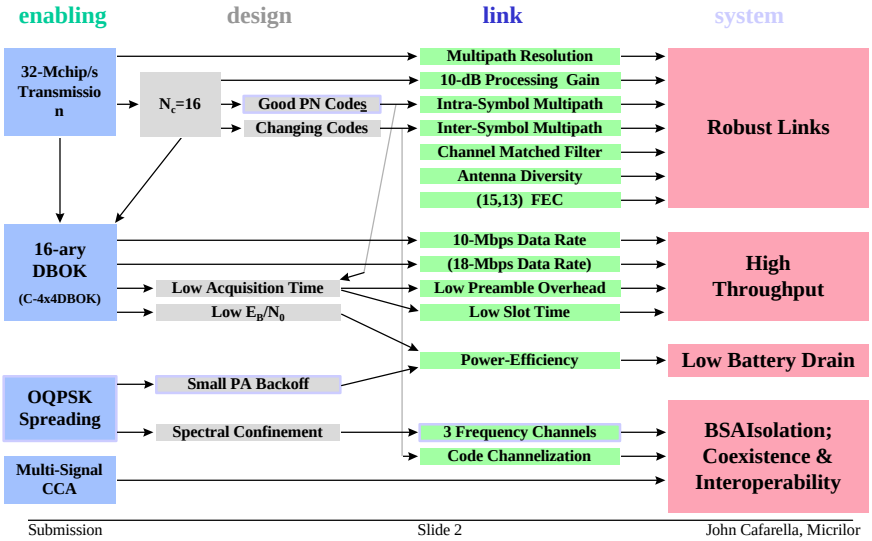
Key Features



Performance Matrix

	May	July
Processing Gain	≥12 dB	
Multipath Tolerance*	275 ns	360 ns
Basic Data Rate	10 Mbps	
Spin-up Rate (good channel)	18 Mbps	
Preamble Overhead	24 us	
Frequency Channels	2	3
Code Channels	48	1744
Chip Complexity	40K gates	
PA Backoff (10 mW PCMCIA)	~ 0 Db (MSK)	~ 2 dB (OQPSK)
Interoperate Legacy DSSS?	use CFI	CCA & Header
Interoperate Legacy FHSS?	- -	CCA & Header

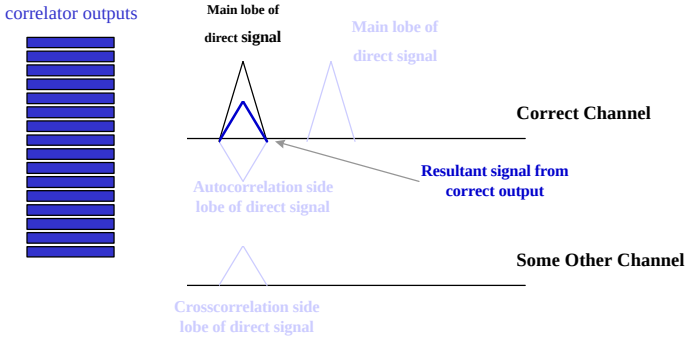
* 10 Mbps with Channel Matched Filter but no MLSE; MLSE could be added to strengthen 18 Mbps mode as technology upgrade

Select New PN Codes (cosets)

- 8 Cosets with Best Autocorrelation Side Lobes
  - Previously chosen for best full crosscorrelation
  - Autocorrelation side lobes are worse problem than crosscorrelation side lobes
- Increase Delay-Spread Tolerance to 360 ns
- Motivates Different Data-Code-Channel Sets
  - single code, 2 alternating or 4 alternating
  - 1744 total; 40 with “best” multipath tolerance

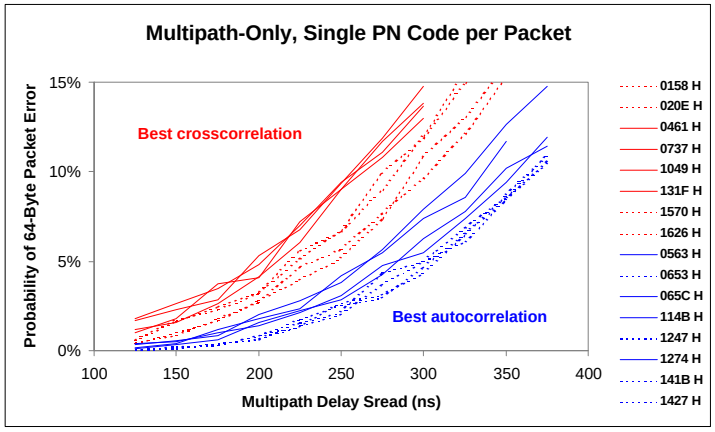
Coset definitions ref: Doc 97/117, Cafarella

Effect of Autocorrelation Side Lobe



A high autocorrelation side lobe can reduce the magnitude of the correct output, making is easier for a crosscorrelation side lobe in any incorrect channel to exceed the magnitide of the correct channel

Delay Spread Tolerance



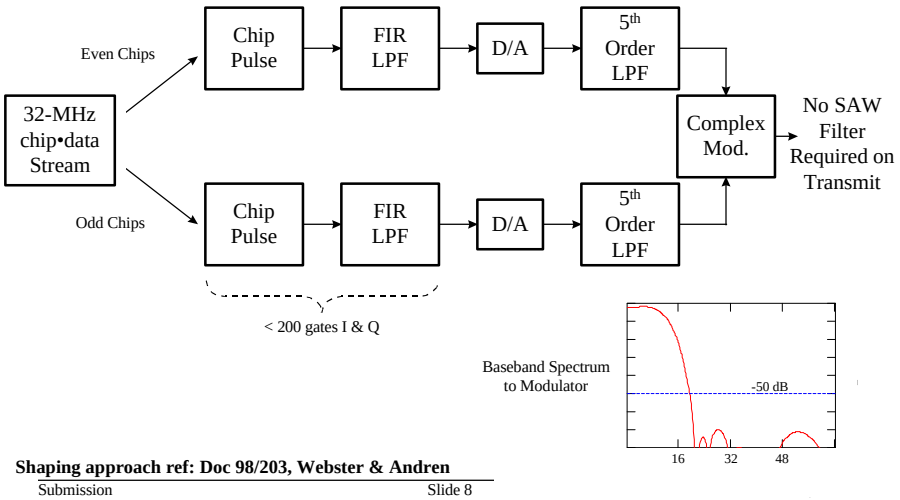
Previously reported 275 ns was average for "best crosscorrelation" codes

~~Channel matched filter ref: Doc 98/175, Boer~~

Three-Channel Operation

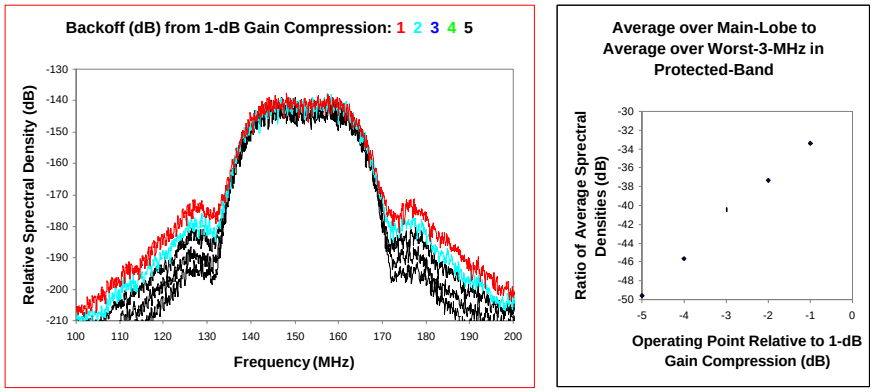
- 32-Mchip/s OQPSK Spreading Modulation
  - Reduce bandwidth while retaining 10-Mbps rate
  - Limits spectral re-growth in PA nonlinearity
- Suppress Spectral Side Lobes
  - Meet FCC protected band requirement
- Expand but "Square-Up" Main Spectral Lobe
  - Meet MKK 90%-energy bandwidth requirement
  - Achieve same 35-dB ACR as current 802.11

OQPSK Spreading



Shaping approach ref: Doc 98/203, Webster & Andren

Power Amplifier Backoff



100 mW Tx power requires almost 5-dB backoff,
but for 10-mW PCMCIA is closer to 2-dB

Interoperability

- Multi-Signal CCA for Legacy DSSS and FHSS
- Dual-Mode transceiver (exploit CCA circuitry)
  - High-rate DSSS plus Legacy DSSS or FHSS PHY
  - Transmit Legacy Header as Precursor to High-Rate DSSS
- Single PHY Solution
  - No need to coordinate Alternate High-Rate PHY Headers
  - Does not sacrifice high-rate throughput potential

Summary

- **Robust In Multipath & Interference**
- **Simple Hardware**
- **High Data Rate: 10 Mbps (+ 18 Mbps spin-up)**
- **Low Preamble Overhead for High Throughput**
- **3 Frequency Channels**
- **Code Channels For High System Capacity**
- **Interoperable with Legacy DSSS or FHSS**