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**Wireless Access Method and Physical Specification**

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Title: **Figures for Interleaver Proposal**

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This submission provides clarifying figures for the proposal made in 99/074 by Tal Kaitz and Naftali Chayat. The changes are made to the interleaver definition consistent with standard formats.

The D3.0 draft of Tga is not overly generous in describing the interleaver output to symbol mapping. The following figures which describe the modified interleaver ordering (figures 2 and 5) and appropriate text should be included in the draft to clarify the interleaver output to symbol mapping

Figure 1 illustrates the current interleaving with symbol mapping. The proposal in 99/047 and in my comment in LB16 is as shown in Figure 2 for 16QAM. There is a cyclic shift of 1 bit every other row to effectively interleave bits coming from LSB's and MSB's. Figures 3 and 4 show the current and proposed interleaving for 64QAM.

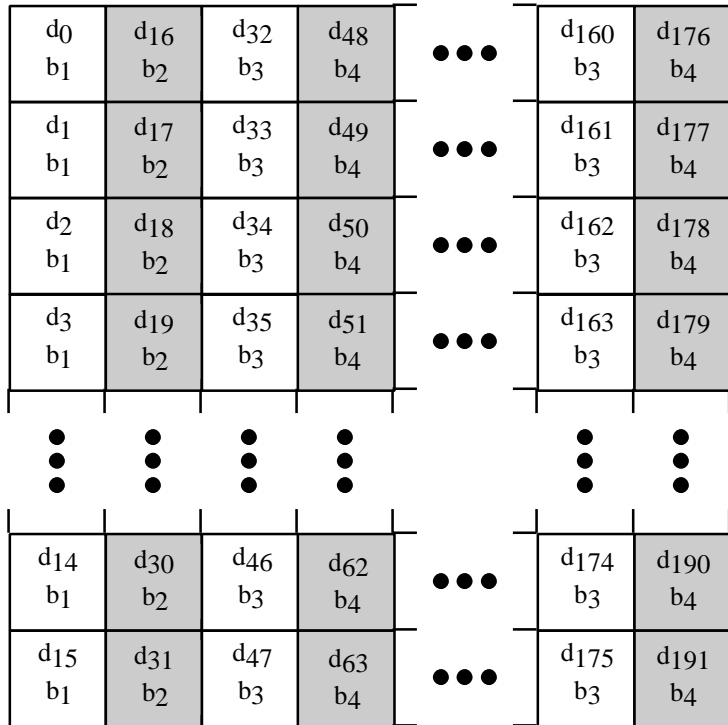


Figure 1. Current 16QAM interleaver with symbol mapping

where  $d_k$  = input bit stream with original ordering  $k$   
 $b_n$  =  $n^{\text{th}}$  bit of symbol as defined in Gray code mapping.

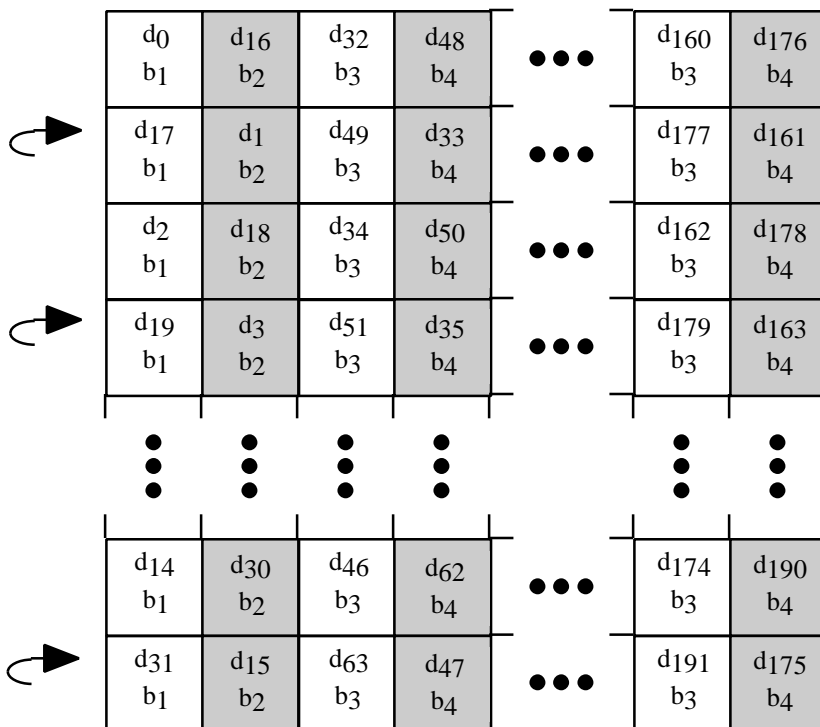


Figure 2. Modified 16QAM interleaver with cyclic shift.

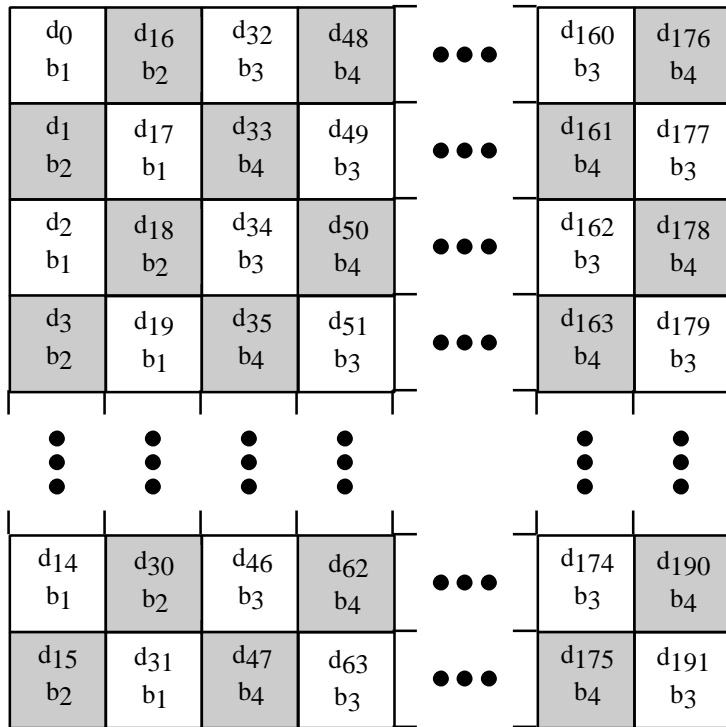


Figure 3. Modified 16QAM deinterleaver with cyclic shift removed.

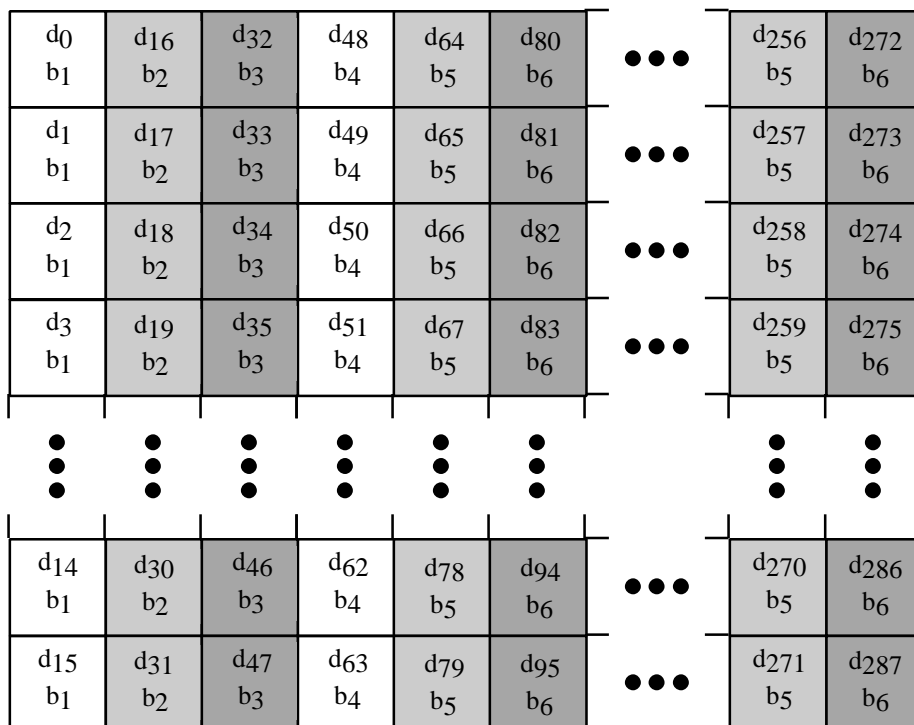


Figure 4. Current 64QAM interleaver with symbol mapping.

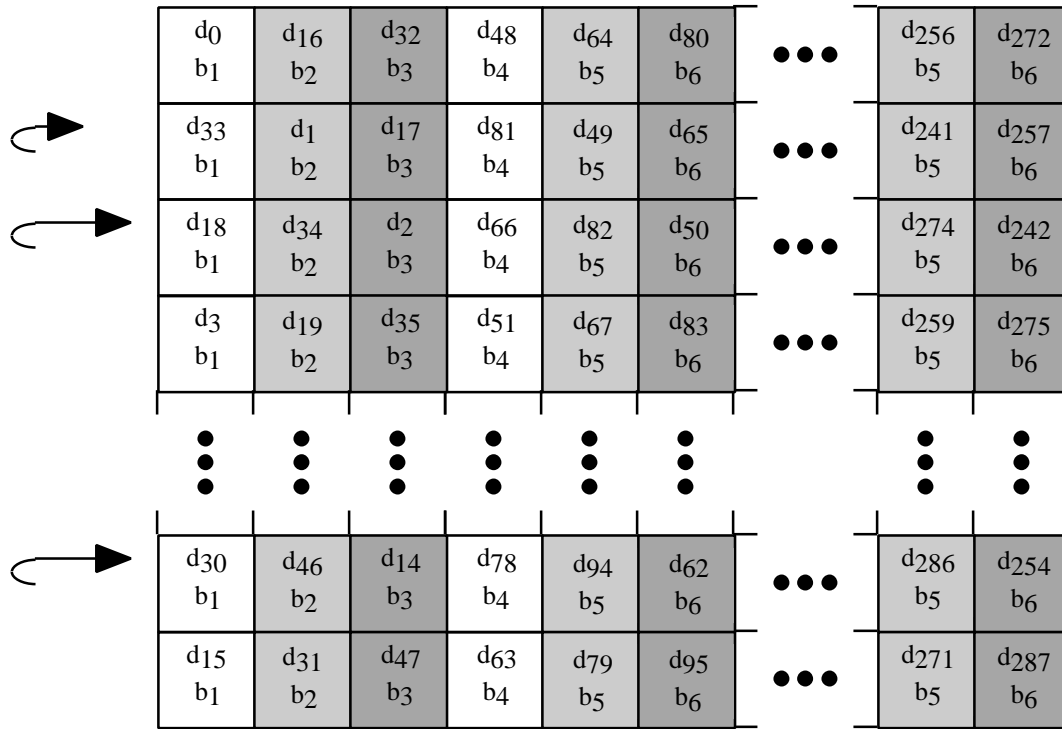


Figure 5. Modified 64QAM interleaver with cyclic shift.

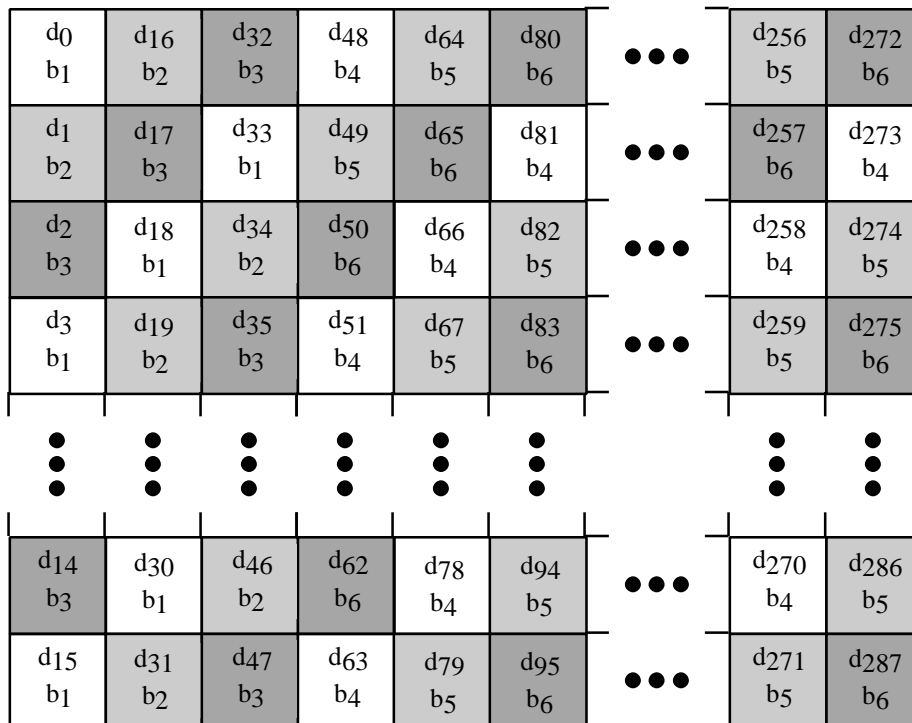


Figure 6. Modified 64QAM deinterleaver with cyclic shift removed