Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [Implementation Complexity of MB-OFDM Modem]
Date Submitted: [11 January, 2004]
Source: [Mark Rich] Company [Commstack]

Address [Commstack, 2635 N First St, Suite 224, San Jose, CA, 95134]
Voice:[+1 (408) 432-3066], E-Mail:[markr@commstack.com]

Re:

Abstract: [The following contribution provides an implementation complexity measurement for an MB-OFDM UWB system]

Purpose: [This document presents results of an implementation study on the complexity of MB-OFDM]

Implementation Complexity of an MB-OFDM Modem

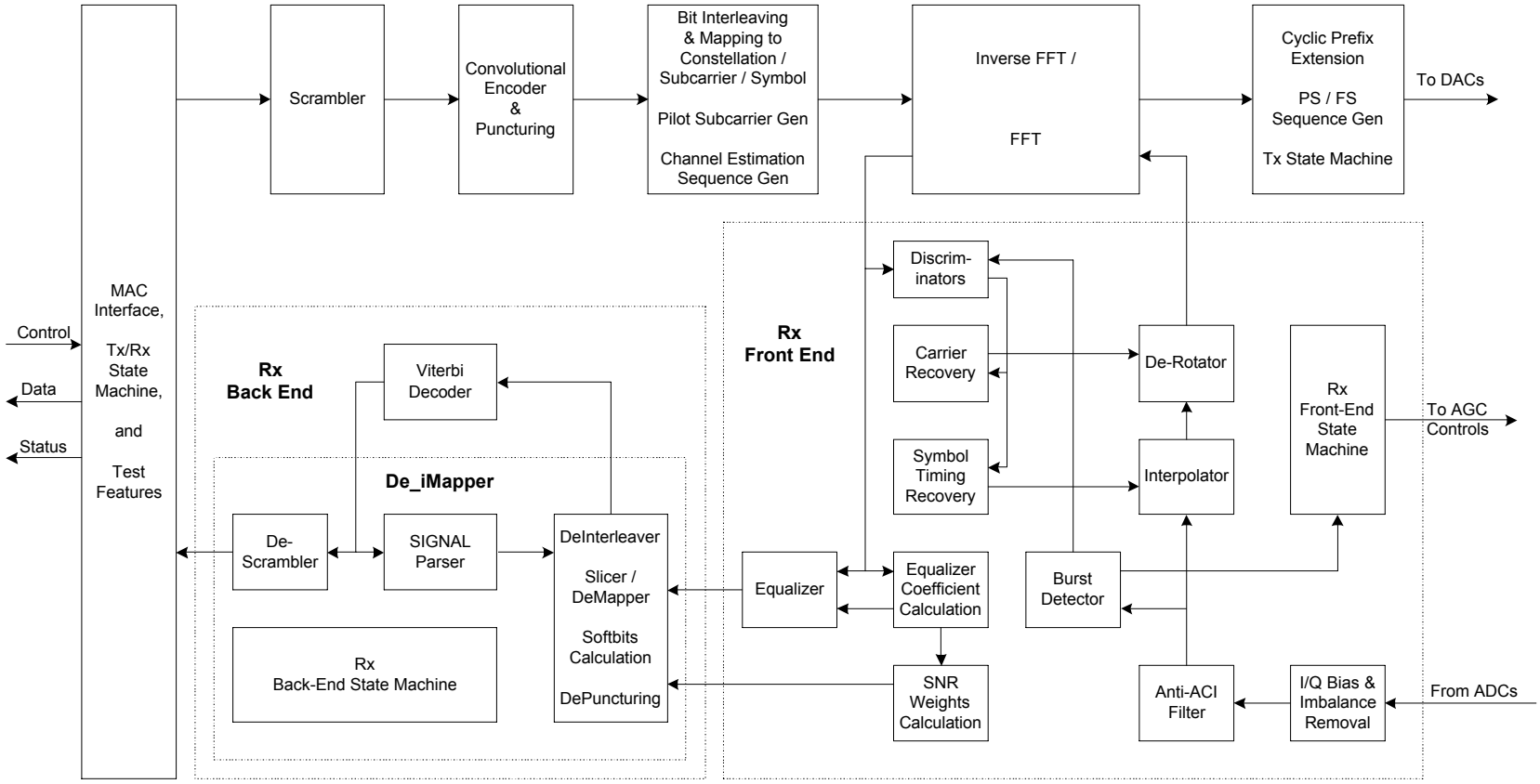
Mark Rich

Commstack
2635 N First St
Suite 224
San Jose, CA, 95134

Introduction

- Commstack has modified a Verilog implementation of an 802.11a OFDM modem to meet the July, 2003 MB-OFDM submittal
- The code is being tested in an Altera Stratix FPGA at approximately 1/4 clock speed
- This presentation documents the performance and complexity of the Verilog code that would be used to develop an MB–OFDM ASIC baseband processor.

Baseband Processor Block Diagram



Demonstration Details

- Verilog compiled for Altera EP1S80 Quartus II (v3.0)
- Performance is shown on a Stratix DSP development board
- Development board includes ADCs (12 bits-125 Msps) and DACs (14 bits-165 Msps)
- Samplerate is limited to 120/160 MHz by ADC/DAC,
- ASIC would use a 528 MHz clock
- FPGA implementation uses 6 bits at ADC/DAC; ASIC would require 5-6 bits resolution
- Internal processing uses 8 bits for both FPGA and ASIC

Design Details

- Interleaving
  - Across three symbol periods
- FFT/IFFT
  - 128 point FFT
  - Common logic used for both forward and reverse
- Acquisition and Tracking
  - Zero IF, Parallel Carrier and Timing Acquisition
  - Selectable aiding of timing loop by carrier loop
- Equalization
  - Band unique equalization coefficients
- Filtering
  - Reduced FFT requirements by up-sampling clock in TX filter
- Viterbi Decoder
  - Length 126 traceback

Complexity of major components

Component	Compiled Size (LEs)	Typical Clock Rate in Stratix FPGA	Memory (bits)
Transmit Chain	1800 LEs	200 MHz	3400
FFT/IFFT	4100 LEs	150 MHz	14500
Receiver Front End	8300 LEs	150 MHz	42000
Receiver Back End	1800 LEs	150 MHz	14400
Viterbi Decoder	2800 LEs	150 MHz	48000
MAC interface + test	1800 LEs	180 MHz	40000
Total	**20,600 LEs**	**150 MHz**	**162300**

- Optimization efforts are on-going, expect improvements in clock rate and gate count
- Altera Logic Elements (LE) is conservatively 15 ASIC gates
- Clock rates are compiled for –6 speed grade, expect 20% increase for –5 part

Conclusion

- Commstack has completed Verilog code suitable for ASIC integration
- 4x speed increase required for ASIC implementation
  - Easily accomplished in conventional CMOS processing
- Expect 300k gates ASIC MB-OFDM baseband processor