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Re:	IEEE P802.16-2004/Cor1-D1
Abstract	Correct the misfortunate combination of interleaver and permutation
Purpose	Adopt changes
Notice	
Release	
Patent Policy and Procedures	

Problem in Interleaver and Permutation Combination in OFDMA

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1. Motivation

The interleaver definition with d=16 might cause a performance degradation in some cases, due to a disastrous combination of interleaving and permutation. This is because, in OFDMA, the permutation actually performs an "interleaving like" operation, which partially reverse the current interleaver operation. This performance degradation occurs with burst allocations having low frequency diversity, for example bursts allocated to a single sub-channel. In these cases, adjacent coded bits might be transmitted on the same sub-carrier. Thus the interleaver operation becomes useless.
Simulation results show, in a worst case scenario, a degradation of about 4 dB at BER of 10^-4, with the current interleaver compared to interleaver bypass scheme. It is unreasonable to use an interleaver which might cause severe performance degradation in some cases, whereas it is supposed to improve the performance.

Thus, we propose modifications to both interleaving scheme and permutation to allow equal (better) performance to all burst allocations.

2. Contents

3. Details

For an interleaver with dimension d, a pair of adjacent coded bits before the interleaver is separated after the interleaver by distance Ncbps/d bits. If a FEC block spans more than one slot duration, then several bits from the same FEC block are transmitted on each sub-carrier. These bits are distributed in the FEC block periodically, where the period equals the number of bits in a single symbol divided by the distance.

With the current interleaver dimension d = 16, for a worst case scenario (DL PUSC, burst allocation of 1 sub-channel, 4 slots in a FEC block, QPSK constellation) this period can be as small as 2 bits !! This example is depicted in Figure 1 where the numbers in brackets are the indices of the coded bits before the interleaver.

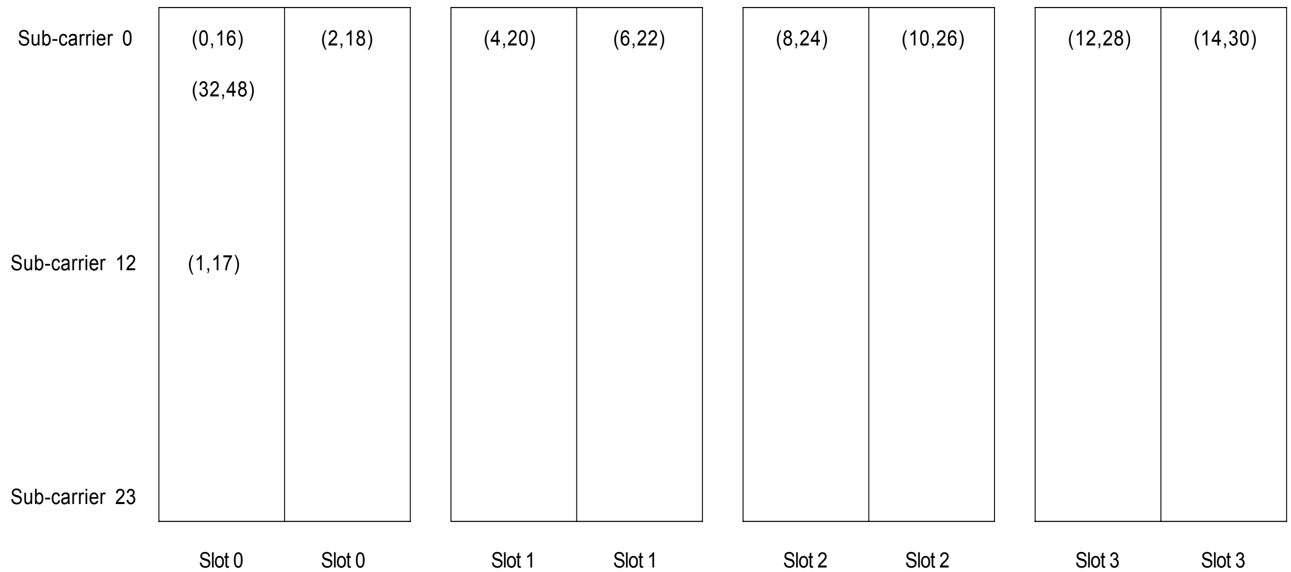


Figure 1: Worst case scenario of permutation-interleaver combination

The reason for this is that the order of subcarriers passed to the de-interleaver (in the receive side) is not a linear frequency-domain order (which the interleaver was designed for), but an arbitrary order. This order depends on the permutation, on the way the 48 logical subcarriers are mapped to physical subcarriers, on the in-slot rotation between subchannels, and on the way the slots are aggregated. The following figure shows the correlation structure in a FEC block on which the de-interleaver works (and of which the interleaver is unaware):

Similar colors mean high correlation (of fading):

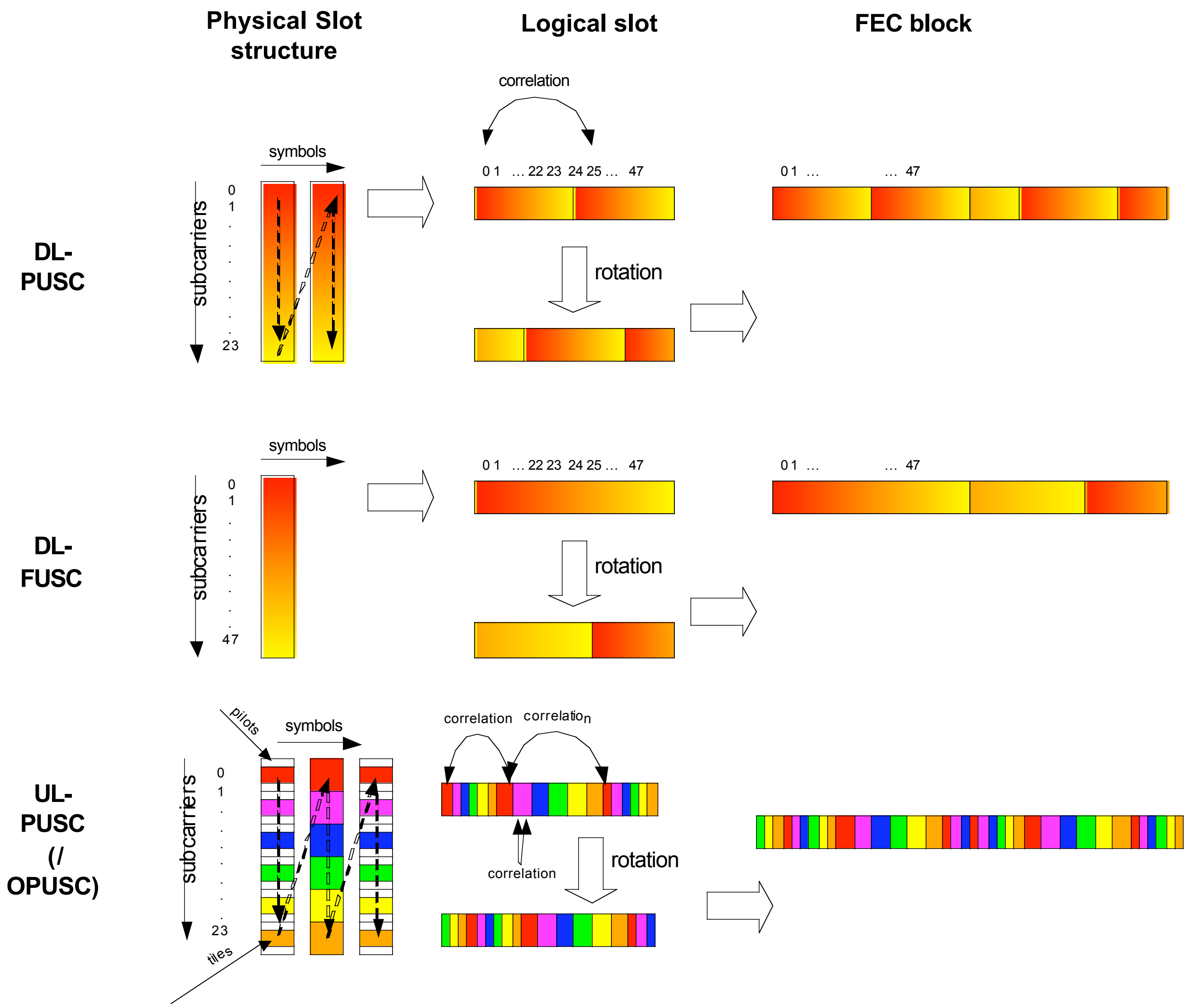


Figure 2: Example of correlation in slot and FEC block

The seemingly "random" structures of correlations in the FEC block are processed by the de-interleaver and create another "seemingly random" correlation structure at the input to the decoder. However, since these sequences are repetitive and not random, there are misfortunate choices of FEC block size for each permutation that create high correlations and reduce the performance significantly.

Our target is to first make this correlation structure similar between permutations, and correct the interleaver or the slot aggregation to solve this problem.

4. Simulation results

Example of out simulation results are given in the following, more results are in the appendices.

4.1. Downlink

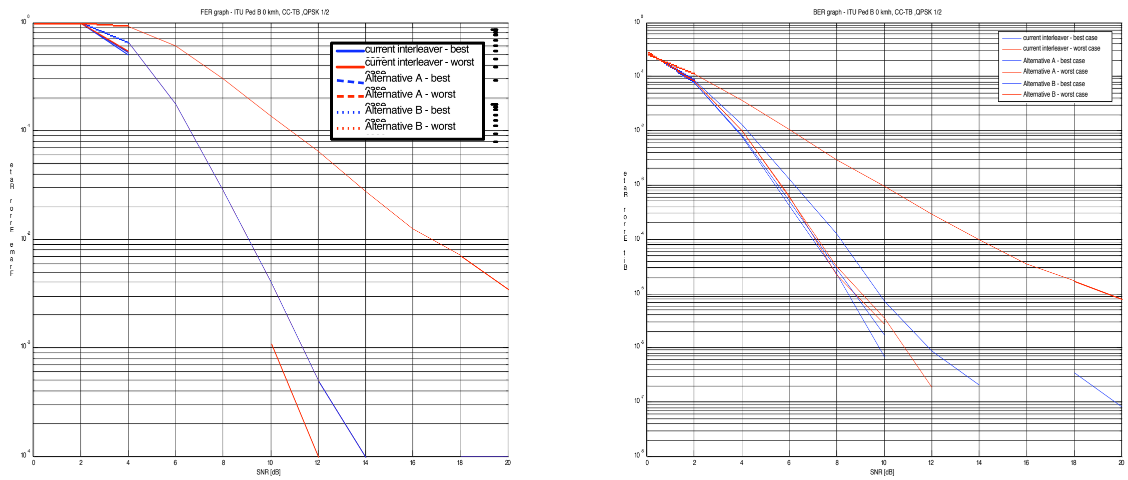
In the simulations below we simulated two cases:

1. best case – FEC blocks with 6 slots mapped over 5 sub-channels

2. worst case – FEC blocks with 4 slots mapped over 1 sub-channel

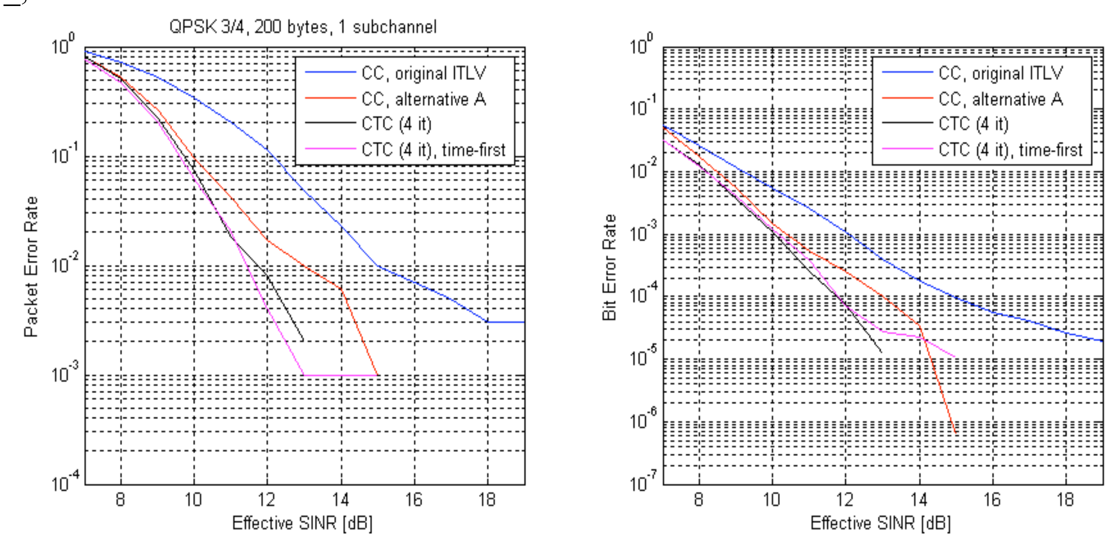
The best/worst case are in terms of distance between bits after interleaving and permutation. In worst case, each other bit at encoder output is mapped to a subcarrier with the same frequency.

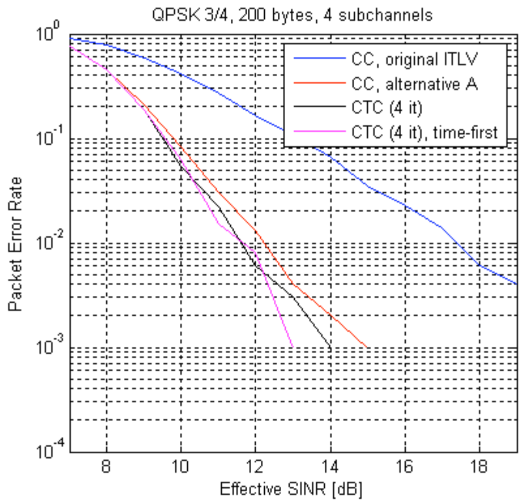
CC, QPSK _

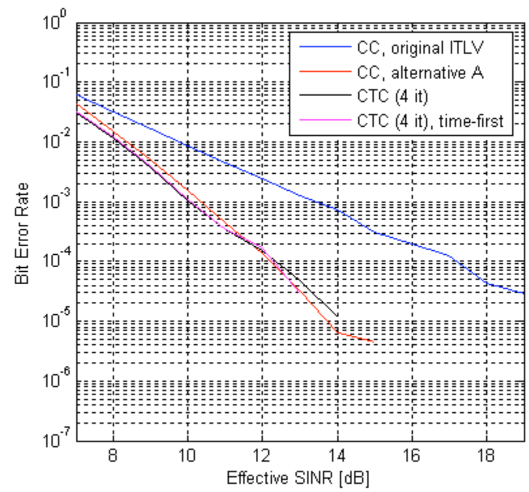


4.2. Uplink

QPSK _, 4 slots/FEC block







5. Changes summary

We present two alternatives, which are summarized in the following table:

	Alternative A	**Alternative B**
Interleaver dimension UL	6N	6
Interleaver dimension DL	12N	12
PUSC time first	+	+
Sub-channel reordering	k+48*n (Stays the same)	k*N+(n-k)modN
In-slot rotation (n+13*s)	Stays the same	Remove
Repetition	Stays the same	Should be changed

where

N – number of allocated slots per FEC block

k – sub-carrier index

n – slot index

5.1. Changes relevant to both alternatives

Both alternatives utilize mapping of the data sub-carriers inside a slot in time-first order, instead of frequency first order. This mapping is relevant to DL PUSC and UL PUSC. By doing so, all permutations (namely: FUSC, DL PUSC and UL PUSC) can be treated the same by the interleaver. The logical subcarriers 0..47 have decreasing order of correlation for subcarriers that are further apart.

5.2. Alternative A

Change the interleaver dimension to be dependent on the number of slots in FEC block (N). Specifically, the interleaver dimension in the UL is 6N, and in the DL is 12N. With these interleaver dimensions the distance between 2 adjacent coded bits is 4 sub-carriers in the DL and 8 sub-carriers in the UL, i.e. 2 adjacent coded bits in the UL resides in 2 different tiles. With the interleaver dimension a multiple of N, we get the effect of interleaving each slot separately. This simple change provides a remedy to the problem, however it does not offer time diversity. The reason for choosing 6N for the uplink is that the diversity order of each slot is 6 (6 tiles), and each 8 subcarriers are correlated, so increasing the dimension above 6N would create couples of adjacent bits that reside in the same tiles and are correlated. In the downlink, the dimension 12N is designed to slightly increase the distance between subcarriers carrying adjacent bits (4 subcarriers compared to 3 subcarriers today).

5.3. Alternative B

Use the same interleaver (with interleaver dimension equals 6 / 12 in the UL / DL respectively), however reorder the sub-carriers in the FEC block. The purpose of this reordering is to gather adjacent sub-carriers in frequency domain and in time domain, so that adjacent sub-carriers in the interleaver input will have significant correlation. The proposed reordering operation is depicted in Figure 3:

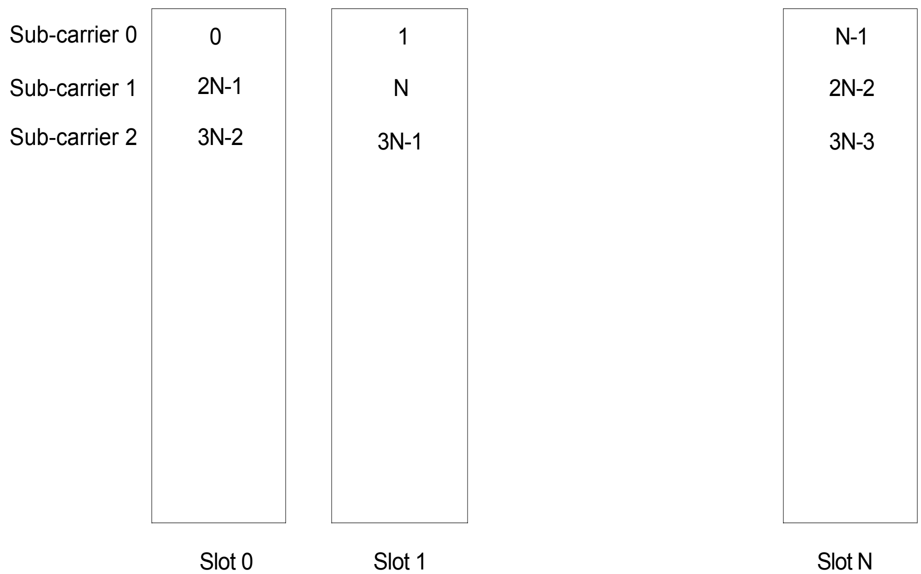
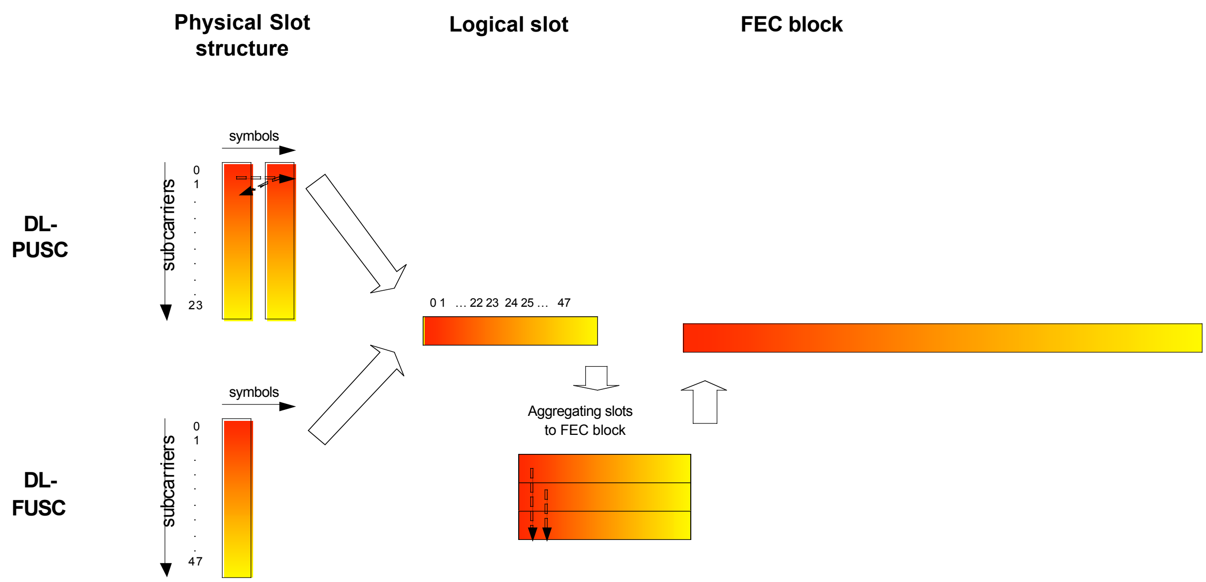


Figure 3: Sub-carrier reordering

In order to do the reordering properly, we need to remove the in-slot rotation, for both DL and UL. Removal of the in-slot rotation requires a change in the way repetition is done. We suggest that each slot shall be rotated by $48 \cdot n/R$ subcarriers where R is the number of repetition and n is the repetition index (0 .. R-1).

After this remedy is applied the correlation structure in a FEC block before de-interleaving will look as follows:



<u>Figure 4: FEC block correlation after correction</u>

6. Text changes

6.1. Alternative A

6.1.1. Change of mapping inside a slot to time-first

8.4.6.1.2.1.1 Downlink subchannels subcarrier allocation in PUSC

[Change the numbered items of the first paragraph]

5) The data subcarriers of each slot shall be mapped to the subchannel such that <u>even numbered</u> data subcarriers <u>(0,2,4,… 46)</u> ~~numbered 0 to 23~~ reside on the first (time wise) symbol of each symbol pair on the subcarriers whose index is 0 to 23 respectively in Equation (111) and the <u>odd numbered</u> data subcarriers <u>(1,3,5,… 47)</u> ~~numbered 24 to 47~~ reside on the second symbol on the subcarriers whose index is 0 to 23 respectively in Equation (111).

8.4.6.2.2 Partitioning of subcarriers into subchannels in the uplink

[Change the first bullet of the enumerated list below Equation (113)]

1. After allocating the pilot carriers within each tile, indexing of the data subcarriers within each subchannel is performed <u>in a time-first order</u> starting from the first symbol at the lowest indexed subcarrier of the lowest indexed tile and continuing in an ascending manner throughout the <u>slot symbols in the same subcarrier, then going to the next subcarrier at the lowest index symbol in the slot, and so on.</u> ~~subchannel's subcarriers in the same symbol, then going to the next symbol at the lowest indexed data subcarrier, and so on.~~ Data subcarriers shall be indexed from 0 to 47.

6.1.2. Change of interleaver dimension

8.4.9.3 Interleaving

[Delete all d=16 appearances, in formulas (130) - (133)]

[Add the following sentence at the end of the second paragraph]

The value of d shall be set to 12n for the DL and 6n for the UL, where n is the number of allocated slots per FEC block.

6.2. Alternative B

6.2.1. Change of mapping inside a slot to time-first

8.4.6.1.2.1.1 Downlink subchannels subcarrier allocation in PUSC

[Change the numbered items of the first paragraph]

5) The data subcarriers of each slot shall be mapped to the subchannel such that even numbered data subcarriers (0,2,4,… 46) ~~numbered 0 to 23~~ reside on the first (time wise) symbol of each symbol pair on the subcarriers whose index is 0 to 23 respectively in Equation (111) and the odd numbered data subcarriers (1,3,5,… 47) ~~numbered 24 to 47~~ reside on the second symbol on the subcarriers whose index is 0 to 23 respectively in Equation (111).

8.4.6.2.2 Partitioning of subcarriers into subchannels in the uplink

[Change the first bullet of the enumerated list below Equation (113)]

2. After allocating the pilot carriers within each tile, indexing of the data subcarriers within each subchannel is performed in a time-first order starting from the first symbol at the lowest indexed subcarrier of the lowest indexed tile and continuing in an ascending manner throughout the slot symbols in the same subcarrier, then going to the next subcarrier at the lowest index symbol in the slot, and so on. ~~subchannel's subcarriers in the same symbol, then going to the next symbol at the lowest indexed data subcarrier, and so on.~~ Data subcarriers shall be indexed from 0 to 47.

6.2.2. Removal of in-slot rotations

6.2.2.1. Downlink FUSC & PUSC

8.4.6.1.2.2.2 Partitioning of data subcarriers into subchannels in downlink FUSC

[Replace Equation (111) with the following equation]

$$subcarrier(k,s) = N_{subchannels} \cdot k + \{p_s[k \bmod N_{subchannels}] + DL\_PermBase\} \bmod N_{subchannels} \quad (111)$$

[Remove the parameter 'n$_k$' and insert new parameter 'k' below equation (111)]

~~$n_k = (k + 13 \cdot s) \bmod N_{subcarriers}$,~~

~~where k is the subcarrier-in-subchannel index from the set $[0 \ldots N_{subcarriers} - 1]$,~~

k is the subcarrier-in-subchannel index from the set $[0 \ldots N_{subcarriers} - 1]$,

6.2.2.2. Uplink PUSC and OPUSC

8.4.6.2.2 Partitioning of subcarriers into subchannels in the uplink

[Remove the second bullet of the enumerated list below Equation (113)]

2. ~~The enumeration of the subcarriers will follow Equation (114). This enumeration sets the order to which the mapping of the data onto the subcarriers shall be performed.~~

[Remove equation (114) and the parameters legend below it]

6.2.2.3. AMC

8.4.6.3 Optional adjacent subcarrier permutations AMC

[Remove the text below table 316 at page 575, until the end of section 8.4.6.3]

~~Let the index of the traffic subcarriers be numbered from 0 to 47 within an AMC subchannel. The index of first traffic subcarrier in the first bin is 1, next one is 2 and so on. The index of the subcarriers increases along the subcarriers first then the bin. The j-th symbol of the 48 symbols where a band AMC subchannel is allocated is mapped onto the -th subcarrier of a subchannel. j is [0, 47].~~

~~…. (equation) … (112)~~

~~where~~
~~Pper(j) is the j-th element of the left cyclic shifted version of basic sequence P0 by per.~~
~~P0 Basic sequence defined in GF(72): {01, 22, 46, 52, 42, 41, 26, 50, 05, 33, 62, 43, 63, 65, 32, 40, 04, 11, 23, 61, 21, 24, 13, 60, 06, 55, 31, 25, 35, 36, 51, 20, 02, 44, 15, 34, 14, 12, 45, 30, 03, 66, 54, 16, 56, 53, 64, 10} in hepta-notation.~~
~~per = IDcell mod 48~~
~~off =...~~
~~The addition between two element in GF(72) is component-wise addition modulo 7 of two representation. For example, (56) + (34) in GF(72) = (13).~~

6.2.3. Addition of new slot-aggregation scheme into interleaver (as 3rd permutation)

8.4.9.3 Interleaving

[Change the section]

All encoded data bits shall be interleaved by a block interleaver with a block size corresponding to the number of coded bits per the encoded block size N_{cbps}. The interleaver is defined by a ~~two~~ three-step permutation. The first ensures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second permutation insures that adjacent coded bits are mapped alternately onto less or more significant bits of the constellation, thus avoiding long runs of lowly reliable bits. The third permutation collects subcarriers to form slots, and ensures that adjacent bits are mapped to different slots and distant locations inside the slot.

Let N_{cpc} be the number of coded bits per subcarrier, i.e., 2, 4 or 6 for QPSK, 16-QAM or 64-QAM, respectively. Let $s = N_{cpc}/2$. Within a block of N_{cbps} bits at transmission, let k be the index of the coded bit before the first permutation, m_k be the index of that coded bit after the first and before the second permutation, ~~and let j_k~~ l_k be the index after the second and before the third permutation, and let j_k be the index after the third permutation just prior to modulation mapping, and d be the modulo used for the permutation. The value of d shall be set to 12 for the DL and 6 for the UL.

The first permutation is defined by the formula: ~~k = 0,1,…,N_{cbps} – 1 , d = 16~~

(130) $m_k = (N_{cbps}/d)\cdot k_{\mathrm{mod}\,d} + floor(k/d) \qquad k = 0,1,\dots,N_{cbps-1}$ ~~$d = 16$~~

The second permutation is defined by the formula:

(131) ~~j_k~~ $l_k = s\cdot floor(m_k/s) + (m_k + N_{cbps} - floor(d\cdot m_k/N_{cbps}))_{\mathrm{mod}\,s} \qquad k = 0,1,\dots,N_{cbps-1}$ ~~$d = 16$~~

The third permutation is defined by the following formula:

(131a)
$$j_k = \left(floor\left(\frac{l_k}{N\cdot N_{cpc}}\right) + \left(floor\left(\frac{l_k}{N\cdot N_{cpc}}\right) + floor\left(\frac{l_k}{N_{cpc}}\right)\right)\bmod N\cdot 48\right)\cdot N_{cpc} + l_k \bmod N_{cpc}$$
$$k = 0,1,\dots,N_{cbps-1} \qquad N = N_{cbps}/(48N_{cpc})$$

The de-interleaver, which performs the inverse operation, is also defined by ~~two~~ three permutations. Within a received block of N_{cbps} bits, let j be the index of a received bit before the first permutation; l_j be the index of that bit after the first and before the second permutation; m_j be the index ~~of that bit~~ after the ~~first~~ second and before the ~~second~~ third permutation; and let k_j be the index of that bit after the ~~second~~ third permutation, just prior to delivering the block to the decoder.

The first permutation is defined by the formula:

(132a)

$$l_j = \left(floor\left(\frac{j}{N_{cpc}}\right) \bmod 48 \cdot N + \left(floor\left(\frac{j}{48N_{cpc}}\right) - floor\left(\frac{j}{N_{cpc}}\right) \bmod 48 \right) \bmod N \right) \cdot N_{cpc} + j \bmod N_{cpc}$$

$j = 0,1,\ldots,N_{cbps-1}$ $\quad N = N_{cbps}/(48N_{cpc})$

The ~~first~~ second permutation is defined by the formula:

(132) ~~$m_j = s \cdot floor(j/s) + (j + floor(d \cdot j/N_{cbps}))_{\bmod s}$ $\quad j = 0,1,\ldots,N_{cbps-1}$ $\quad d = 16$~~

$m_j = s \cdot floor(l_j/s) + (l_j + floor(d \cdot l_j/N_{cbps}))_{\bmod s}$ $\quad j = 0,1,\ldots,N_{cbps-1}$

The ~~second~~ third permutation is defined by the formula:

(133) $k_j = d \cdot m_j - (N_{cbps} - 1) \cdot floor(d \cdot m_j / N_{cbps})$ $\quad j = 0,1,\ldots,N_{cbps-1}$ $\quad$ ~~$d = 16$~~

The first permutation in the de-interleaver is the inverse of the ~~second~~ third permutation in the interleaver, the second permutation in the de-interleaver is the inverse of the second permutation in the interleaver, and the third permutation in the de-interleaver is the inverse of the first permutation in the interleaver. ~~and conversely.~~

6.2.4. Resolution of repetition

8.4.9.5 Repetition

[Add the following sentence at the end of section]

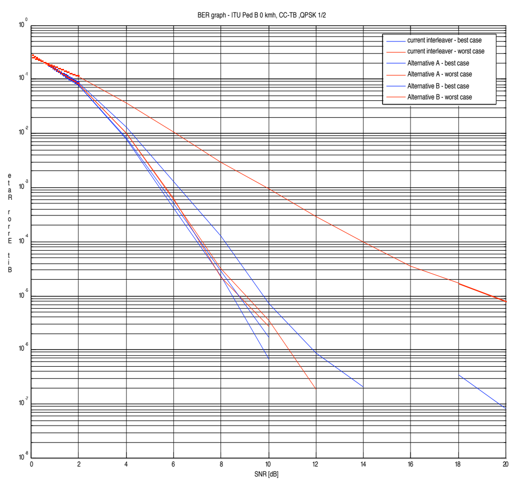
Each repeated slot shall be rotated by 48·n/R subcarriers, where n is the repetition index (0,1, ..., R-1), such that the i-th bit in the n-th repeated slot comes from the (i-48·N_{cpc} n/R) bit in the original slot.

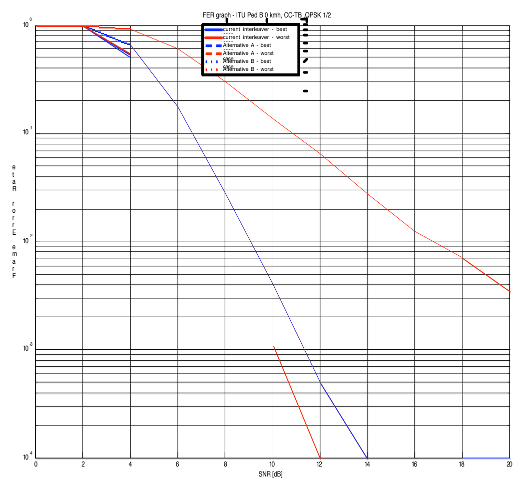
Appendix A - Downlink simulation results

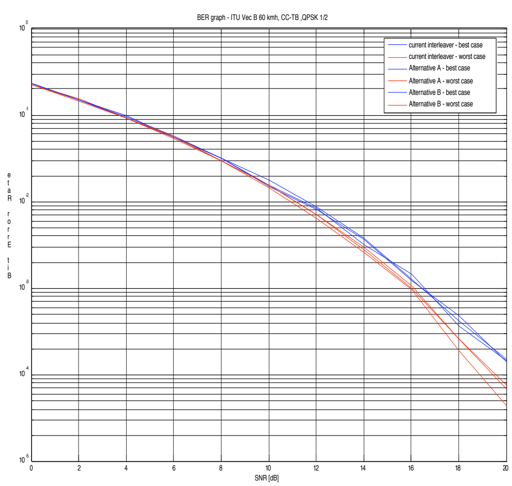
A.1. Simulation parameters

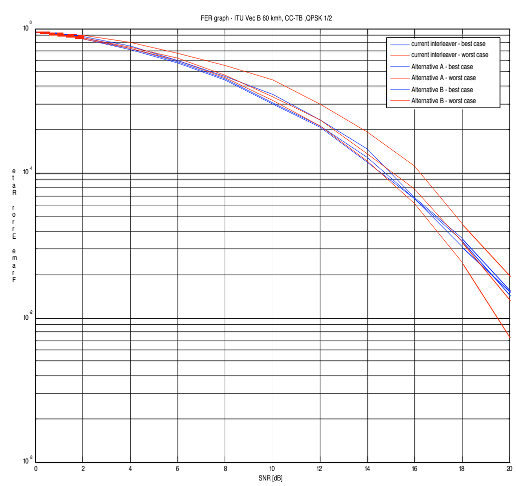
Permutation	DL-PUSC
FFT size	512
BW	5 Mhz
Modulation	QPSK _
Code	CC-TB
Frame	600 bytes
Bursts allocation	best case - 5 sub-channels / worst case – 1 sub-channel
FEC block size	best case - 6 slots / worst case – 4 slots
Channel	random channel , normalized to unity power over signal band
	ITU ped B 0 kmh / ITU vec A 60 kmh / ITU vec B 60 kmh

A.2. Simulation results









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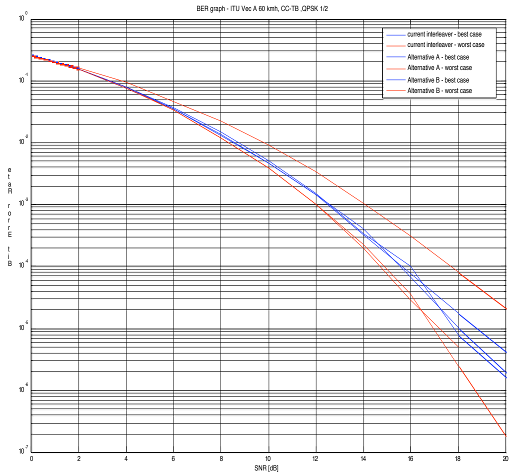
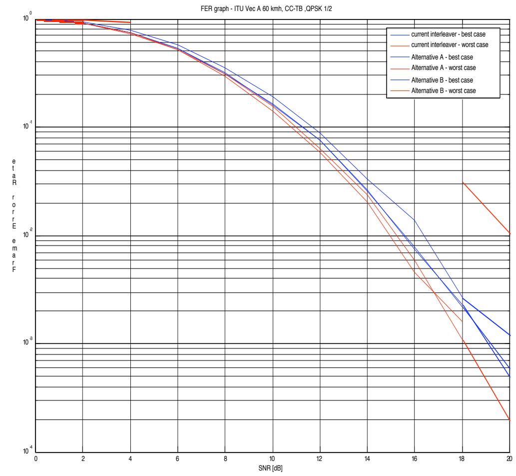

BER graph - ITU Vec A 60 kmh, CC-TB ,QPSK 1/2
current interleaver - best case
current interleaver - worst case
Alternative A - best case
Alternative A - worst case
Alternative B - best case
Alternative B - worst case
Bit Error Rate
SNR [dB]


FER graph - ITU Vec A 60 kmh, CC-TB ,QPSK 1/2
current interleaver - best case
current interleaver - worst case
Alternative A - best case
Alternative A - worst case
Alternative B - best case
Alternative B - worst case
Frame Error Rate
SNR [dB]

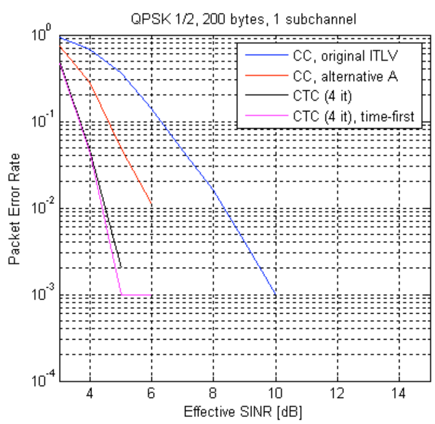
Appendix B – Uplink simulation results

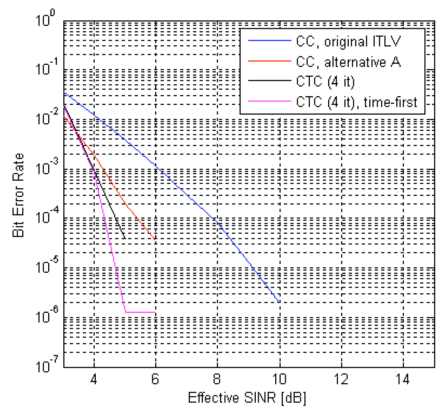
B.1. Simulation parameters

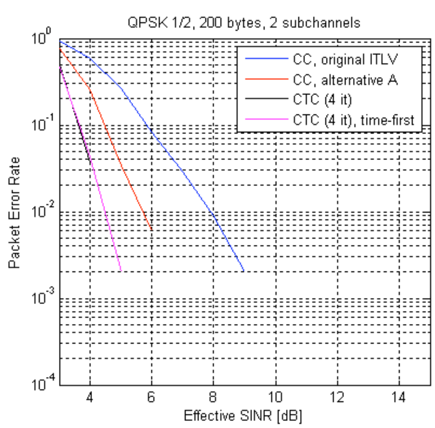
Permutation	UL-PUSC
FFT size	512
BW	5 Mhz
Modulation	QPSK _ / QPSK _ / 16-QAM _ / 64-QAM _ / 64-QAM 3/4
Code	CC-TB / CTC
Frame	200 bytes
Bursts allocation	1 / 2 / 4 sub-channels
FEC block size	According to modulation: 6 / 4 / 3 / 2 / 1 slots
Channel	random channel, normalized to unity power over signal band ITU ped B 0 kmh

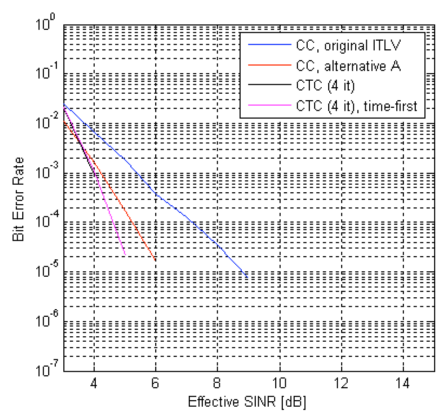
B.2. Simulation results

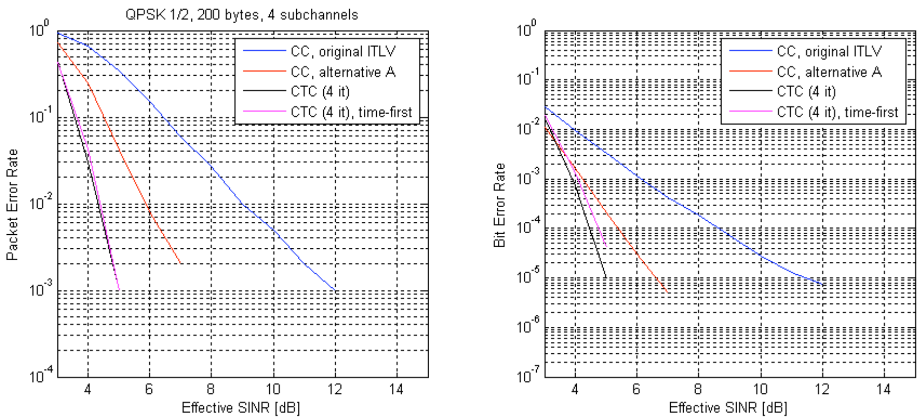
QPSK _, 6 slots/FEC block:



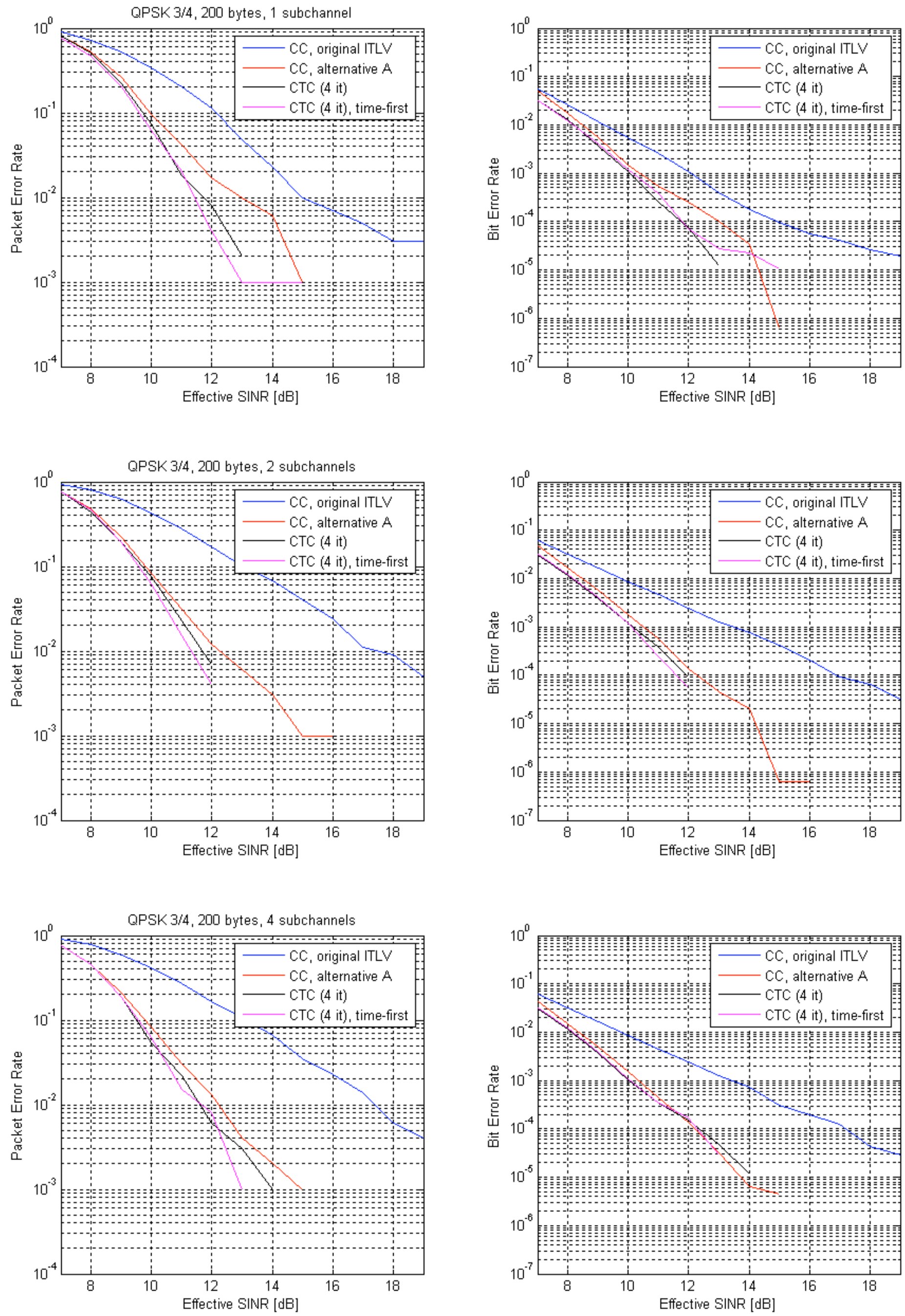




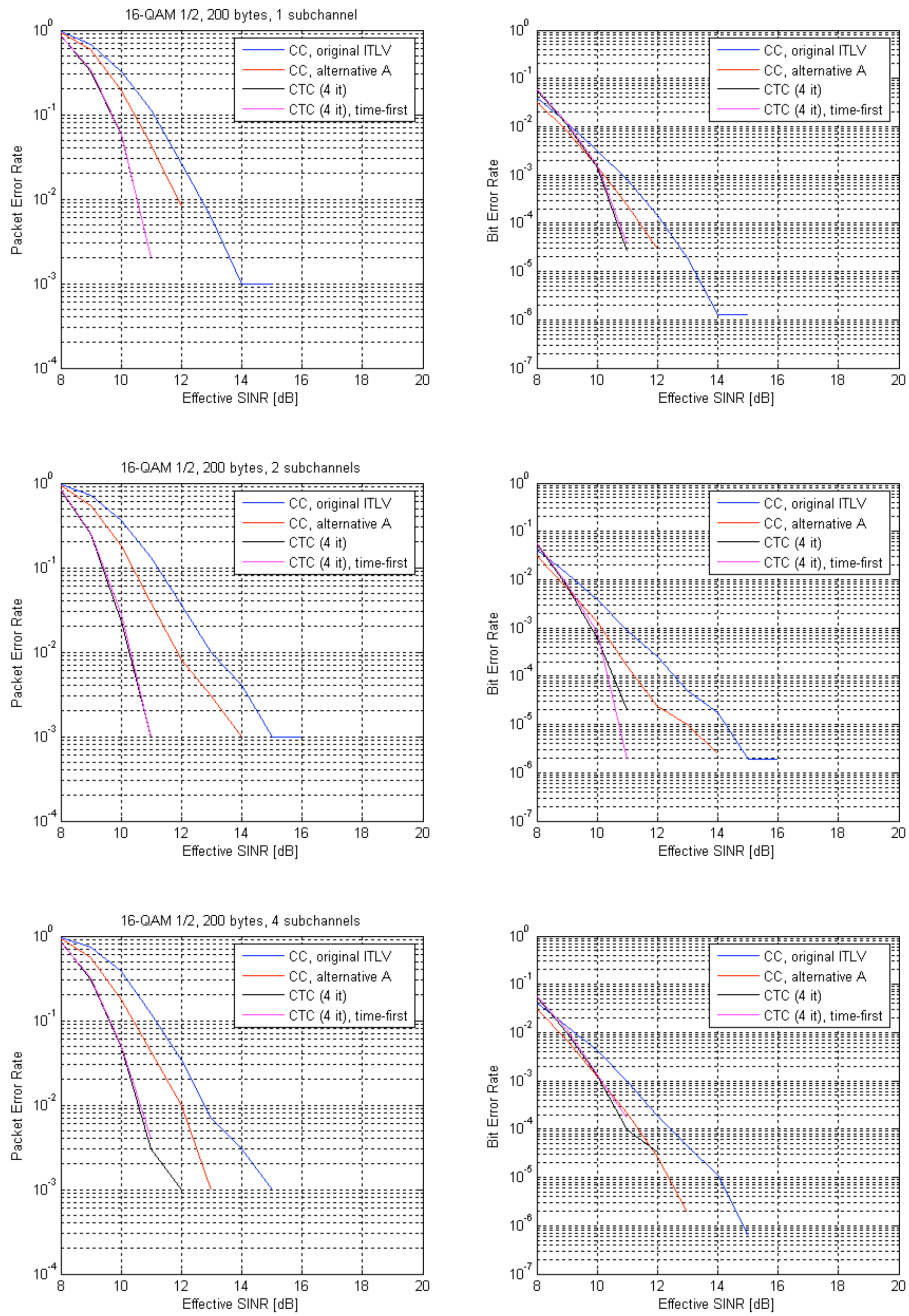



QPSK 1/2, 200 bytes, 4 subchannels
Packet Error Rate
Effective SINR [dB]
CC, original ITLV
CC, alternative A
CTC (4 it)
CTC (4 it), time-first
Bit Error Rate
Effective SINR [dB]
CC, original ITLV
CC, alternative A
CTC (4 it)
CTC (4 it), time-first

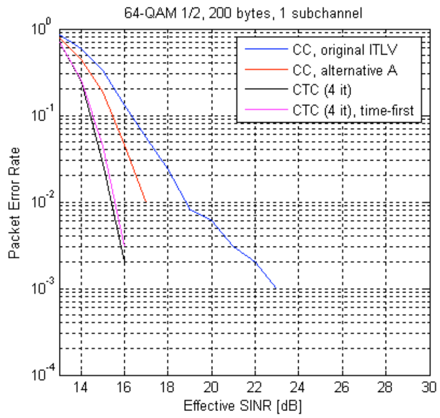
QPSK _, 4 slots/FEC block:

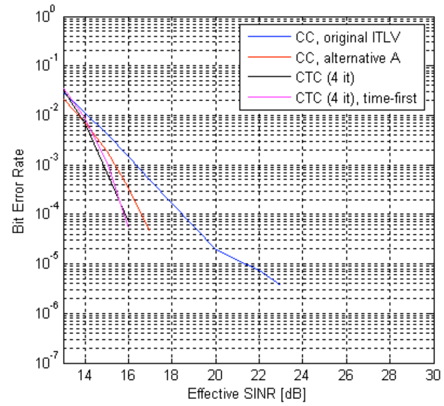


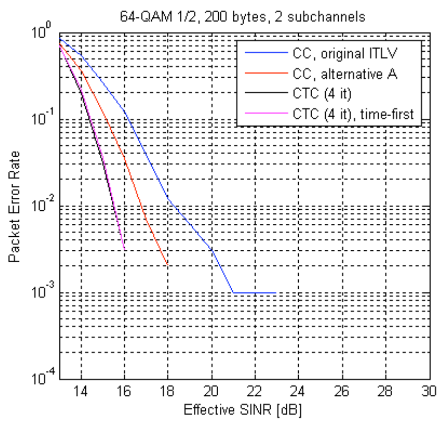
16-QAM _, 3 slots/FEC block:

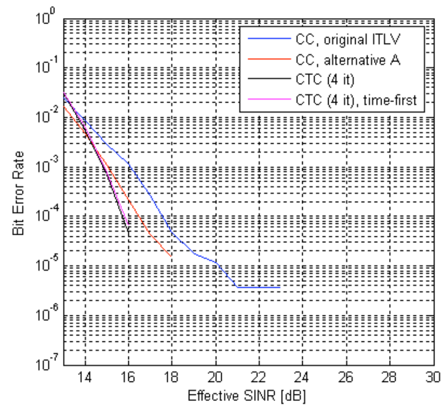


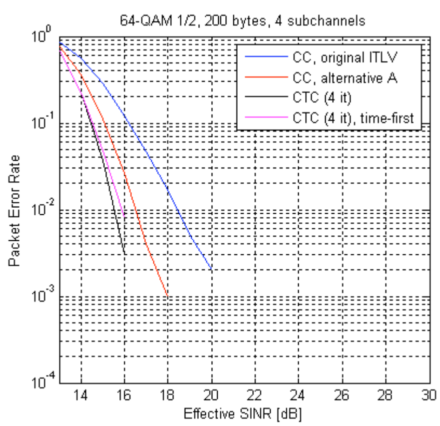
64-QAM _, 2 slots/FEC block:

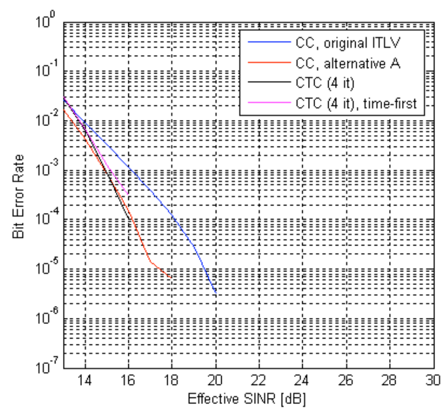












64-QAM _, 1 slot/FEC block: