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Re:	Recirculation of P802.16 REVe/D3
Abstract	This contribution presents correction of DL/UL Physical modifier IEs.
Purpose	Adopt into P802.16e/D4
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Correction of DL/UL Physical modifier IEs

Problem Definition

The resolution on comment 253 in 80216-04_23 is not reflected on 802.16 REVd/D3. Thus, the following should be adopted.

The adopted UL AAS preambles are not consistent with the DL AAS preamble. Orthogonal AAS preambles are needed also in the UL to obtain the accurate UL channel response for multiple SS's transmitting simultaneously. The "exact time index shift" defined in PHY_MOD_DL_IE is missing in PHY_MOD_UL_IE.

Proposed Enhancement

[Replace section 8.4.5.4.14 "UL-MAP physical Modifier IE"]

8.4.5.4.14 UL-MAP Physical Modifier IE
The Physical Modifier Information Element indicates that the subsequent allocations shall utilize a preamble, which is either randomized or cyclically delayed in time by k samples (see Equation (100) and Equation (101)). The PHYMOD_UL_IE can appear anywhere in the UL map, and it shall remain in effect until another PHYMOD_UL_IE is encountered, or until the end of the UL map.

Table 300. Structure of PHYMOD_UL_IE ()

PHY_MOD_UL_IE() {		
Extended UIUC	4 bits	
Length	4 bits	
Preamble Modifier Type	1 bit	0 – Randomized preamble 1 – Cyclically shifted Preamble
if (Preamble Modifier Type == 0) {		
Preamble Frequency Shift Index	4 bits	Indicates the value of K in equation (aaa)
Reserved	1 bit	
} else {		
Time Index Shift Type	1 bit	0 – Rounded down shift 1 – Exact shift
if (Time Index Shift Type == 0)		
Preamble Time Shift Index	4 bits	For PUSC, 0 – 0 sample cyclic shift 1 – floor(Nfft/4) sample cyclic shift …. 3 – floor(Nfft/4*3) sample cyclic shift 4-15 – reserved For optional PUSC, 0 – 0 sample cyclic shift 1 – floor(Nfft/3) sample cyclic shift 2 – floor(Nfft/3*2) sample cyclic shift 3-15 – reserved For AMC permutation, 0 – 0 sample cyclic shift 1 – floor(Nfft/9) sample cyclic shift ….

		8 – floor(Nfft/9*8) sample cyclic shift 9-15 – reserved
} else {		
Preamble Time Shift Index	4 bits	For PUSC, 0 – 0 sample cyclic shift 1 – Nfft/4 sample cyclic shift …. 3 – Nfft/4*3 sample cyclic shift 4-15 – reserved For optional PUSC, 0 – 0 sample cyclic shift 1 – Nfft/3 sample cyclic shift 2 – Nfft/3*2 sample cyclic shift 3-15 – reserved For AMC permutation, 0 – 0 sample cyclic shift 1 – Nfft/9 sample cyclic shift …. 8 – Nfft/9*8 sample cyclic shift 9-15 – reserved
}		
}		
Reserved	3 2 bits	
}		

Preamble Modifier Type
This parameter defines whether the preamble will be randomized or cyclically shifted in time or in frequency.

Preamble Frequency Shift Index
This parameter effects the cyclic shift of the preamble in frequency axis, as defined by equation (aaa)

Preamble Time Shift Index
The parameter defines how many samples of cyclic shift shall be introduced into the preamble symbols. The unit of cyclic shift depends on the subchannel permutation to ensure the frequency-domain orthogonality between the different preambles in the same subchannel.

[Replace Table 284 in section 8.4.5.3.11]

Table 284.-OFDMA DL-MAP Physical Modifier IE format

PHY_MOD_DL_IE() {		
Extended DIUC	4 bits	PHYMOD = 0x08
Length	4 bits	Length = 0x03
Preamble Modifier Type	1 bit	0 – Randomized preamble 1 – Cyclically shifted Preamble
if (Preamble Modifier Type == 0) {		
Preamble Frequency Shift Index	4 bits	Indicates the value of K in equation (101)
Reserved	1 bit	
} else {		
Time Index Shift Type	1 bit	0 – Rounded down shift 1 – Exact shift
if (Time Index Shift Type == 0)		
Preamble Time Shift Index	4 bits	For PUSC, 0 – 0 sample cyclic shift 1 – floor(Nfft/14) sample cyclic shift ….

		13 – floor(Nfft/14*13) sample cyclic shift 14-15 – reserved For AMC permutation, 0 – 0 sample cyclic shift 1 – floor(Nfft/9) sample cyclic shift …. 8 – floor(Nfft/9*8) sample cyclic shift 9-15 – reserved
} else {		
Preamble Time Shift Index	4 bits	For PUSC, 0 – 0 sample cyclic shift 1 – ~~floor(~~Nfft/14~~)~~ sample cyclic shift …. 13 – ~~floor(~~Nfft/14*13~~)~~ sample cyclic shift 14-15 – reserved For AMC permutation, 0 – 0 sample cyclic shift 1 – ~~floor(~~Nfft/9~~)~~ sample cyclic shift …. 8 – ~~floor(~~Nfft/9*8~~)~~ sample cyclic shift 9-15 – reserved
}		
}		
Reserved	2 bits	
}		