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Abstract	*Proposal for LDPC FEC scheme as an option for OFDMA*
Purpose	This document is submitted for review by 802.16e Working Group members
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Scalable LDPC coding scheme for OFDMA

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1 Introduction

There are a lot of proposals [1,2,3,4] for the design of LDPC codes. Some of those contributions are based on a single H-matrix to minimize possible complexity and the others [1] use multiple matrices in order to provide different code rates. On the current agreement, maximum codeword length is around 2000 bits. This contribution describes the design method and encoding procedure for proposed LDPC codes, which shows good performance without high complexity. In addition, the proposed scheme gives good flexibility for rate adjustment.

2 Parity check matrix of LDPC codes

For an (N, K) LDPC code, where N, K, and R are codeword length, Information length respectively. Given (N, K) H matrix with size (N-K)*N, let H be [H_d | H_p], where H_p is a dual-diagonal square matrix. Let H_d have column weight w_c and row weight w_r. H_d matrix consists of R/(1-R) square matrices $H_{d,i}$ with size (N-K)*(N-K), where i =1,2, … , R/(1-R). Now each $H_{d,i}$ consists of m*m square-submatrices $H_{d,i}^{(j,k)}$ with size ((N-K)/m)*((N-K)/m), where j=1,2, … , m and k=1,2, … ,m and m is resolution factor. Square-submatrices $H_{d,i}^{(j,k)}$ are permutation matrices or square zero matrices. H_d has constant row weight and constant column weight. If w_c = m, there is no square zero matrix with size ((N-K)/m)* ((N-K)/m) in H_d . If w_c < m, , H_d has square zero matrices with size ((N-K)/m)*((N-K)/m) in H_d. In this case, the number of square zero matrices with size ((N-K)/m)* ((N-K)/m) is m- w_c in each column submatix and each row submatix in each $H_{d,i}$ and the rest of submatrices are permutation matrices. Additionally the number of short cycles is minimized.

Equation.1) $$H_d = \left[H_{d,1} \middle| H_{d,2} \middle| ..... \middle| H_{d,q} \right] \quad \text{for } q = R/(1-R) \text{ and } R=K/N.$$

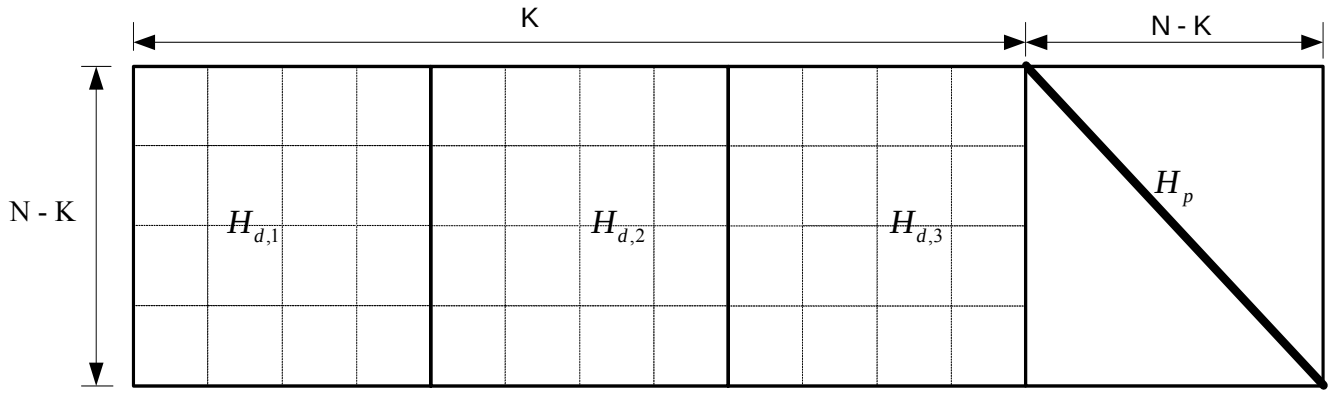


Figure1. Regular H-matrix with q=3

Characteristics of the H-matrix

- **H_d has nearly regular weights in column and row-wise.**
- **Due to evenly spread weight distribution, after shortening and puncturing, loss of weight is minimized in both column and row-wise.**
- **Its regularity is kept even in the case of reducing column or row-wise in unit of sub-matrix for rate adjustment**
- **No error floor in FER range of interest (around FER=10^{-4})**
- **Low complexity in the aspects of encoding, decoding, and implementation due to relatively small number of total weight.**
- **High scalability for rate adjustment based on a single matrix, e.g., r=1/2, 2/3, 3/4**
- **Low complexity encoding by using exact dual-diagonal part, i.e., H_p with size (N-K)*(N-K)**
- **Fully support H-ARQ**

3 Encoding procedure

In the Equation.1, H_p is represented by a differential encoder and thus only one sparse matrix multiplication, $H_d \times u$, is needed.

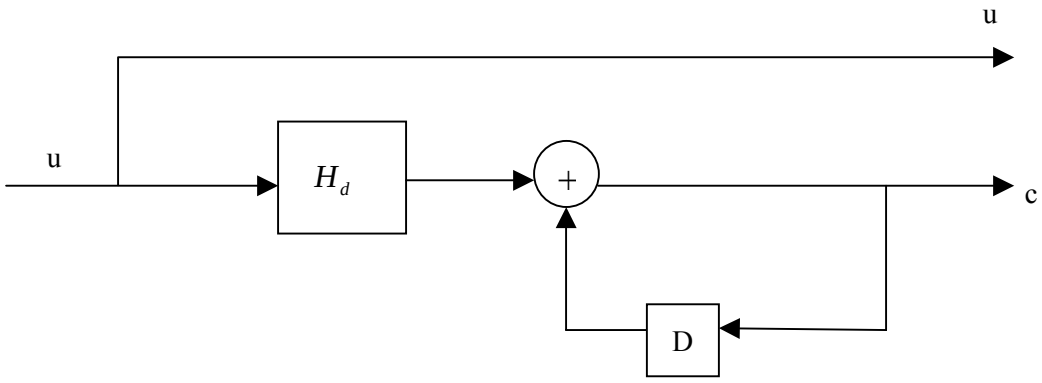


Figure 2. Encoder diagram

4 Rate Adaptation

The essential feature of LDPC codes for AMC and H-ARQ including IR and Chase-combining is rate adaptation based on OFDMA PHY subcarrier allocation. The following subsections describe various rate adaptation scheme supported with proposed LDPC codes.

4.1 Shortening Scheme

To decrease the code rate, shortening is used. For shortening, the part of H_d matrix is masked in unit of square submatrix with size ((N-K)/m)*((N-K)/m) in column-wise and in turn the length of the systematic portion of the codeword is reduced. After shortening, the row weight and column weight keep their regularity because of the structure of proposed LDPC codes.

R Code Rate	N_{cw} (bits)	N_{info} (bits)	N_{parity} (bits)
R = 4/5	1920	1536	384
R = 3/4	1536	1152	384
R =2/3	1152	768	384
R =1/2	768	384	384
R = 1/3	576	192	384

Table 1. Parameters for rate adjustment by shortening, given a single master matrix.

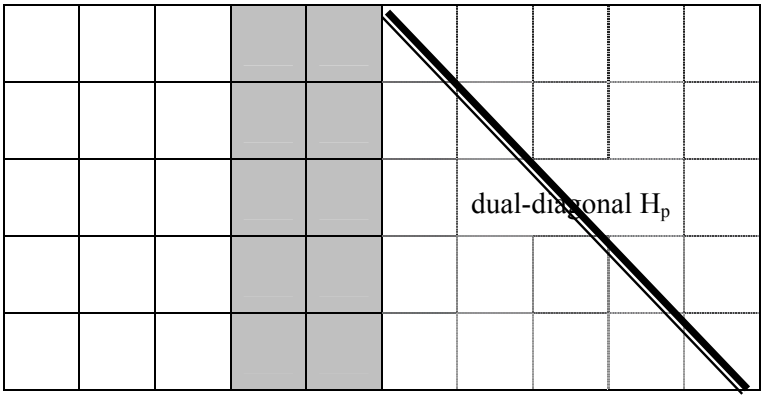


Figure 3. An example of reducing systematic bits (shaded area is reduced)

4.2 H matrix reduction (puncturing) for IR

To increase the code rate, puncturing is used. For puncturing, the part of H_d matrix and the part of H_p matrix are masked in unit of square submatrix with size ((N-K)/m)*((N-K)/m) in column-wise and row-wise and in turn the length of the parity portion of the codeword is reduced. After puncturing, the row weight and column weight keep their regularity because of the structure of proposed LDPC codes.

R Code Rate	N_{cw} (bits)	N_{info} (bits)	N_{parity} (bits)
R = 4/5	1440	1152	288
R = 3/4	1536	1152	384
R =2/3	1728	1152	576
R =1/2	2304	1152	1152
R = 1/3	3456	1152	2304

Table 2. Parameters for IR by puncturing, given a single master matrix.

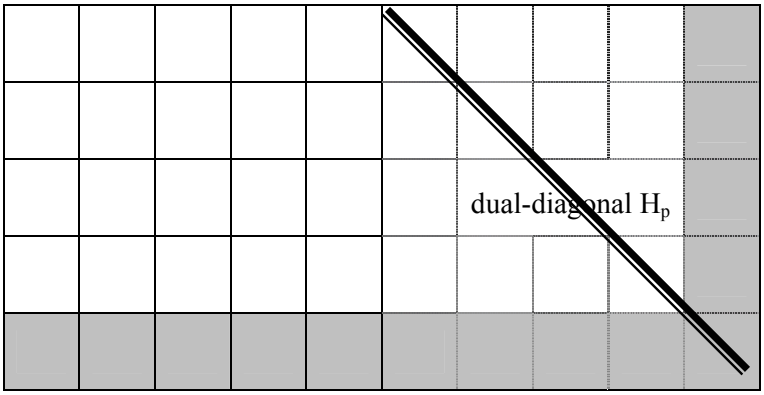


Figure 4. An example of reducing parity bits (shaded area is reduced)

4.3 Combinations of shortening and puncturing

For more flexible rate adjustment, any combinations of shortening and puncturing can be used in proposed LDPC codes keeping regularity of column and row weight. For example, first shortening applies to H master matrix and then puncturing applies to the reduced H matrix. When shortening and puncturing is applied, severe weight loss can be avoided.

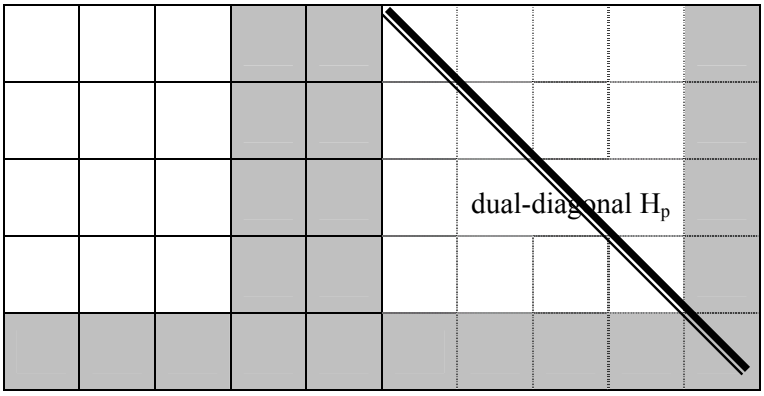


Figure 5. An example of reducing parity bits and systematic bits (shaded area is reduced)

5 H-ARQ using LDPC codes

Current 802.16 Rev/D5 supports H-ARQ operation with IR for all codes in MAC layer. Specifically CTC PHY provides H-ARQ operation. Since LDPC codes have many good properties for H-ARQ originated from block code properties, such as puncturing and shortening. The following subsections describe various options supported with proposed LDPC codes

5.1 Chase combining scheme

Proposed LDPC codes support fully chase–combining operation in a given code rate. Chase–combining operation is attractive because of simplicity.

5.2 IR sheme

Proposed LDPC codes support IR operation with puncturing technique without performance degradation due to severe weight loss, e.g., very low column weight (1 or 2). For certain channel state, IR operation shows better performance [4].

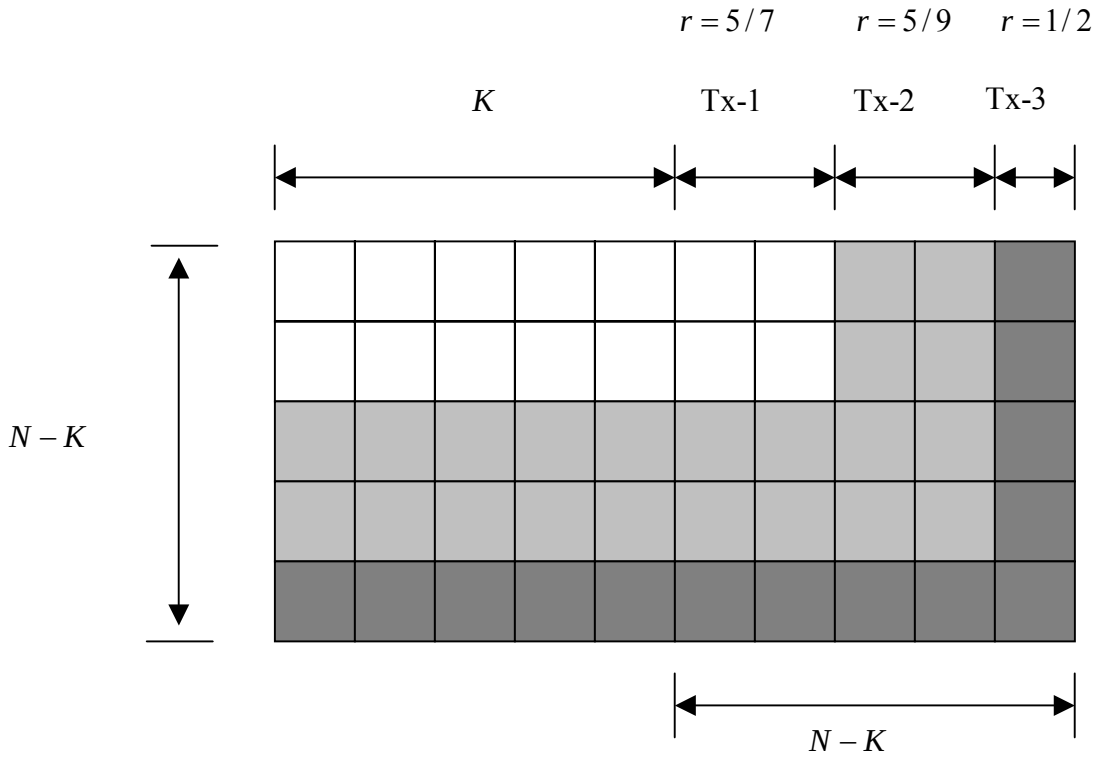


Figure 6. An example of IR scheme (For Tx-1, white area in H is used. For Tx-2, white and lightly shaded area is used. For Tx-3, full matrix H is used.)

5.3 Code Rate Table

Proposed LDPC codes support Chase–combining operation and IR operation. Such an example is shown the following table.

subchannel	coded bit	parity bit		parity bit		parity bit		parity bit		parity bit		parity bit		parity bit		parity bit	
		288		384		480		576		672		768		864		960	
1	96																
2	192	rate	info. bit														
3	288			rate	info. bit												
4	384	0.25	96			rate	info. bit										
5	480	0.4	192	0.2	96			rate	info. bit								
6	576	0.5	288	0.333333	192	0.166667	96			rate	info. bit						
7	672	0.57143	384	0.428571	288	0.285714	192	0.142857	96			rate	info. bit				
8	768	0.625	480	0.5	384	0.375	288	0.25	192	0.125	96			rate	info. bit		
9	864	0.66667	576	0.555556	480	0.444444	384	0.333333	288	0.222222	192	0.111111	96			rate	info. bit
10	960	0.7	672	0.6	576	0.5	480	0.4	384	0.3	288	0.2	192	0.1	96		
11	1056	0.72727	768	0.636364	672	0.545455	576	0.454545	480	0.363636	384	0.272727	288	0.181818	192	0.09091	96
12	1152	0.75	864	0.666667	768	0.583333	672	0.5	576	0.416667	480	0.333333	384	0.25	288	0.16667	192
13	1248	0.76923	960	0.692308	864	0.615385	768	0.538462	672	0.461538	576	0.384615	480	0.307692	384	0.23077	288
14	1344	0.78571	1056	0.714286	960	0.642857	864	0.571429	768	0.5	672	0.428571	576	0.357143	480	0.28571	384
15	1440	0.8	1152	0.733333	1056	0.666667	960	0.6	864	0.533333	768	0.466667	672	0.4	576	0.33333	480
16	1536	0.8125	1248	0.75	1152	0.6875	1056	0.625	960	0.5625	864	0.5	768	0.4375	672	0.375	576
17	1632	0.82353	1344	0.764706	1248	0.705882	1152	0.647059	1056	0.588235	960	0.529412	864	0.470588	768	0.41176	672
18	1728	0.83333	1440	0.777778	1344	0.722222	1248	0.666667	1152	0.611111	1056	0.555556	960	0.5	864	0.44444	768
19	1824	0.84211	1536	0.789474	1440	0.736842	1344	0.684211	1248	0.631579	1152	0.578947	1056	0.526316	960	0.47368	864
20	1920	0.85	1632	0.8	1536	0.75	1440	0.7	1344	0.65	1248	0.6	1152	0.55	1056	0.5	960
21	2016	0.85714	1728	0.809524	1632	0.761905	1536	0.714286	1440	0.666667	1344	0.619048	1248	0.571429	1152	0.52381	1056
22	2112	0.86364	1824	0.818182	1728	0.772727	1632	0.727273	1536	0.681818	1440	0.636364	1344	0.590909	1248	0.54545	1152
23	2208	0.86957	1920	0.826087	1824	0.782609	1728	0.73913	1632	0.695652	1536	0.652174	1440	0.608696	1344	0.56522	1248
24	2304	0.875	2016	0.833333	1920	0.791667	1824	0.75	1728	0.708333	1632	0.666667	1536	0.625	1440	0.58333	1344
25	2400	0.88	2112	0.84	2016	0.8	1920	0.76	1824	0.72	1728	0.68	1440	0.64	1536	0.6	1440

total number of rates supported = 80
rate table from **a single master matrix** r=1/2 H(1920,960) by shortening and puncturing

6 Consideration

Some issues that require further discussion are as follows.

6.1 Effect of increased weight

- Computation: When weight increases in an LDPC code, the amount of computation also increases. Specifically the increased row weight results in heavy computation of check nodes and variable nodes. However, critical heavy computation is not the variable node but the check node.

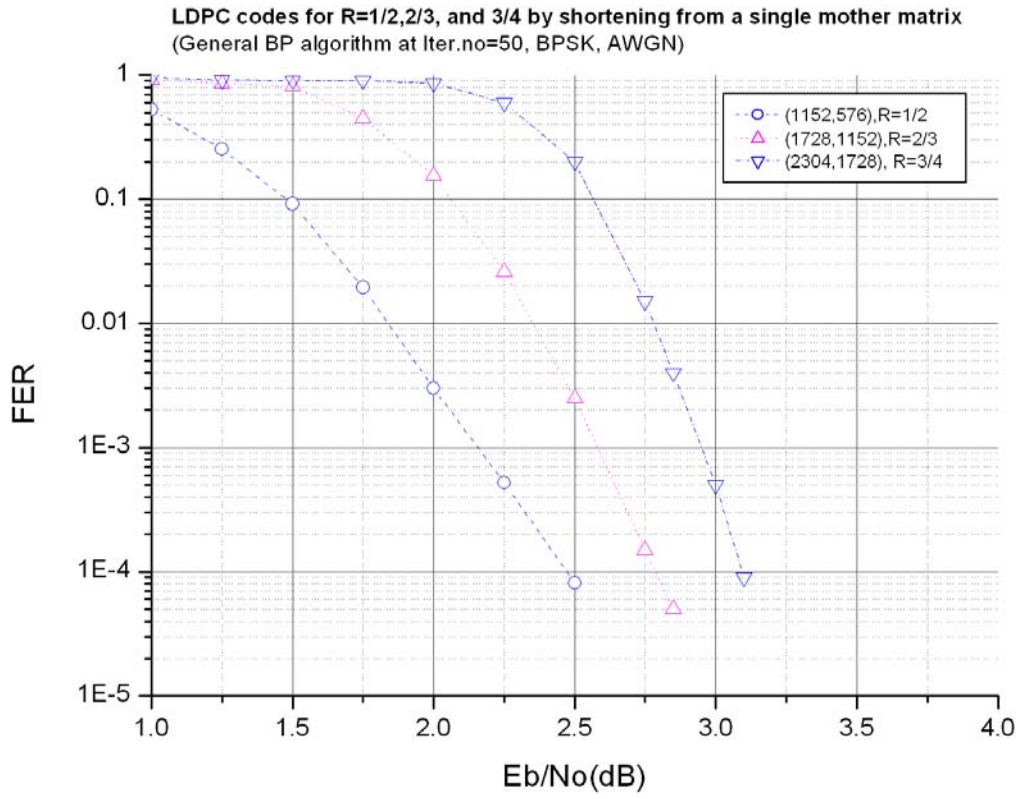
6.2 Flexibility and Efficiency

- Memory size: The chip area is directly related with the size of memory. The majority part of memory for LDPC codes is the size of H matrix.

- Number of H matrices: Because of the memory size issue, the number of H matrices should be minimized. The smaller the number of H matrices are, the smaller the memory size is. A single encoder and decoder is desirable, if possible, for hardware implementation.
- Rate scalability: For saving memory size, the smaller memory size is desirable. Then a single H matrix must have rate scalability, i.e., flexible rate adaptation.
- Supporting both chase-combining and IR: Current standard MAC layer supports IR operation. It is also possible to support chase-combining with additional text change. Then it is a very desirable property for LDPC codes to support both chase-combining and IR operation.

6.3 Evaluation

- Performance and computation trade off is important.



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