

Project	<b>IEEE 802.16 Broadband Wireless Access Working Group</b> < <a href="http://ieee802.org/16">http://ieee802.org/16</a> >	
Title	<b>LDPC Coding for OFDMA PHY</b>	
Date Submitted	<b>2004-11-04</b>	
Source(s)	Min-seok Oh, Kyuhyuk Chung, Kihyoung Cho LG Electronics, Inc. 533, Hogye-1dong, Dongan-gu, Anyang-shi, Kyongki-do, Korea	Voice: 82-31-450-2945 Fax: 82-31-450-7912 <a href="mailto:minoh@lge.com">[mailto:minoh@lge.com]</a> , <a href="mailto:kyuhyuk@lge.com">kyuhyuk@lge.com</a> , <a href="mailto:kihyoung@lge.com">kihyoung@lge.com</a>
Re:	Response to Sponsor Ballot	
Abstract	Proposal for LDPC FEC scheme as an option for OFDMA	
Purpose	Complete the LDPC FEC specification text	
Notice	This document has been prepared to assist IEEE 802.16. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein.	
Release	The contributor grants a free, irrevocable license to the IEEE to incorporate material contained in this contribution, and any modifications thereof, in the creation of an IEEE Standards publication; to copyright in the IEEE's name any IEEE Standards publication even though it may include portions of this contribution; and at the IEEE's sole discretion to permit others to reproduce in whole or in part the resulting IEEE Standards publication. The contributor also acknowledges and accepts that this contribution may be made public by IEEE 802.16.	
Patent Policy and Procedures	The contributor is familiar with the IEEE 802.16 Patent Policy and Procedures < <a href="http://ieee802.org/16/ipr/patents/policy.html">http://ieee802.org/16/ipr/patents/policy.html</a> >, including the statement "IEEE standards may include the known use of patent(s), including patent applications, provided the IEEE receives assurance from the patent holder or applicant with respect to patents essential for compliance with both mandatory and optional portions of the standard." Early disclosure to the Working Group of patent information that might be relevant to the standard is essential to reduce the possibility for delays in the development process and increase the likelihood that the draft publication will be approved for publication. Please notify the Chair < <a href="mailto:chair@wirelessman.org">mailto:chair@wirelessman.org</a> > as early as possible, in written or electronic form, if patented technology (or technology under patent application) might be incorporated into a draft standard being developed within the IEEE 802.16 Working Group. The Chair will disclose this notification via the IEEE 802.16 web site < <a href="http://ieee802.org/16/ipr/patents/notices">http://ieee802.org/16/ipr/patents/notices</a> >.	

## Introduction

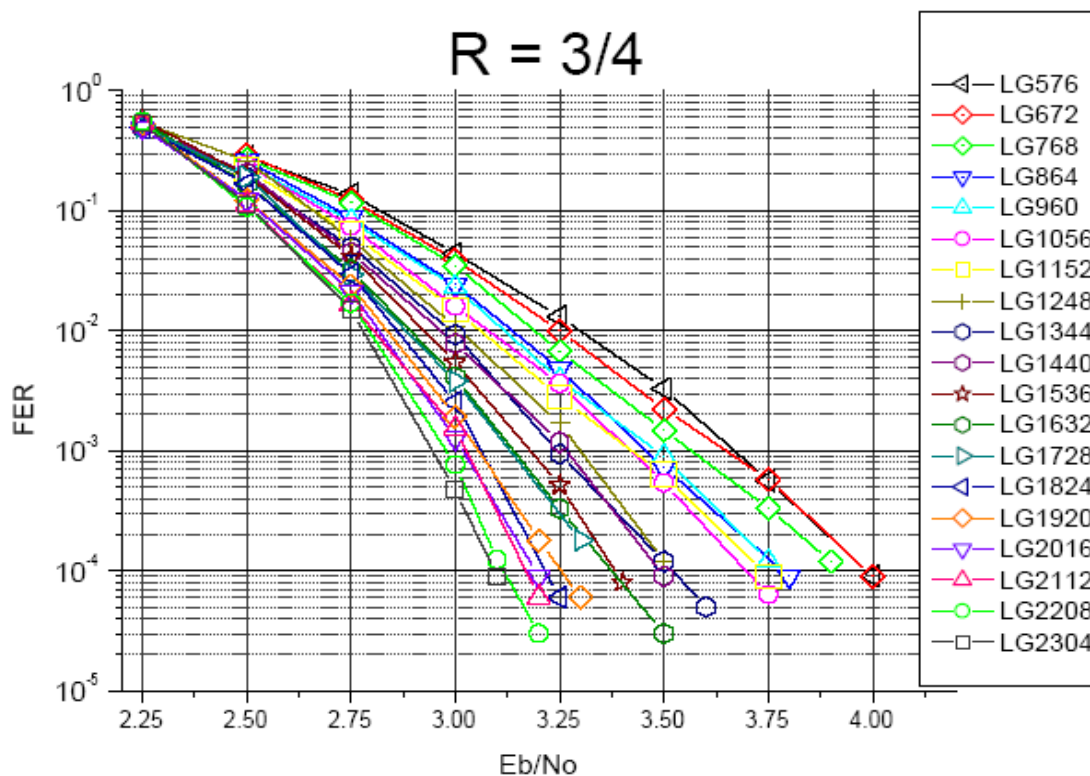
On the last session, the basic framework of LDPC codes for OFDMA PHY was adopted. So the completing of the LDPC code section is required. We propose low-complexity and high performance LDPC codes supporting all rates and codeword sizes with flexible and efficient rate adjustment. The proposed LDPC codes are based on the contribution IEEE C802.16e-04/373r1.

## Features

- Low complexity encoding and decoding
- Low memory requirement
- Good performance over AWGN channel and fading channel environment
- Simple code description

## Simulation Results

For rate 3/4, performance curves are provided for all codeword sizes. One base matrix with 12 by 48 above is used for the following simulations. To cover different codeword sizes at a given code rate, expansion is used.



## Recommended Text Changes:

Add/Modify the following text to 802.16e\_D4, adjusting the numbering as required:

### 8.4.9.2 Encoding

<add text to the end of the ‘Concatenation’ paragraph starting at line 39>

,and for the LDPC encoding scheme (see 8.4.9.2.5) the concatenation rule is defined in 8.4.2.9.5.4

### 8.4.9.2.5 Low Density Parity Check Code (optional)

#### 8.4.9.2.5.1 Code Description

The LDPC code is based on a set of one or more fundamental LDPC codes. Each of the fundamental codes is a systematic linear block code. Using the described methods of scaling and shortening in 8.4.9.2.5.3 Code rate and Block Size Adjustment, the fundamental codes can accommodate various code rates and packet sizes.

Each LDPC code in the set of LDPC codes is defined by a matrix  $\mathbf{H}$  of size  $m$ -by- $n$ , where  $n$  is the length of the code and  $m$  is the number of parity check bits in the code. The number of systematic bits is  $k=n-m$ .

The matrix  $\mathbf{H}$  is defined as

$$\mathbf{H} = \begin{bmatrix} \mathbf{P}_{0,0} & \mathbf{P}_{0,1} & \mathbf{P}_{0,2} & \cdots & \mathbf{P}_{0,n_b-2} & \mathbf{P}_{0,n_b-1} \\ \mathbf{P}_{1,0} & \mathbf{P}_{1,1} & \mathbf{P}_{1,2} & \cdots & \mathbf{P}_{1,n_b-2} & \mathbf{P}_{1,n_b-1} \\ \mathbf{P}_{2,0} & \mathbf{P}_{2,1} & \mathbf{P}_{2,2} & \cdots & \mathbf{P}_{2,n_b-2} & \mathbf{P}_{2,n_b-1} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ \mathbf{P}_{m_b-1,0} & \mathbf{P}_{m_b-1,1} & \mathbf{P}_{m_b-1,2} & \cdots & \mathbf{P}_{m_b-1,n_b-2} & \mathbf{P}_{m_b-1,n_b-1} \end{bmatrix} = \mathbf{P}^{H_b}$$

where  $\mathbf{P}_{i,j}$  is one of a set of  $z$ -by- $z$  permutation matrices or a  $z$ -by- $z$  zero matrix. The matrix  $\mathbf{H}$  is expanded from a base matrix  $\mathbf{H}_b$  of size  $m_b$ -by- $n_b$ , where  $n = z \cdot n_b$  and  $m = z \cdot m_b$ , with  $z$  an integer  $\geq 1$ . The base matrix is expanded by replacing each permutation information in the base matrix with a  $z$ -by- $z$  permutation matrix, and each  $-1$  with a  $z$ -by- $z$  zero matrix. The base matrix is an integer multiple of 24.

$\mathbf{H}_b$  is partitioned into two sections, where  $\mathbf{H}_{b1}$  corresponds to the systematic bits and  $\mathbf{H}_{b2}$  corresponds to the parity-check bits, such that  $\mathbf{H}_b = \left[ (\mathbf{H}_{b1})_{m_b \times k_b} \mid (\mathbf{H}_{b2})_{m_b \times m_b} \right]$ .



One method of encoding is to determine a generator matrix  $\mathbf{G}$  from  $\mathbf{H}$  such that  $\mathbf{G}\mathbf{H}^T = 0$ . A  $k$ -bit information block  $s_{1 \times k}$  can be encoded by the code generator matrix  $\mathbf{G}$  via the operation  $x = s\mathbf{G}$  to become an  $n$ -bit codeword  $x_{1 \times n}$ , with codeword  $x = [s \ p] = [s_0, s_1, \dots, s_{k-1}, p_0, p_1, \dots, p_{m-1}]$ , where  $p_0, p_1, \dots, p_{m-1}$  are the parity-check bits; and  $s_0, s_1, \dots, s_{k-1}$  are the systematic bits.

Encoding an LDPC code from  $\mathbf{G}$  can be quite complex. The LDPC codes are defined such that very low complexity encoding directly from  $\mathbf{H}$  is possible.

#### 8.4.9.2.5.3 Code Rate and Block Size Adjustment

The code design will be flexible to support a range of code rates and block sizes through code rate and block Adjustment of the one or more  $\mathbf{H}$  matrices of the fundamental code set. For each supported rate and block size. Some combinations of matrix selection, shortening, repetition, matrix expansion, and/or Concatenation will be used.

Different block sizes and code rates are supported through using a variable  $z$  expansion factor. In each case, the number of information bits is equal to the code rate times the coded block size  $n$ . In addition to matrix expansion, shortening is used and puncturing may be used to support some coded block sizes and code rates.

n (bits)	n (bytes)	k (bytes)			Number of subchannels		
		R=1/2	R=2/3	R=3/4	QPSK	16QAM	64QAM
576	72	36	48	54	6	3	2
672	84	42	56	63	7		
768	96	48	64	72	8	4	
864	108	54	72	81	9		3
960	120	60	80	90	10	5	
1056	132	66	88	99	11		
1152	144	72	96	108	12	6	4
1248	156	78	104	117	13		
1344	168	84	112	126	14	7	
1440	180	90	120	135	15		5
1536	192	96	128	144	16	8	
1632	204	102	136	153	17		
1728	216	108	144	162	18	9	6
1824	228	114	152	171	19		
1920	240	120	160	180	20	10	
2016	252	126	168	189	21		7
2112	264	132	176	198	22	11	
2208	276	138	184	207	23		
2304	288	144	192	216	24	12	8

Shortening may be applied to any expanded  $\mathbf{H}$  matrix by reducing the number of subchannels available for the codeword. The number of bit corresponding to the reduced number of subchannels is equal to the number of shortened bits  $L$ . The matrix  $\mathbf{H}$  is designed such that excellent performance is achieved under shortening, with different column weights interlaced between the first  $L$  columns of  $\mathbf{H}_1$  and the rest of  $\mathbf{H}_1$ . Encoding with shortening is similar to encoding without shortening, except that the current symbol set has only  $k-L$

systematic bits in the information block,  $s' = (s_0, \dots, s_{k-L-1})$ . When encoding, the encoder first prepends  $L$  zeros to  $s'$  of length  $(k-L)$ . Then the zero-padded information vector  $s = [0_L s']$  is encoded using  $H$  as if unshortened to generate parity bit vector  $p$  (length  $m$ ). After removing the prepended zeros, the code bit vector  $x = [s' p]$  is transmitted over the channel. This encoding procedure is equivalent to encoding using the last  $(n-L)$  columns of the matrix  $H$  to determine the parity-check vector  $p$ .

The  $z$  expansion factors are determined by the target block size  $n$  and the base matrix size  $n_b$ . Examples of the  $z$  expansion factors are given in the tables below. The base matrix  $n_b$  is an integer is an integer multiple of 24.

### 8.4.9.2.5.4 Packet Encoding

The encoding block size  $k$  shall depend on the number of subchannels allocated and the modulation specified for the current transmission. Concatenation of a number of subchannels shall be performed in order to make larger blocks of coding where it is possible, with the limitation of not passing the largest block under the same coding rate (the block defined by the 64-QAM modulation). The table below specifies the concatenation of subchannels for different allocations and modulations. The concatenation rule follows the subchannel concatenation rule for CC (Table 315) except that for LDPC the concatenation dose not depend on the code rate.

For any modulation and FEC rate, given an allocation of  $N_{sch}$  subchannels, we define the following parameters:

- $j$  parameter dependent on the modulation and FEC rate
- $N_{sch}$  number of allocated subchannels
- $F$   $\text{floor}(N_{sch}/j)$
- $M$   $N_{sch} \text{ mod } j$

The subchannel concatenation rule for CC in Table 315 is applied, noting that in Table 315 the parameter  $n$  is equal to  $N_{sch}$ , the parameter  $k$  is equal to  $F$ , and the parameter  $m$  is equal to  $M$ . The parameter  $j$  for LDPC is determined as shown in the table below.

Modulation	$j$
QPSK	$j=24$
16-QAM	$j=12$
64-QAM	$j=8$

Control information and packets that result in a codeword size  $n$  of less than 576 bits are encoded using convolutional coding (CC) with appropriate code rates and modulation orders, as described in section 8.4.9.2.1.