Generic PHY Specification

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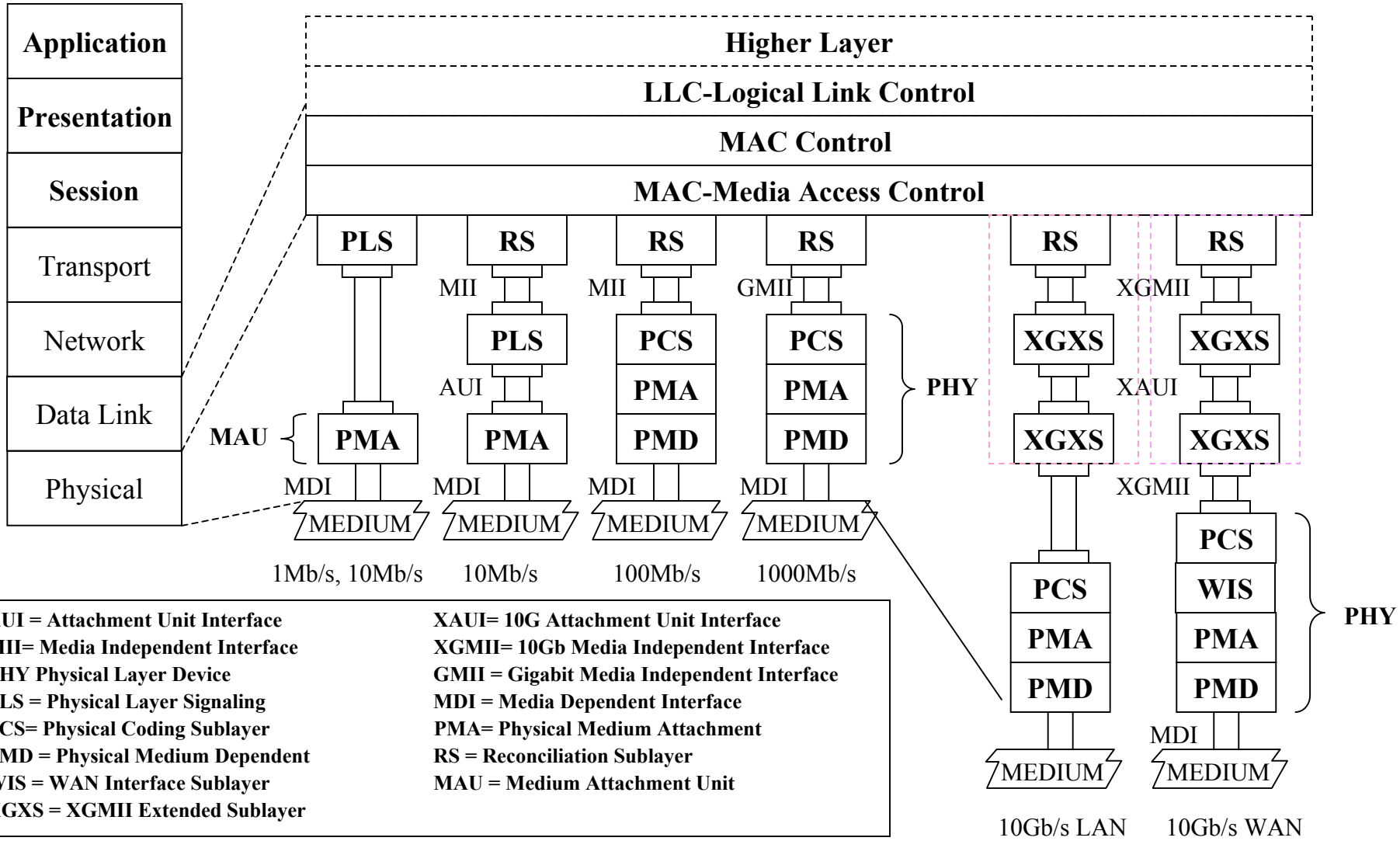
Goal

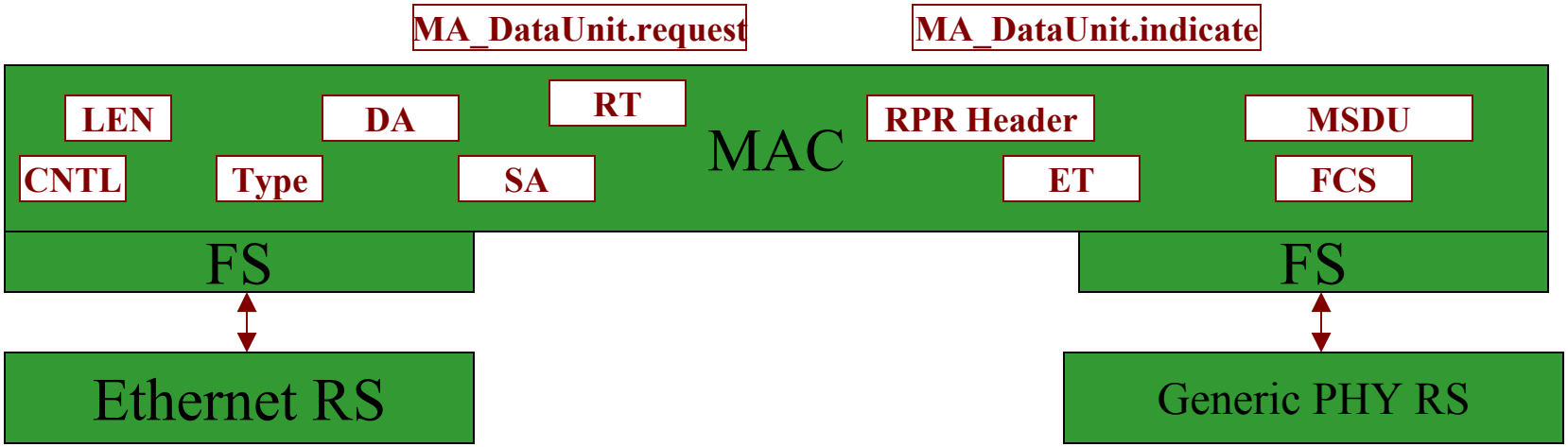
- Standard 802 and T1X1 PHY support
- Future proving the specification
  - Generic Framing Process (GFP)
    - T1X1 and ITU
    - SONET/SDH
    - OTN
- Define frame format on medium
- Define Physical specification
  - Various applications

802 MAC Model:ethernet



AUI = Attachment Unit Interface
MII= Media Independent Interface
PHY Physical Layer Device
PLS = Physical Layer Signaling
PCS= Physical Coding Sublayer
PMD = Physical Medium Dependent
WIS = WAN Interface Sublayer
XGXS = XGMII Extended Sublayer
XAUI= 10G Attachment Unit Interface
XGMII= 10Gb Media Independent Interface
GMII = Gigabit Media Independent Interface
MDI = Media Dependent Interface
PMA= Physical Medium Attachment
RS = Reconciliation Sublayer
MAU = Medium Attachment Unit

Frame Formats



MII/GMII/XGMII

Preamble	SFD	DA	SA	RT	RPR Header	cHEC	ET	payload	FCS

10M | 100M | 10G LAN | 10G WAN } **PHY**

Preamble	SFD	DA	SA	RT	RPR Header	cHEC	ET	payload	FCS

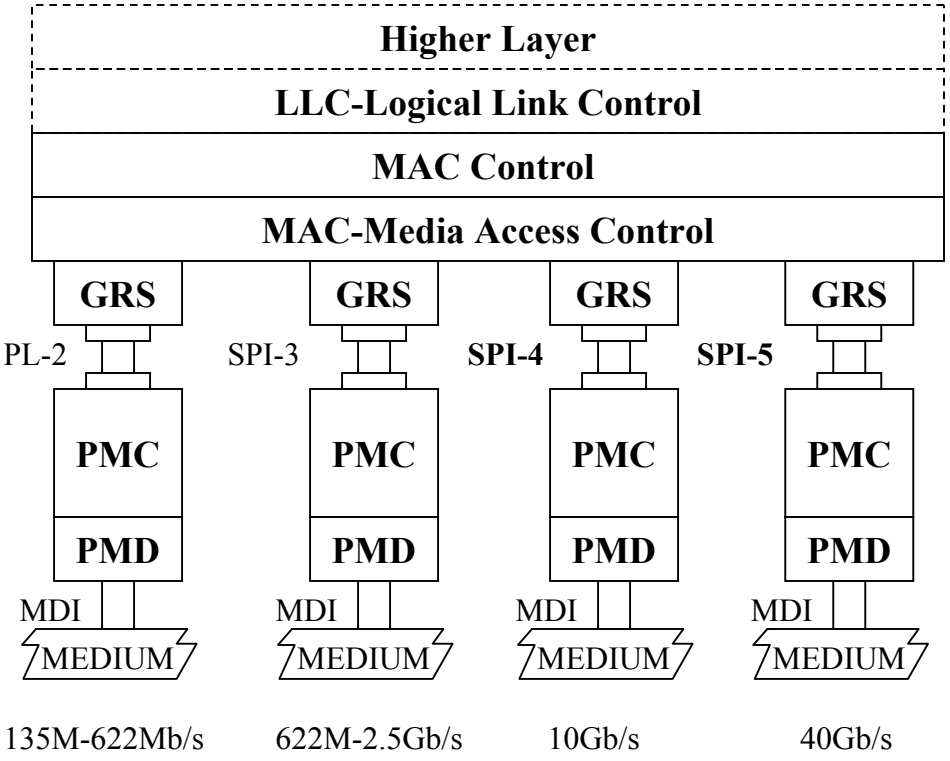
SPI-n/PL2

LEN	cHEC	DA	SA	RT	RPR Header	cHEC	payload	FCS

GFP Frame delineation
Coding
SONET SDH | OTN } **PHY**

Type	cHEC	LEN	cHEC	DA	SA	RT	RPR Header	cHEC	payload	FCS

Generic Reconciliation Sublayer



- Generic RS
  - Generic frame structure
  - Generic Packet transfer interface
- Physical Media Component (PMC)
  - Word level flow control
  - $X^{43}+1$ scrambling
  - Framing
    - Idle frame
    - Frame Delineation
      - HEC
  - SONET/SDH frame
- PMD
  - CDR

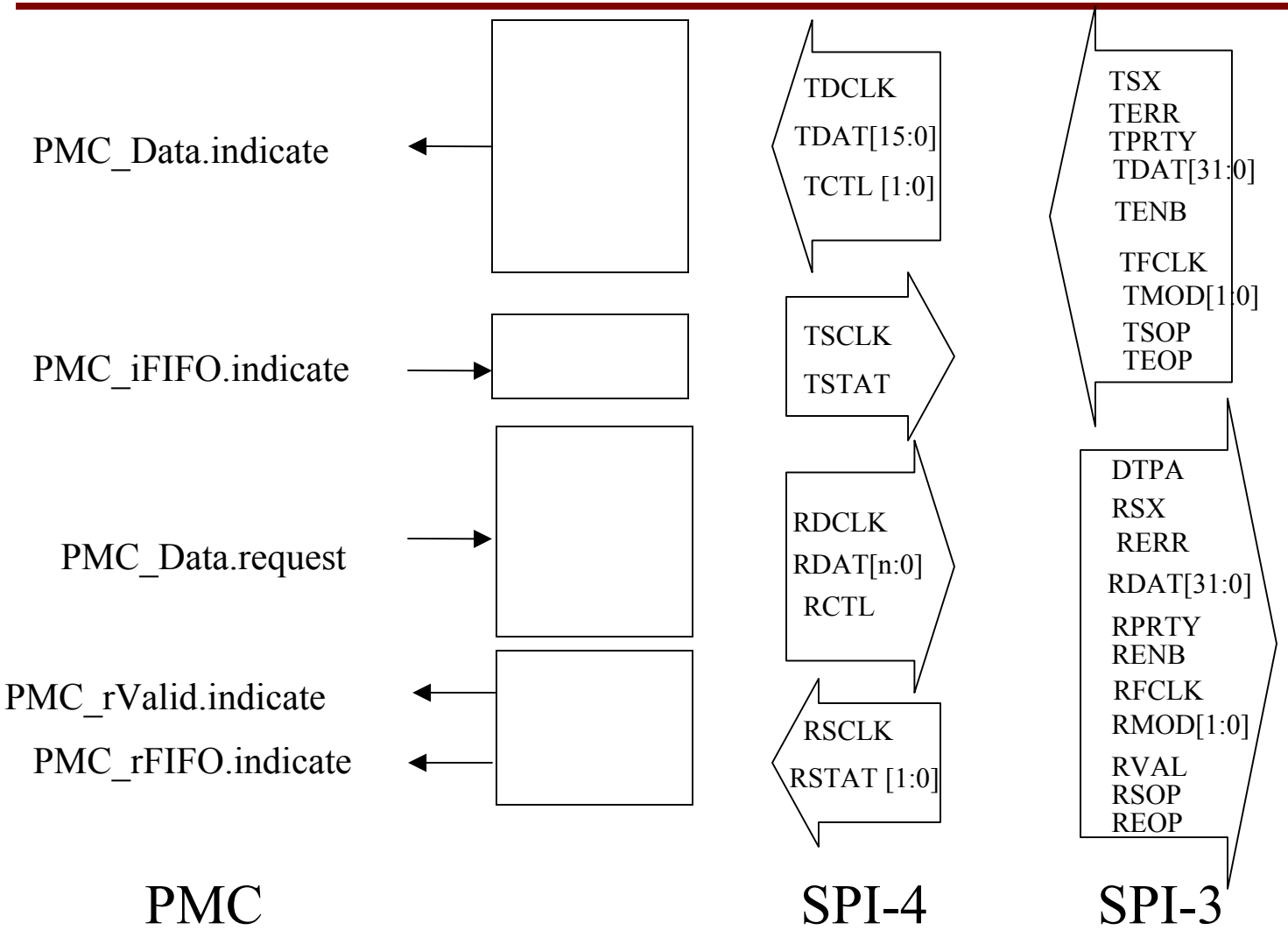
RS Physical Specifications

- 40G SPI-5
- 10G SPI-4 phase 2
  - 16 bits
  - 800 M clock
  - LVDS
- 2.5G SPI-3 and below
  - 8/32 bit interface
  - Up to 104 MHz clock
  - LVTTL
- 622 and below SPI-3 8 bits
  - PL-2
  - LVTTL

Support for Logical channels

Word level flow control

Mapping of Primitives



Management Issues

- No Management interface to PHY
- Management object for interface
  - Clock speed and bus width
  - Logical channel provision
  - FIFO provision
- Indications for PHY stats
  - FIFO status
  - Rx fault stats
  - Remote fault stats, no hw consequence action
  - Interface types SPI-5, SPI-4, and SPI-3/PL2
  - For SPI-3/PL2
    - Interface clock selection
    - Interface Bus width

Conclusion

- Separate Reconciliation sublayer from ethernet
- Generic RS to support for emerging Standard for SONET/SDH and other Generic packet Process:
  - OTN
- For various ring BW
  - Physical specifications: SPI-n and PL-2