1. Physical Sublayer Interface

1.1 SONNET/SDH Physical Sublayer

1.1.1 Overview

This clause defines the logical and electrical characteristics for the SPI interfaces between the 802.17 MAC and the SONET PHY. There are two interfaces defined (SPI-3, and SPI-4), each intended for different ranges of data transfer rates. These interface definitions and their details are taken directly from the Optical Internetworking Forum (OIF) documents (OIF-SPI4-02.0 and OIF-SPI3-01.0).

1.1.1.1 summary of Major concepts

The System Packet Interfaces (SPIs) defined by the OIF are pin efficient point-to-point packet transfer interfaces intended for full duplex data transfer rates between approximately 800 Mb/s and 10 Gb/s using separate transmit and receive data signals. These interfaces support logical channels with individual word-level flow control. The flow control is done out-of-band to allow for uni-directional operation.

1.1.1.2 Applications

The implementation of these interfaces may assume any of the following forms:

1) Chip-to-chip interface implemented with traces on a printed circuit board
2) A motherboard to daughterboard interface between two or more printed circuit boards
3) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector

1.1.1.3 Rates of operations

The SPI-3 interface can be implemented with either a 8-bit or 32-bt data buses and is specified to run at clock frequencies of upto 104 MHz. This allows full duplex data transfer rates suitable for 622 Mb/s or 2.5Gb/s applications.

The SPI-4 interface is specified to be implemented with a 16-bit data bus and clock frequencies of at least 311 Mhz using both edges of the clock to transfer data. This allows full duplex data transfer rates suitable for 10Gb/s applications.

1.1.1.4 Allocation of Functions

The allocation of functions in the SPI interfaces is such that it readily lends itself to implementation in both PHY and MAC sublayer entities.

1.1.1.5 Relationship Between SPI-n's

SPI-3 and SPI-4 are similar in overall function and structure including much of the signal naming. However, SPI-4 includes additional functions and differences with respect to implementation which are primarily due to the

differences in clock frequency of operation and data rate capabilities (eg. deskew functions, dual edge clocking, calendar etc.)

1.1.1.6 Frame structures

GFP

(POS)

1.1.1.7 Signaling function specifications

1.1.1.8 management functions

1.1.2 OC-192/ STM-64 (SPI-4P2)

SPI-4 is an interface for packet and cell transfer between a physical layer (PHY) device and a link layer device, for aggregate bandwidths of OC-192 ATM and Packet over SONET/SDH (POS), as well as 10 Gb/s Ethernet applications.

On both the transmit and receive interfaces, FIFO status information is sent separately from the corresponding data path. By taking FIFO status information out-of-band, it is possible to decouple the transmit and receive interfaces so that each operates independently of the other. Such an arrangement makes POS-PHY L4 suitable not only for bidirectional but also for unidirectional link layer devices.

In both the transmit and receive interfaces, the packet's address, delineation information and error control coding is sent in-band with the data.

SPI-4 has the following general characteristics:

° Point-to-point connection (i.e., between single PHY and single Link Layer device).
° Support for 256 ports (suitable for STS-1 granularity in SONET/SDH applications (192 ports) and Fast Ethernet granularity in Ethernet applications (100 ports)).
° Transmit / Receive Data Path:
- 16 bits wide.
- In-band port address, start/end-of-packet indication, error-control code.
- LVDS I/O (IEEE 1596.3 – 1996 [1], ANSI/TIA/EIA-644-1995 [2]).
- 622 Mb/s minimum data rate per line.
- Source-synchronous double-edge clocking, 311 MHz minimum.
° Transmit / Receive FIFO Status Interface:
- LVTTL I/O or optional LVDS I/O (IEEE 1596.3 – 1996 [1], ANSI/TIA/EIA-644-1995 [2]).
- Maximum 1/4 data path clock rate for LVTTL I/O, data path clock rate (double-edge clocking) for LVDS I/O.
- 2-bit parallel FIFO status indication.
- In-band Start-of-FIFO Status signal.
- Source-synchronous clocking.

1.1.2.1 Signaling function specifications

Data and control lines are driven off the rising and falling edges of the clock [TDCLK].

1.1.2.2 TDCLK (Transmit Data Clock)

TDCLK is a clock associated with TDAT and TCTL. TDCLK provides the datapath source-synchronous double-edge clocking with a minimum frequency of 311 MHz. Data and control lines are driven off the rising and falling edges of the clock. TDCLK is sourced by the MAC to the PHY.

1.1.2.3 TDAT[15:0] Transmit Data

TDAT is a 16-bit bus used to carry payload data and in-band control words from the Link Layer to the PHY device. A control word is present on TDAT when TCTL is high. The minimum data rate for TDAT is 622 Mb/s.

1.1.2.4 TCTL (Transmit Control)

TCTL is high when a control word is present on TDAT, otherwise it is low. TCTL is sourced by the MAC to the PHY.

1.1.2.5 TSCLK (Transmit Status Clock)

TSCLK is a clock associated with TSTAT providing source-synchronous clocking. For LVTTL I/O a maximum clockrate restraint is ¼ that of the data path clock rate. LVDS I/O allows a maximum of that equal to the data path clock (double-edge clocking).

1.1.2.6 TSTAT[1:0] (Transmit FIFO Status)

TSTAT is a 2-bit bus used to carry round-robin FIFO status information, along with associated error detection and framing. The maximum data rate for TSTAT is dependent on the I/O type, either LVDS or LVTTL, and is limited to its respective TSCLK restraints. TSTAT is sourced by the PHY to the MAC. The FIFO status formats are:

TSSTAT[1:0] = “11”	Reserved for framing or to indicate a disabled status link.
TSSTAT[1:0] = “10”	SATISFIED
TSSTAT[1:0] = “01”	HUNGRY
TSSTAT[1:0] = “00”	STARVING

1.1.2.7 RDCLK (Receive Data Clock)

RDCLK is a clock associated with RDAT and RCTL. RDCLK provides the datapath source-synchronous double-edge clocking with a minimum frequency of 311 MHz. Data and control lines are driven off the rising and falling edges of the clock. RDCLK is sourced by the PHY to the MAC.

1.1.2.8 RDAT[15:0] (Receive Data)

RDAT is a 16-bit bus which carries payload data and in-band control from the PHY to the Link Layer device. A control word is present on RDAT when RCTL is high. The minimum data rate for RDAT is 622 Mb/s.

1.1.2.9 RCTL (Receive Control)

RCTL is high when a control word is present on RDAT, otherwise it is low. RCTL is sourced by the PHY to the MAC.

1.1.2.10 RSCLK (Receive Status Clock)

RSCLK is a clock associated with RSTAT providing source-synchronous clocking. RSCLK is sourced by the Mac to the PHY. LVDS I/O allows a maximum of that equal to the data path clock (double-edge clocking).

1.1.2.11 RSTAT[1:0] (Receive FIFO Status)

RSTAT is a 2-bit bus used to carry round-robin FIFO status information, along with associated error detection and framing. The maximum data rate for RSTAT is dependent on the I/O type, either LVDS or LVTTL, and is limited to its respective RSCLK restraints. RSTAT is sourced by the Mac to the PHY. The FIFO status formats are:

TSSTAT[1:0] = "11" Reserved for framing or to indicate a disabled status link.
TSSTAT[1:0] = "10" SATISFIED
TSSTAT[1:0] = "01" HUNGRY
TSSTAT[1:0] = "00" STARVING

1.1.2.12 Management Functions

Parameter	Definition	P	CH	Units
CALENDAR[i]	Port address at calendar location i.	Yes	I	(N/A)
CALENDAR_LEN	Length of the calendar sequence.	Yes	I	(N/A)
CALENDAR_M	Number of times calendar sequence is repeated between insertions of framing pattern.	Yes	I	(N/A)
MAX_CALENDAR_LEN	Maximum supported value of MA_CALENDAR_LEN	No	I	(N/A)
MaxBurst1	Maximum number of 16 byte blocks that the FIFO can accept when FIFO Status channel indicates Starving.	Yes	C/I	16 byte blocks
MaxBurst2	Maximum number of 16 byte blocks that the FIFO can accept when FIFO Status channel indicates Hungry. MaxBurst2 <= MaxBurst1	Yes	C/I	16 byte blocks
α	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles.	Yes	I	(N/A)
DATA_MAX_T	Maximum interval between scheduling of training sequences on Data Path interface.	Yes	I	Cycles
FIFO_MAX_T	Maximum interval between scheduling of training sequences on FIFO Status Path interface.	Yes	I	Cycles

P = Provisionable, CH = Per channel (C) pr per interface (I)

Upon reset, the FIFOs in the datapath receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, but before active traffic is generated, the data transmitter shall send continuous training patterns. Transmission of training patterns shall continue until valid information is received on the FIFO Status Channel. The receiver shall ignore all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisionable number of consecutive correct DIP-4 codewords are seen. Loss of synchronization may be reported after a provisionable number of consecutive incorrect DIP- 4 codewords is detected.

After reset but before active traffic is generated, the FIFO Status Channel transmitter shall send a continuous "1 1" framing pattern for LVTTL implementations, or continuous training patterns for optional LVDS implementations. Once the corresponding data channel has achieved synchronization, and a calendar has been provisioned, it may begin transmission of FIFO Status information. Once the data transmitter has received valid FIFO Status information (as indicated, for example, by a sufficient number of consecutively correct DIP- 2 codewords), it may begin transmission of data bursts to channels that have been provisioned and have space available.

In the event that the data path receiver is reset but the transmitter is still active, events at the receiver follow the same behavior as above. It shall ignore all incoming data until it has observed the training pattern and acquired synchronization with the data. It shall also send a continuous "1 1" framing pattern for LVTTL implementations (or continuous training patterns for optional LVDS implementations) on its FIFO Status Channel, cancelling previously granted credits and setting them to zero. In this case the transmitter should send continuous training patterns to facilitate reacquistion by the receiver.

In the event that the data path transmitter is reset but the receiver is still active, events at the transmitter follow the same behavior as above. The transmitter shall send continuous training patterns until a calendar is configured and valid status information is received on the FIFO Status Channel. At the same time, the receiver may have lost synchronization with the data, and begun sending continuous framing patterns (or continuous training patterns for optional LVDS implementations) on the FIFO Status Channel. Once the data transmitter has received valid FIFO Status information (as indicated, for example, by a sufficient number of consecutively correct DIP- 2 codewords), it may begin transmission of data bursts to channels that have been provisioned and have space available.

1.1.2.13 Functional Specification

1.1.2.13.1 Data Path

The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted only between burst transfers; once a transfer has begun, data words are sent uninterrupted until end-of-packet or a multiple of 16 bytes is reached. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and training patterns.

The minimum and maximum supported packet lengths are determined by the application. For ease of implementation however, successive start-of-packets must occur not less than 8 cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

A control word format is use in both the transmit and receive interfaces:

Bit	Label	Description
15	Type	Control Word Type. 1: payload control word (payload transfer will immediately follow the control word). 0: idle or training control word (otherwise).
14:13	EOPS	End-of-Packet (EOP) Status. 0 0: Not an EOP. 0 1: EOP Abort (application-specific error condition). 1 0: EOP Normal termination, 2 bytes valid. 1 1: EOP Normal termination, 1 byte valid. EOPS is valid in the first control word following a burst, otherwise is ignored and set to "0 0".
12	SOP	Start-of-Packet. 1: Payload transfer immediately following the control word corresponds to the start of a packet. 0: Otherwise. Set to 0 in all idle and training control words.
11:4	ADR	Port Address. 8-bit port address of the payload data transfer immediately following the control word. None of the addresses are reserved (all are available for payload transfer). Set to all zeroes in all idle control words. Set to all ones in all training control words.

3:0	DIP-4	4-bit Diagonal Interleaved Parity. 4-bit odd parity computed over the current control word and the immediately preceding data words (if any) following the last control word.

TCTL/RCTL is high when TDAT/RDAT contain control words. Idle periods correspond to back-to-back control words.

1.1.2.13.2 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the PHY to the Link Layer device, and over the RSTAT link from the Link Layer to the PHY device. Implementation of the FIFO status channel for the transmit interface is mandatory; the corresponding implementation for the receive interface is optional. If both status channels are implemented, they shall operate independently of each other.

The FIFO status of each port is encoded in a 2-bit data structure, whose format is defined by:

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED Indicates that the corresponding port's FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks or the remainder of what was previously granted (whichever is greater) may be sent to the corresponding port until the next status update.
0	0	STARVING Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update.

1.1.2.13.3 Higher Bandwidth Operation

Applications which require higher FIFO Status Channel bandwidths than feasible with LVTTL I/O, may optionally use LVDS I/O instead. If LVDS I/O is used, double-edge clocking is used on TSCLK and RSCLK, running at the same rate as the corresponding data path rate. The framing structure and operation of TSTAT[1:0] and RSTAT[1:0] remain unchanged.

A training sequence is scheduled to be sent at least once every preconfigured bounded interval on both the transmit and receive FIFO Status interfaces. These training sequences may be used by the receiving end of each interface for deskewing bit arrival times on the FIFO status and control lines. The training sequence consists of 1 idle control word followed by one or more repetitions of a 20-word training pattern consisting of 10 (repeated) training control words and 10 (repeated) training data words.

1.1.2.14 Signal Timing Characteristic

1.1.2.14.1 Data Path

Two sets of data path timing parameters are specified to support different bit alignment schemes at the receiver. “Static alignment" is where the receiver latches data at a fixed point in time relative to clock (requiring a more precisely specified sampling window). “Dynamic alignment” is where the receiver has the capability of centering the data and control bits relative to clock.

TDCLK / RDCLK frequency is a minimum of f_D = 311 MHZ with a duty cycle of 45 – 55%.

Data Path Interface Timing (Static Alignment):

The worst-case cummulative skew and jitter contribution of 790 ps. It has 20 – 80% rise and fall times between 100ps up to $0.36/2f_D$.

Data Path Interface Timing (Dynamic Alignment):

Maximum jitter of 0.1/2fD on TDCLK/RDCLK. Maximum jitter of $0.24/2f_D$ on TDAT/RDAT/TCTL/ RCTL of $0.24/2f_D$. It has 20 – 80% rise and fall times between 100ps up to $0.36/2f_D$.

1.1.2.14.2 FIFO Status Channel

The parameters for the FIFO Status Channel are dependent on the I/O type, either LVTTL or LVDS.

LVTTL I/O Timing:

TSCLK has a maximum frequency of $f_D/4$ with a duty cycle between 40 – 60%. TSTAT Setup time to TSCLK (RSTAT Setup time to RSCLK) is a minimum of 2 ns. TSTAT Hold time to TSCLK (RSTAT Hold time to RSCLK) is a minimum of 0.5 ns

LVDS I/O Timing:

Refer to data path timing.

1.1.2.15 Electrical Characteristics

1.1.3 OC-48/ STM-16 and OC-12/STM-4 (SPI-3)

SPI-3 defines the requirements for interoperable single-PHY (one PHY layer device connected to one Link Layer device) and multi-PHY (multiple PHY layer devices connected to one Link Layer device) applications. It stresses simplicity of operation to allow forward migration to more elaborate PHY and
Link Layer devices.

Two bus widths are provided to support multiple data transfer rates. The 8-bit data bus is used for OC-12/STM-4 applications and a 32-bit bus is used for OC-48/STM-16 applications.

1.1.3.1 Signaling function specifications

All signals are expected to be updated and sampled using the rising edge of the transmit FIFO clock TFCLK.

1.1.3.1.1 TFCLK (transmit clock)

TFCLK is a continuous clock used to synchronize data transfer transactions between the LINK Layer device and the PHY layer device. TFCLK may cycle at a rate up to 104 MHz. TFCLK is sourced by the MAC to the PHY.

1.1.3.1.2 TERR (transmit error Indicator)

TERR is used to indicate that there is an error in the current packet. TERR should only be asserted when TEOP is asserted; it is considered valid only when TENB is asserted.

1.1.3.1.3 TENB (transmit write enable)

TENB is used to control the flow of data to the transmit FIFOs. When TENB is high the TDAT, TMOD, TSOP, TEOP and TERR signals are invalid and should be ignored by the PHY. The TSX signal is valid and is processed by the PHY when TENB is high. When TENB is low the TDAT, TMOD, TSOP, TEOP and TERR signals are valid and are processed by the PHY. The TSX signal is ignored by the PHY when TENB is low.

1.1.3.1.4 TDAT[31:0] (transmit packet data bus)

TDAT is an 8-bit or 32-bit bus which carries the packet octets that are written to the selected transmit FIFO and the in-band port address to select the desired transmit FIFO. The TDAT bus is considered valid only when TENB is asserted. Data is transmitted in big endian order on TDAT.

1.1.3.1.5 TMOD[1:0] (transmit word modulo)

TMOD is required only when TDAT is 32-bits. TMOD indicates the number of valid bytes of data in TDAT. The TMOD bus should always be zero except during the last word transfer of a packet on TDAT. When TEOP is asserted the number of valid packet data bytes on TDAT is decoded from TMOD as:

TMOD[1:0] = “00” TDAT[31:0] is valid
TMOD[1:0] = “01” TDAT[31:8] is valid
TMOD[1:0] = “10” TDAT[31:16] is valid
TMOD[1:0] = “11” TDAT[31:24] is valid

TMOD is considered valid only when TENB is asserted.

1.1.3.1.6 TPRTY (transmit bus parity)

TPRTY indicates the parity calculated over the TDAT bus. TPRTY is considered valid only when TENB or TSX is asserted. The parity calculation is such that odd parity is indicated on this signal.

1.1.3.1.7 TSX (transmit start of transfer)

TSX indicates when the in-band port address is present on the TDAT bus. When TSX is high and TENB is high, the value of TDAT is the address of the transmit FIFO to be selected. Subsequent data transfers on the TDAT bus will

fill the FIFO specified by this in-band address. For single channel PHY devices the TSX signal is optional. TSX is considered valid only when TENB is not asserted.

1.1.3.1.8 TSOP (transmit start of packet)

TSOP is used to delineate the packet boundaries on the TDAT bus. When TSOP is high the start of the packet is present on the TDAT bus. TSOP is required to be present at the beginning of every packet and is considered valid only when TENB is asserted.

1.1.3.1.9 TEOP (transmit end of packet)

TEOP is used to delineate the packet boundaries on the TDAT bus. When TEOP is high, the end of the packet is present on the TDAT bus. TEOP is required to be present at the end of every packets and is considered valid only when TENB is asserted.

1.1.3.1.10 TADR (transmit PHY Address)

TADR bus is used with the PTPA signal to poll the transmit FIFO's packet available status. When TADR is sampled on the rising edge of TFCLK by the PHY the polled packet available indication PTPA is updated with the status of the channel specified by the TADR address on the following rising edge of TFCLK.

1.1.3.1.11 DTPA (direct transmit packet available)

DTPA bus provides direct status indication for the corresponding ports in the PHY device. DTPA transitions high when a predefined minimum number of bytes is available in its transmit FIFO. Once high, the DTPA signal indicates that its corresponding transmit FIFO is not full. When DTPA transitions low it indicates that its transmit FIFO is full or near full. DTPA is updated on the rising edge of TFCLK.

1.1.3.1.12 RFCLK (receive FIFO write clock)

RFCLK is a continuous clock used to synchronize data transfer transactions between the MAC and the PHY. RFCLK may cycle at a rate up to 104 MHz.

1.1.3.1.13 RVAL (receive data valid)

RVAL indicates the validity of the receive data. RVAL is low between transfers and when RSX is asserted. It is also low when the PHY pauses a transfer due to an empty receive FIFO. When a transfer is paused by holding RENB high RVAL will hold its value unchanged although no new data will be present on RDAT until the transfer resumes. When RVAL is high the RDAT, RMOD, RSOP, REOP and RERR signals are valid. When RVAL is low, the RDAT, RMOD, RSOP, REOP and RERR signals are invalid and must be disregarded. The RSX signal is valid when RVAL is low.

1.1.3.1.14 RENB (receive read enable)

The RENB signal is used to control the flow of data from the receive FIFOs. During data transfer, RVAL must be monitored as it will indicate if the RDAT, RPRTY, RMOD, RSOP, REOP, RERR and RSX are valid. The system may deassert RENB at anytime if it is unable to accept data from the PHY device. When RENB is sampled low by

the PHY device a read is performed from the receive FIFO and the RDAT, RPRTY, RMOD, RSOP, REOP, RERR, RSX and RVAL signals are updated on the following rising edge of RFCLK. When RENB is sampled high by the PHY device a read is not performed and the RDAT, RPRTY, RMOD, RSOP, REOP, RERR, RSX and RVAL remain unchanged on the following rising edge of RFCLK.

1.1.3.1.15 RDAT[31:0] (receive packet data bus)

RDAT is an 8-bit or 32-bit bus which carries the packet octets that are read from the receive FIFO and the in-band port address of the selected receive FIFO. RDAT is considered valid only when RVAL is asserted. Data is received in big endian order.

1.1.3.1.16 RPRTY (receive parity)

RPRTY signal indicates the odd parity calculated over the RDAT bus.

1.1.3.1.17 RMOD[1:0] (receive word modulo)

RMOD is required only when RDAT is a 32-bit bus. RMOD indicates the number of valid bytes of data in RDAT. The RMOD bus should always be zero except during the last word transfer of a packet on TDAT. When REOP is asserted the number of valid packet data bytes on RDAT is decoded from RMOD as:

RMOD[1:0] = “00”	RDAT[31:0] is valid
RMOD[1:0] = “01”	RDAT[31:8] is valid
RMOD[1:0] = “10”	RDAT[31:16] is valid
RMOD[1:0] = “11”	RDAT[31:24] is valid

RMOD is considered valid only when RVAL is asserted

1.1.3.1.18 REOP (receive end of packet)

REOP is used to delineate the packet boundaries on the RDAT bus. When REOP is high, the end of the packet is present on the RDAT bus. REOP is required to be present at the end of every packets and is considered valid only when RVAL is asserted.

1.1.3.1.19 RERR (receive error indicator)

RERR is used to indicate that the current packet is in error. RERR shall only be asserted when REOP is asserted. Conditions that can cause RERR to be set may be, but are not limit to, FIFO overflow, abort sequence detection and FCS error.

1.1.3.1.20 RSX (receive start of transfer)

RSX indicates when the in-band port address is present on the RDAT bus. When RSX is high, the value of RADAT[7:0] is the address of the receive FIFO to be selected by the PHY. Subsequent data transfers on the RDAT bus will be from the FIFO specified by this in-band address. For single channel PHY devices the RSX signal is optional. For multi-port PHY devices, RSX must be asserted at the beginning of each transfer. When RSX is high RVAL must be low.

1.1.3.1.21 management functions

Management functions for this interface involves setting of FIFO thresholds used as triggers for flow control indicators.

1.1.3.1.22 Functional specification (transmit direction)

The SPI-3 packet interface supports transmit and receive data transfers at clock rates independent of the line bit rate. As a result, PHY layer devices must support packet rate decoupling using FIFOs.

To ease the interface between the Link Layer and PHY layer devices and to support multiple PHY layer interfaces, FIFOs are used. Control signals are provided to both the Link Layer and PHY layer devices to allow either one to exercise flow control. Since the bus interface is point-to-point, the receive interface of the PHY device pushes data to the Link Layer device. For the transmit interface, the packet available status granularity is byte-based.

In the receive direction, when the PHY layer device has stored an end-ofpacket (a complete small packet or the end of a larger packet) or some predefined number of bytes in its receive FIFO, it sends the in-band address followed by FIFO data to the Link Layer device. The data on the interface bus is marked with the valid signal (RVAL) asserted. A multi-port PHY device with multiple FIFOs would service each port in a round-robin fashion when sufficient data is available in its FIFO. The Link Layer device can pause the data flow by deasserting the enable signal (RENB).

In the transmit direction, when the PHY layer device has space for some predefined number of bytes in its transmit FIFO, it informs the Link Layer device by asserting a transmit packet available (TPA). The Link Layer device can then write the in-band address followed by packet data to the PHY layer device using an enable signal (TENB). The Link Layer device shall monitor TPA for a high to low transition, which would indicate that the transmit FIFO is near full (the number of bytes left in the FIFO can be user selectable, but must be predefined), and suspend data transfer to avoid an overflow. The Link Layer device can pause the data flow by deasserting the enable signal (TENB).

SPI-3 defines both byte-level and packet-level transfer control in the transmit direction. In byte-level transfer, FIFO status information is presented on a cycle-by-cycle basis. With packet-level transfer, the FIFO status information applies to segments of data. When using byte level transfer, direct status indication must be used. In this case, the PHY layer device provides the transmit packet available status of the selected port (STPA) in the PHY device. As well, the PHY layer device may provide direct access to the transmit packet available status of all ports (DTPA[]) in the PHY device if the number of ports is small. With packet level transfer, the Link Layer device is able to do status polling on the transmit direction. The Link Layer device can use the transmit port address TADR[] to poll individual ports of the PHY device, which all respond on a common polled (PTPA) signal.

Since the variable size nature of packets does not allow any guarantee as to the number of bytes available, in both transmit and receive directions, a selected PHY transmit packet available is provided on signal STPA and a receive data valid on signal RVAL. STPA and RVAL always reflect the status of the selected PHY to or from which data is being transferred. RVAL indicates if valid data is available on the receive data bus and is defined such that data transfers can be aligned with packet boundaries.

Physical layer port selection is performed using in-band addressing. In the transmit direction, the Layer device selects a PHY port by sending the address on the TDAT[] bus marked with the TSX signal active and TENB signal inactive. All subsequent TDAT[] bus operations marked with the TSX signal inactive and the TENB active will be packet data for the specified port.

In the receive direction, the PHY device will specify the selected port by sending the address on the RDAT[] bus marked with the RSX signal active and RVAL signal inactive. All subsequent RDAT[] bus operations marked with RSX inactive and RVAL active will be packet data from the specified port.

Both byte-level and packet-level modes are specified in this standard in order to support the current low density multi-port physical layer devices and future higher density multi-port devices. When the number of ports in the physical layer device is limited, byte-level transfer using DTPA[] signals provides a simpler implementation and reduces the need for addressing pins. In this case, direct access will start to become unreasonable as the number of ports increase. Packet-level transfer provides a lower pin count solution using the TADR[] bus when the number of ports is large. In-band addressing ensures the protocol remains consistent between the two approaches. However, the final choice left to the system designers and physical layer device manufacturers to select which approach best suits their desired applications.

Packets shall be written into the transmit FIFO and read from the receive FIFO using a defined data structure. Octets are written in the same order they are to be transmitted or they were received on the SONET line. Within an octet, the MSB (bit 7) is the first bit to be transmitted. The SPI-3 specification does not preclude the transfer of 1-byte packets. In this case, both start of packet and end of packet signals shall be asserted simultaneously.

For packets longer than the PHY device FIFO, the packet must be transferred over the bus interface in sections. The number of bytes of packet data in each section may be fixed or variable depending on the application. In general, the Receive Interface will round-robin between receive FIFOs with fill levels exceeding a programmable high water mark or with at least one end of packet stored in the FIFO. The Receive Interface would end the transfer of data when an end of a packet is transferred or when a programmable number of bytes have been transferred. The Link Layer device may send fixed size sections of packets on the Transmit Interface or use the TPA signal to determine when the FIFO reaches a full level.

The in-band address is specified in a single clock cycle operation marked with the RSX/TSX signals. The port address is specified by the TDAT[7:0]/RDAT[7:0] signals. The address is the numeric value of the TDAT[7:0]/RDAT[7:0] signals where bit 0 is the least significant bit and bit 7 is the most significant bit. Thus, up to 256 ports may be supported by a single interface. With a 32-bit interface, the upper 24 bits shall be ignored.

1.1.3.1.23 Functional Specification (receive direction)

The receive FIFO shall have a programmable threshold defined in terms of the number of bytes of packet data stored in the FIFO. A multi-port PHY device must service each receive FIFO with sufficient packet data to exceed the threshold or with an end of packet. The PHY should service the required FIFOs in a round-robin fashion. The type of round-robin algorithm will depend on the various data rates supported by the PHY device and is outside this specification.

The amount of packet data transferred, when servicing the receive FIFO, is bounded by the FIFO's programmable threshold. Thus, a transfer is limited to a maximum of 256 bytes of data (64 cycles for a 32-bit interface or 256 cycles for an 8-bit interface) or until an end of packet is transferred to the Layer device. At the end of a transfer, the PHY device will round-robin to the next receive FIFO.

The PHY device should support a programmable minimum pause of 0 or 2 clock cycles between transfers. A pause of 0 clock cycles maximizes the throughput of the interface. A pause of 2 clock cycles allows the Layer device to pause between transfers.

1.1.3.1.24 Signal timing characteristic

TFCLK Frequency is specified to be 104 MHz. TFCLK duty cycle is min 40% and max 60%.

Setup time relative to TFCLK for TENB, TDAT, TPRTY, TSOP, TEOP, TMOD, TERR, TSX and TADR is 2 ns minimum. Hold time relative to TFCLK for the same set of signals is 0.5 ns minimum.

Validity of DTPA, STPA, PTPA relative to the rising edge of TFCLK is 1.5ns minimum and 6.0 ns maximum.

RFCLK Frequency is specified to be 104 MHz. RFCLK duty cycle is min 40% and max 60%.

Setup time relative to RFCLK for RENB is 2 ns minimum. Hold time relative to RFCLK for RENB is 0.5 ns minimum.

Validity of RDAT, RPRTY, RSOP, REOP, RMOD, RERR, RVAL, and RSX relative to the rising edge of RFCLK is 1.5 ns minimum and 6.0 ns maximum.

1.1.3.1.25 Electrical Characteristics

1.1.3.1.26

1.1.4 OC-3/ STM-1 (SPI-2)

1.1.4.1 Signaling function specifications

1.1.4.1.1 management functions

1.1.4.1.2 Functional specification

1.1.4.1.3 Signal timing characteristic

1.1.4.1.4 Electrical Characteristics