Framework for Burst Mode Data Synchronization

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Goals of Framework

- Describe the logical elements of the ONU PCS layer needed for 10G burst mode functionality
  - Separation of the framework from the actual choices of patterns and delimiters
  - Keeping the framework largely orthogonal to previous discussions of sync patterns, delimiters, PMA rates etc.
- Recognize that the upstream synchronization function is logically separate from the data detector (and that logical stack should capture this).
- Fully depict the separate phases (ie. AGC/CDR, FEC Block alignment) of the upstream sync sequence
- Address each alignment issue at the appropriate sublayer (ie. 66b encoder sublayer, Scrambler sublayer, FEC sublayer)

Observations on PCS and Data Detector for 64b/66b code (ONU)

1. Data detector's job: to turn on the laser in advance of the actual data transmission and turn it off afterward

    - Must interpret the GMII/XGMII control and data codes to do this
    - In 802.3ah the data detector resides at the bottom of the stack (ie. after IDLE deletion) and decodes the 10bit symbol

2. In 10GEPON we need a new logical function (either co-located with the data detector or separate from it) to manage the control sequences, transmissions, and state transitions for AGC/CDR and Burst Mode Frame Synchronization

    - Call this function the *burst mode synchronizer*

3. PCS layer *behaves differently* before frame synchronization is complete (ie. IDLE substitution, no scrambling, etc.) and afterward

    - Logical stack should capture this

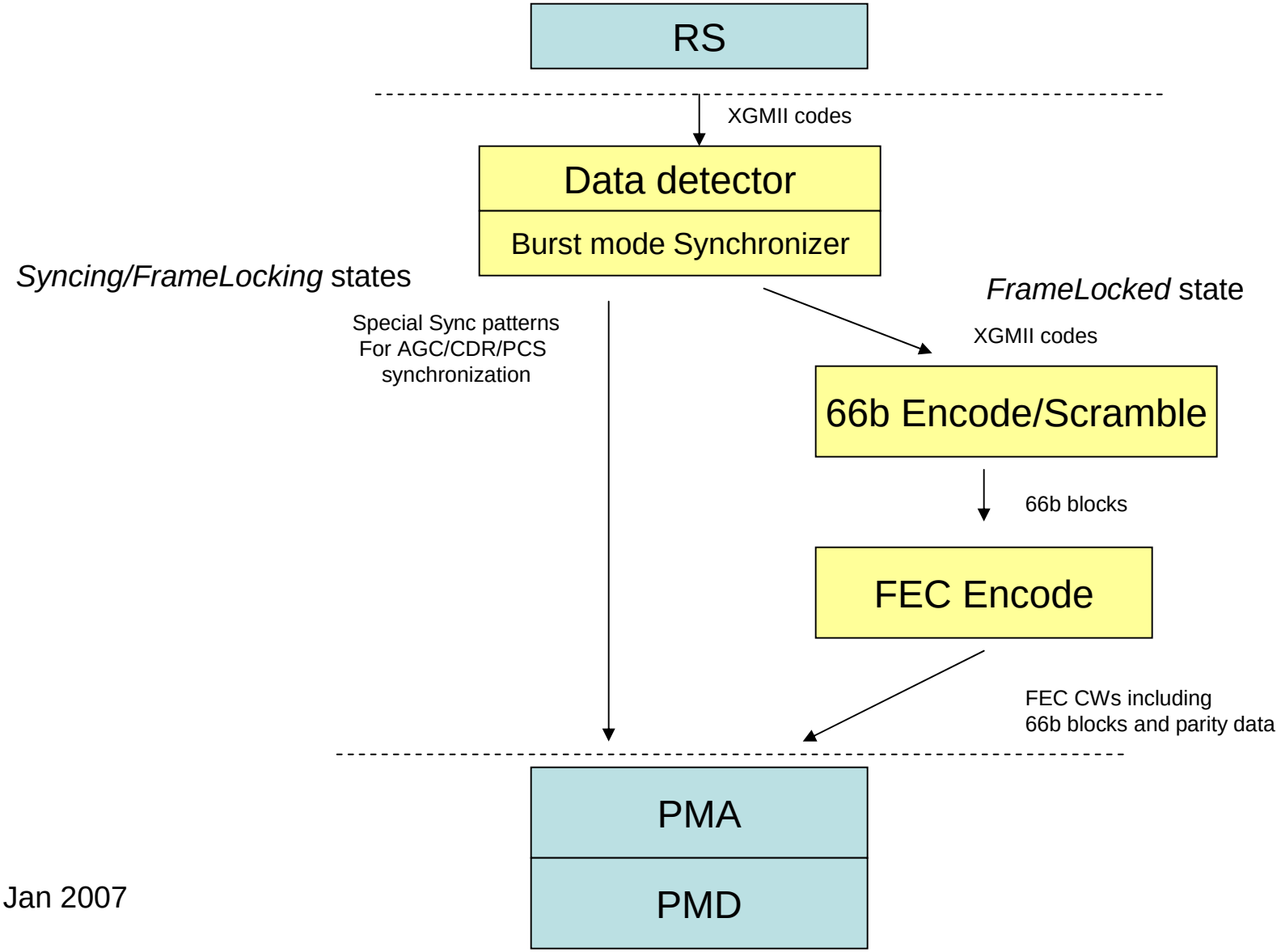
4. /S/ may appear in the first lane of any 32bit XGMII word. PCS must manage the synchronization process in a manner that assures that the /S/ will be in the data position of the 66b block (ie. first or fifth) required by coding rules

PCS and Data Detector for 64b/66b code (ONU)

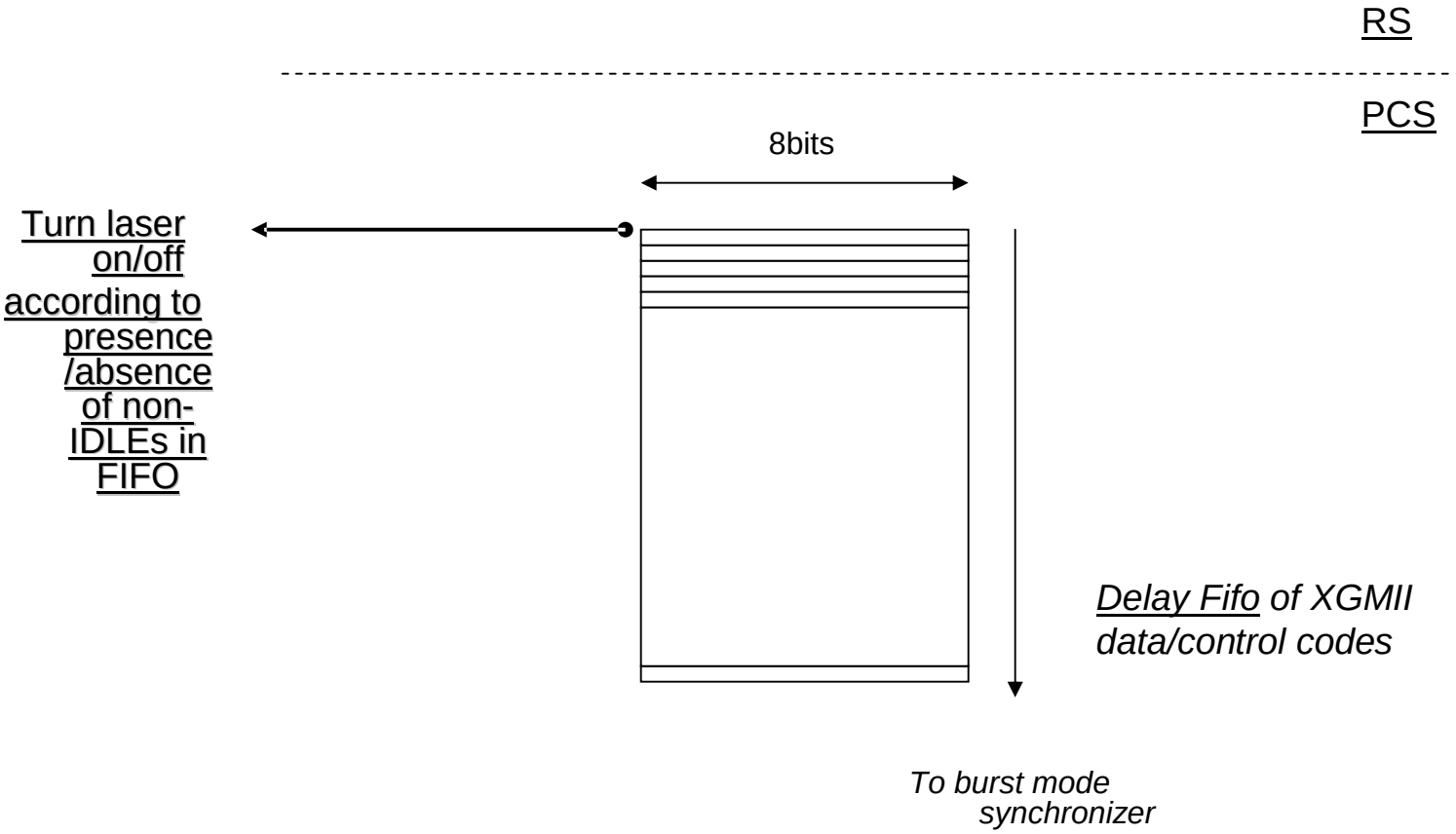
Consequently:

- Natural location in the stack for the 10GEPON data detector and syncing function is at the top of the PCS (just below the XGMII).
  - This way no decoding/recoding is necessary.
- Logical path thru the PCS is determined by *burst mode synchronizer* state
- Synchronizing function includes alignment logic

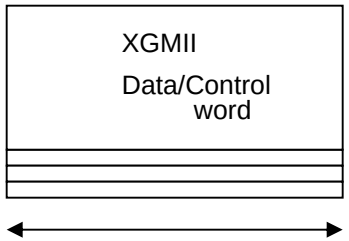
Placement of Data Detector/Synchronizer



Data detector internals



Burst Mode Synchronizer internals



Synchronizer FIFO –
Depth is according to Delimiter length and PMA rate

8bits

Check for Transition to next sync state based on FIFO content

Check *Sync State*

Syncing

Write 16b sync pattern (eg. 0x5555) to PMA (at PMA nominal clock rate)

Frame Locking

Write next 16bits of Delimiter to PMA (PMA nominal clock rate)

Locked

Send XGMII code to 66b encoder/scrambler

PCS

Synchronizer State Transitions

- When FIFO contains only IDLE
  => enter *Syncing*

- When “trigger” position in the FIFO (corresponding to lead time needed for delimiter transmission) contains START
  => enter *FrameLocking*

- When first position in the FIFO contains START
  => enter *Locked*

  - Note: If OLT’s scrambler definition is such that it needs data to initialize its state (ie. self-synchronous), then *Locked* state takes effect when START reaches the ninth slot in the FIFO (rather than the first). *FrameLocking* state would take effect earlier as well and the FIFO length would be longer.

Thank you