Upstream Synchronization Framework Update

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ONU PCS Functional Block Diagram
(transmit direction)

RS

36 bit XGMII

Burst Mode Controller

66b

64b/66b Encoder

66b

Scrambler

66b

FEC Encode

66b

SyncData
Transmit

66b

Gearbox

tx_code-group<15:0>

New

Modified

Unchanged

Laser On/Off

PMA

PMD

Feb 2007

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2
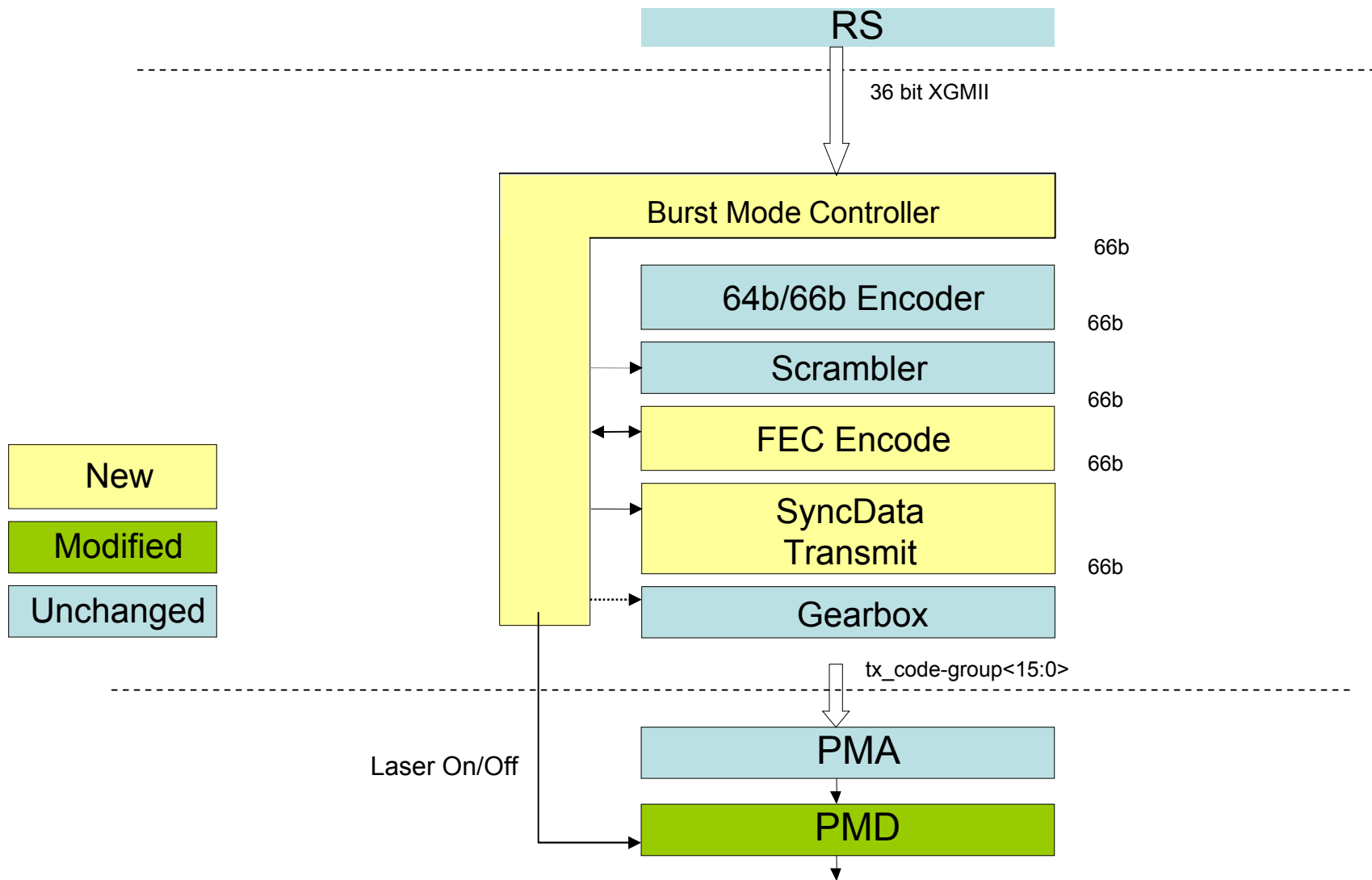
Elements in the Functional Block Diagram

a)   *Burst Mode Controller (BMC)*

- Functional element which includes 2 processes:

    - data detector process

    - burst mode control process
        - Invokes "laser-on/laser-off" function in PMD
        - Controls the generation of synchronization patterns (ie. burst preamble and delimiter) during initialization
        - \<Performs necessary alignment and reset of the datapath\>

b)   *FEC encoder*

- Builds FEC codewords (ie. calculates and inserts parity to datastream)
- Reports "End of Burst" to the BMC

c)   *Sync Data Transmit*
- During the initialization phases: <u>periodically</u> writes the appropriate initialization data pattern (*Initdata*) to the gearbox
- After initialization: passes the output from the FEC encoder to the gearbox

Elements in the Functional Block Diagram (2)

a) *64b66b encoder*

- No changes, but the contents of the input vector tx_raw<71:0> (clause 49.2.13) will be aligned by the Burst Mode Control process

b) *Scrambler*

- No changes, but the scrambler is (optionally) reseeded and restarted by the Burst Mode Control process

c) *Gearbox*

- No changes, but the gearbox can be reset or realigned by the Burst Mode Control process

Data Detector Delay Line (FIFO)

(SyncTime + DelimiterTime
+ 16 leading IDLES)

Trigger offset for *Data_pending* Signal

0

XGMII words (36 bits)
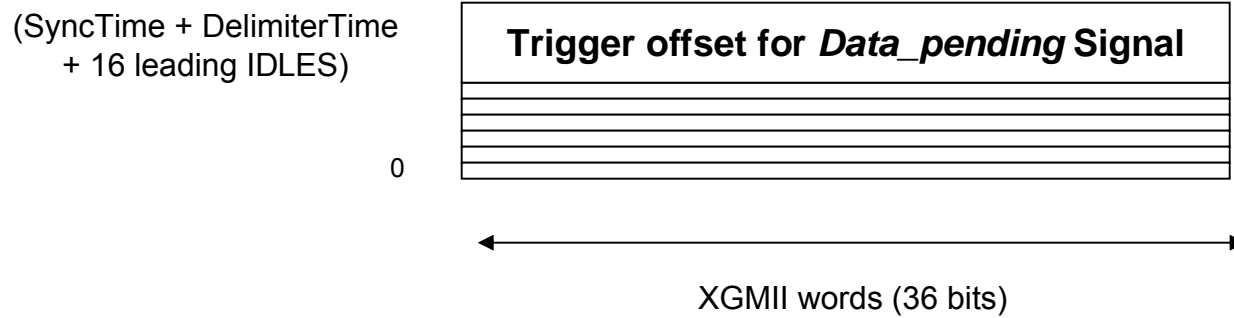
Data Detector State Diagram

```
                        DD_WAIT_ON_XGMII
```

TX != ||IDLE|| TX = ||IDLE||
(cf. clause 48.2.6)

```
      DD_DATA_ARRIVAL                        DD_IDLE_ARRIVAL
       idleLength <=0                          idleLength++
      Data_pending <= 1
```

                                    idleLength >   else
                                     delayBound

                 UCT

```
                              DD_END_OF_BURST
                               Data_pending <= 0
```

                                         UCT

```
                              DD_ADVANCE_FIFO
                   Dtx_code-group = FIFO.RemoveHead
                          FIFO.Append (TX)
```

                                         UCT
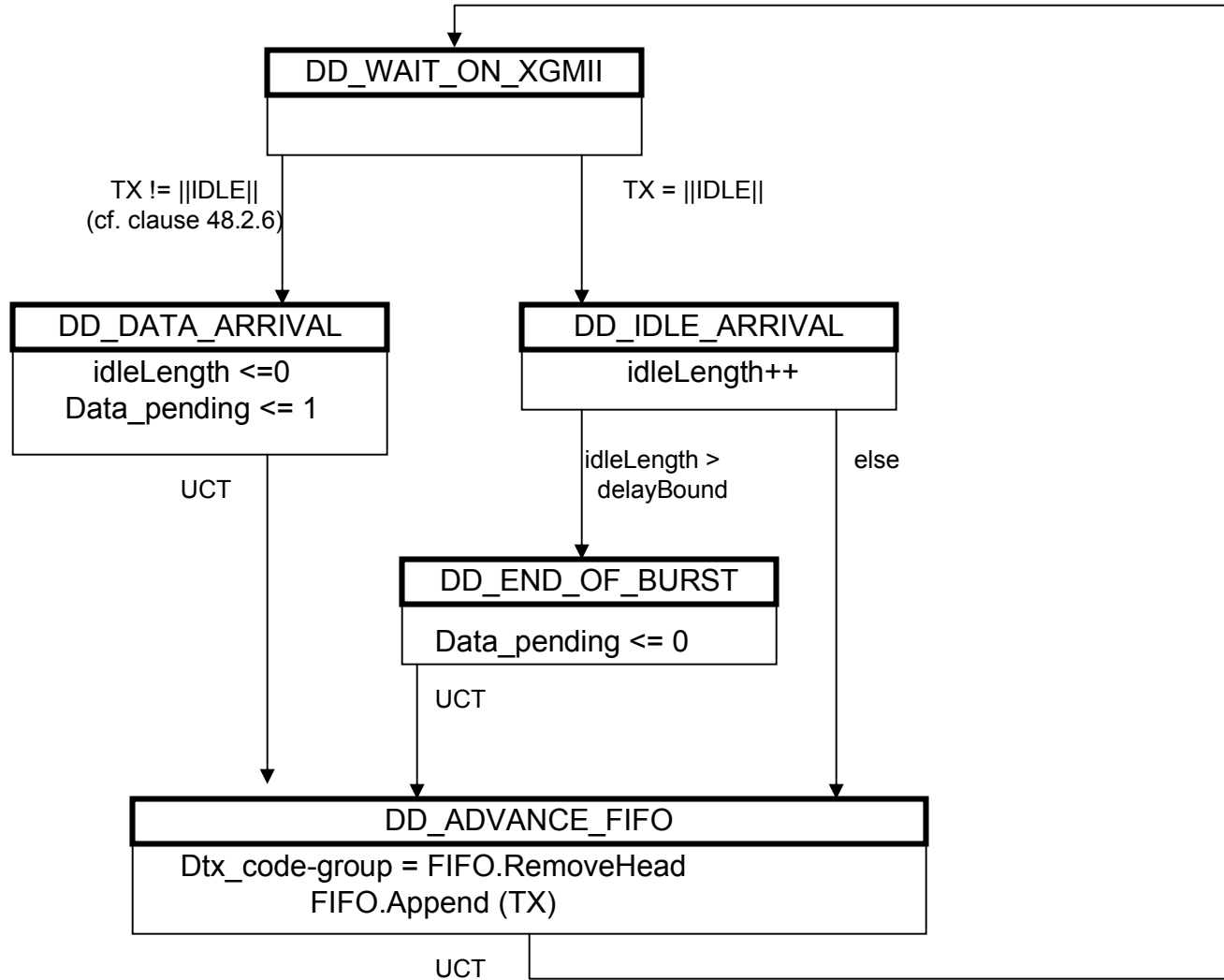
State Diagram for *Burst Mode Control*

```
                          ┌──────────────────────────────────────────┐
                          │                                          │
                          ▼                                          │
        ┌─────────────────────────────────┐                         │
        │      BC_LASEROFF_PHASE          │                         │
        ├─────────────────────────────────┤                         │
        │        PMD.Signal(False)        │                         │
        │                                 │                         │
        └─────────────────────────────────┘                         │
                          │                                          │
                          │   Data_Pending =1                        │
                          ▼                                          │
        ┌─────────────────────────────────┐                         │
        │        BC_CDR_PHASE             │                         │
        ├─────────────────────────────────┤                         │
        │    InitData <= SyncPattern      │                         │
        │    Select_Initdata <= 1         │                         │
        │       PMD.Signal(True)          │                         │
        └─────────────────────────────────┘                         │
                          │                                          │
                          │   SyncTime has elapsed                   │
                          ▼                                          │
        ┌─────────────────────────────────┐                         │
        │      BC_FRAMING_PHASE           │                         │
        ├─────────────────────────────────┤                         │
        │  InitData <= DelimiterPattern   │                         │
        └─────────────────────────────────┘                         │
                          │                                          │
                          │   DelimiterTime has elapsed              │
                          ▼                                          │
        ┌─────────────────────────────────┐                         │
        │       BC_DATA_PHASE             │                         │
        ├─────────────────────────────────┤                         │
        │      Select_Initdata <= 0       │                         │
        └─────────────────────────────────┘                         │
                          │   Burst_Complete =1                      │
                          └──────────────────────────────────────────┘
```
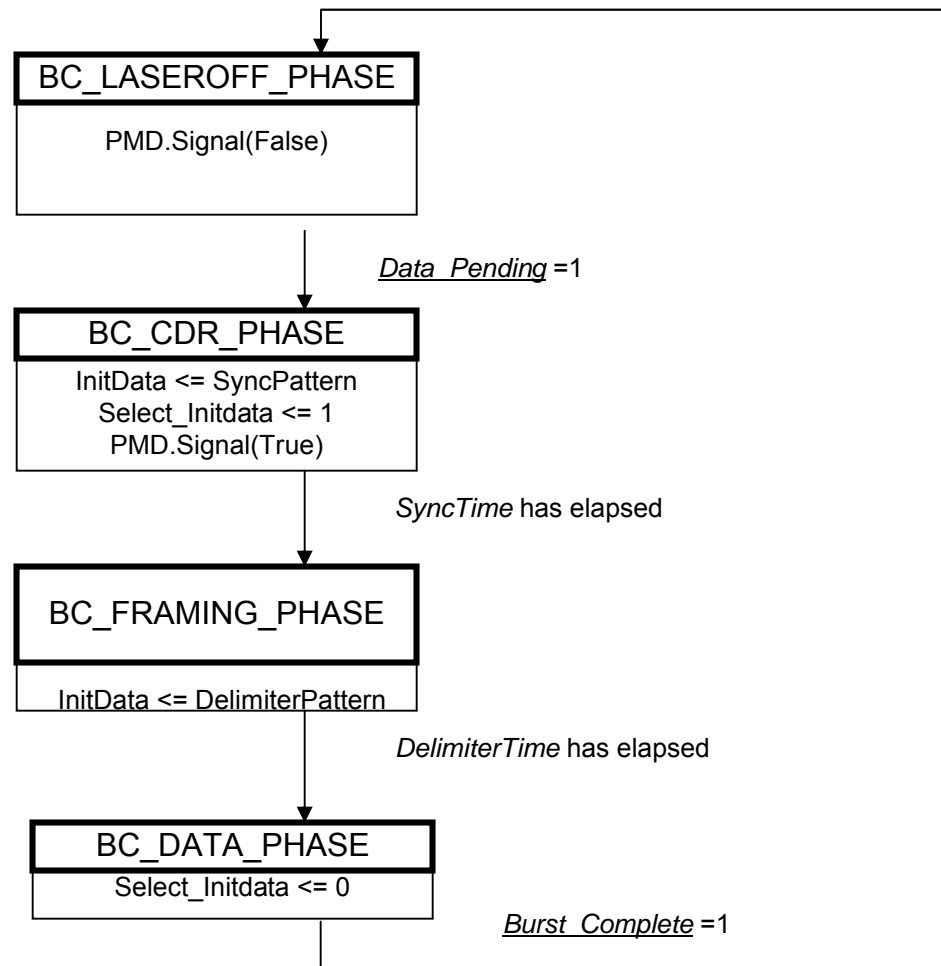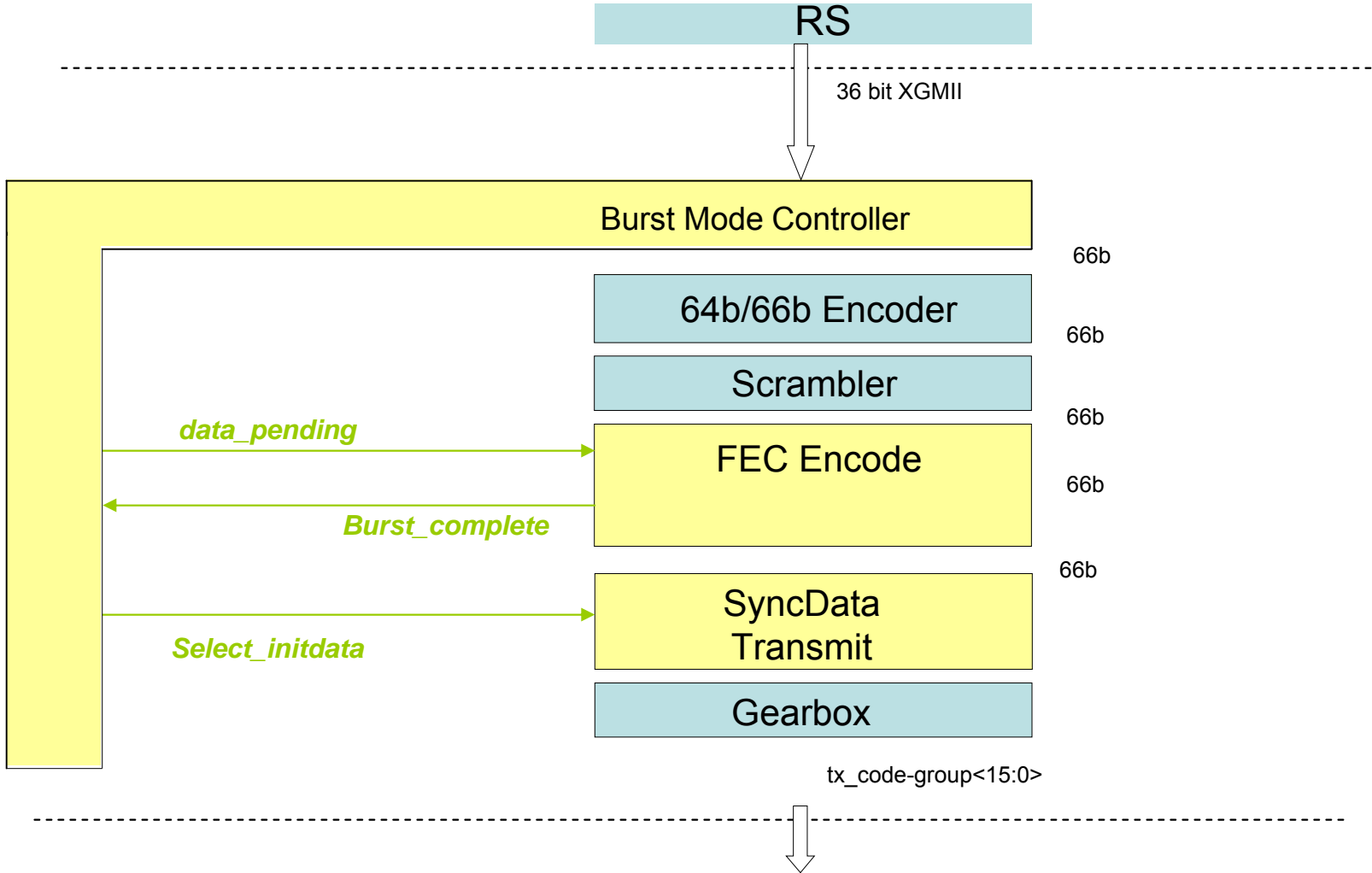
Entry to Data_Phase

Additional actions are performed when the BMC transitions to data_phase:

a)   Align the contents of the input vector tx_raw<71:0> (clause 49.2.13) so that /S/ will appear in column 0 and similarly align the gearbox output (eg. Clearing the FIFO of the gearbox when the correct alignment is achieved)

b)   Reset the FEC encoder so that codeword build restarts

c)   Optionally: reseed the scrambler
- ONU shouldn't be *required* to maintain the same seed between bursts
- Start of burst always contains the same data, so there might be a security or DC-balance advantage to reseed.

ONU PCS Functional Block Diagram (transmit direction)

RS

36 bit XGMII

Burst Mode Controller

66b

64b/66b Encoder

66b

Scrambler

66b

data_pending

FEC Encode

66b

Burst_complete

66b

Select_initdata

SyncData Transmit

Gearbox

tx_code-group<15:0>

Thank you

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